MN-3
August 2011 QE

1. Sketch and identify the physical features of a conventional Si NMOSFET. This is an inversion-type enhancement-mode NMOSFET fabricated on a p-type Si substrate. (15 points)

2. Based on the above structure, considering a submicron NMOSFET with L=0.25 μm, Z=5 μm, $N_A=10^{17}/cm^3$, $\mu_n=500 cm^2/Vs$, $C_{ox}=3.45\times10^{-7}$ F/cm^2, and $V_T=0.5$ V, find the channel conductance for $V_G=1$ V and $V_D=0.1$V. (20 points)

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3. Sketch and identify the physical features of a depletion-mode Si NMOSFET on a p-type Si substrate, in contrast to Problem 1. How do you distinguish a depletion-mode NMOSFET from an enhancement-mode NMOSFET through electrical characterization? (Hint: Plot the respective transfer characteristics.) (15 points)

4. Assume that the device in Problem 1 and Problem 2 is based on SiO_2/Si technology. Calculate the equivalent oxide thickness (EOT) of SiO_2 for the device in Problem 2. In order to reduce the gate oxide leakage current, a high-k dielectric is used for advanced Si technology. Envision using a composite high-k structure with the same EOT as the one in Problem 2. The composite structure is assumed to be composed of 1 nm SiO_2 on Si channel, x nm HfO2 (k=20) in the middle, and 1 nm SiO_2 on top next to the metal gate. Calculate the HfO_2 thickness. (10 points)

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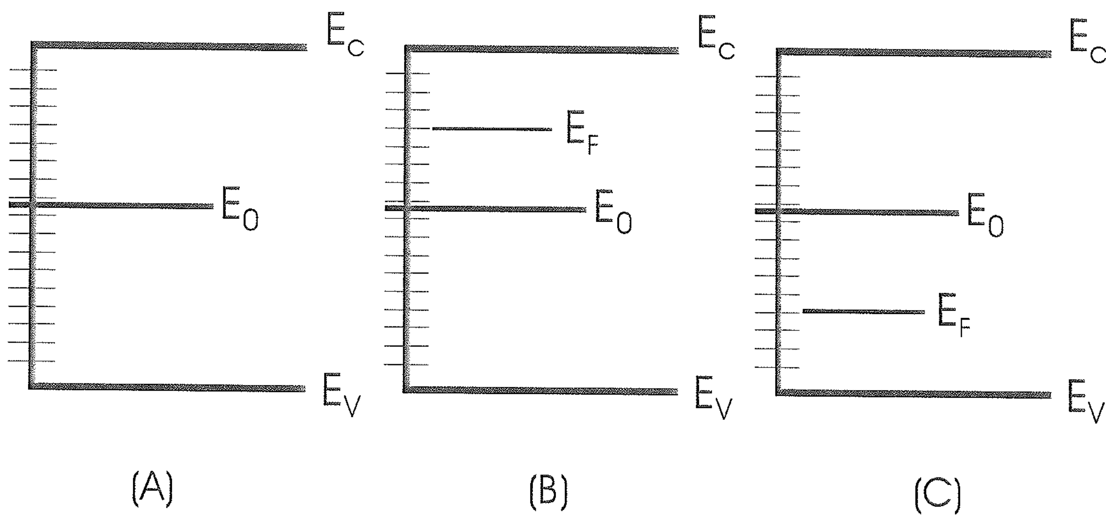
5. A High-k dielectric (HfO_2) directly on Si leads to a higher interface trap density at the HfO_2/Si interface compared to the SiO_2/Si interface. In Sze and Ng's book on Page 214, the trap neutral level E_0 is used to describe a non-ideal oxide-semiconductor interface. Figure A shows that the trap neutral level E_0 locates in between the conduction band minimum and valence band maximum. Identify which part of trap states are dominated by donor-type trap states and which part of trap states are dominated by acceptor-type states in Figure A. If the Fermi level E_F is located above E_0, identify which part of traps are filled in Figure B and the sign (+ or – or neutral) of these traps. If the Fermi level E_F is located below E_0, identify which part of traps are empty in Figure C and the sign (+ or – or neutral) of these traps. (10 point)



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6. Sketch the low-frequency and high-frequency C-V characteristics (y-axis C; x-axis V) of an ideal SiO_2/Si MOS capacitor. What kind of low-frequency and high-frequency C-V curves will be obtained if the measurement is performed on a HfO_2/Si MOS capacitor with the same EOT but with a significant interface trap density. Please draw all four C-V curves into the same plot. Draw to scale. (10 point)

7. Interface traps affect C-V characteristics and on-state performance of a MOSFET. They also affect the off-state performance of a device. In the presence of a significant interface trap density D_{it}, the sub-threshold slope becomes S (with D_{it})=(ln10)(kT/q)(1+C_{it}/C_{ox}). If the measured value for S is 100 mV/dec, and we assume the device in Problem 4, what is the average D_{it} for the composite oxide/Si interface? If we cannot improve the interface by means of an optimized process, how could one still achieve a device with S=80 mV/dec ? (20 points)

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