1. Sketch and identify the physical features of a conventional Si NMOSFET. This is an inversion-type enhancement-mode NMOSFET fabricated on a p-type Si substrate. (15 points)

2. Maintain a constant electric field as dimensions are scaled down by κ. Given the gate length L and the gate width W is scaled down to L/κ and W/κ. How should (1) dielectric thickness t_{ox} (2) junction depth x_j (3) p-type Si substrate doping density N_A, and (4) supply voltage V_{DD} be scaled down to maintain a constant electric field. (10 points)
Hint: Consider the electric field in the gate under strong inversion condition and the electric field in the drain-substrate reverse biased junction.

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3. Based on the structure in Problem 1, considering a submicron NMOSFET with L=0.25 μm, Z=5 μm, $N_A=10^{17}/cm^3$, $\mu_n=500 cm^2/Vs$, $C_{ox}=3.45x10^{-7}$ F/cm², and $V_T=0.5$ V, find the channel conductance for $V_G=1$ V and $V_D=0.1$V. (20 points)

4. Sketch and identify the physical features of an inversion-type and enhancement-mode Si PMOSFET on an n-type Si substrate, in contrast to Problem 1. What are the typical inversion mobility values for Si NMOSFETs and Si PMOSFETs ? (15 points)

5. Assume that the devices in Problem 1 and Problem 4 are based on SiO_2/Si technology. Calculate the oxide thickness of SiO_2 for the device in Problem 3. Dielectric constant for SiO_2 is 3.9. In order to reduce the gate oxide leakage current, a high-k dielectric is used for advanced Si technology. Envision using a composite high-k structure with the same capacitance as the one in Problem 3. The composite structure is assumed to be composed of 0.5 nm SiO_2 on Si channel, x nm HfO2 (k=20) in the middle, and 0.5 nm SiO_2 on top next to the metal gate. Calculate the HfO_2 thickness. (10 points)

6. Sketch the low-frequency and high-frequency C-V characteristics (y-axis C; x-axis V) of an ideal SiO_2/Si p-type MOS capacitor. What kind of low-frequency and high-frequency C-V curves will be obtained if the measurement is performed on a HfO_2/Si MOS capacitor with the same EOT but with a significant interface trap density. Please draw all four C-V curves into the same plot. Draw to scale. (10 point)

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7. Interface traps affect C-V characteristics and on-state performance of a MOSFET. They also affect the off-state performance of a device. In the presence of a significant interface trap density D_{it}, the sub-threshold slope becomes S (with D_{it})=(ln10)(kT/q)(1+C_{it}/C_{ox}). If the measured value for S is 100 mV/dec, and we assume the device in Problem 3 or 5, what is the average D_{it} for the composite oxide/Si interface? If we cannot improve the interface by means of an optimized process, how could one still achieve a device with S=80 mV/dec ? (15 points)

8. If the measured Si NMOSFET in Problem 1 has threshold voltage V_T=-0.2V instead of the desired enhancement-mode operation with V_T>0, what can we do to realize V_T>0 in terms of process? (hint: modern high-k/Si devices use metal gate process) (5 points)