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Review

Interfacial chemistry of oxides on $In_xGa_{(1-x)}As$ and implications for MOSFET applications

C.L. Hinkle [a], E.M. Vogel [a], P.D. Ye [b], R.M. Wallace [a,*]

[a] Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, TX 75044, USA
[b] School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, USA

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ABSTRACT

The prospect of enhanced device performance from III–V materials has been recognized for at least 50 years, and yet, relative to the phenomenal size of the Si-based IC industry, these materials fulfilled only specific niches and were often referred to as "the material of the future" [1]. A key restriction enabling widespread use of III–V materials is the lack of a high quality, natural insulator for III–V substrates like that available for the SiO_2/Si materials system [2]. The prospect of impending scaling challenges for technologies based on silicon metal oxide semiconductor field effect transistor (MOSFET) devices has brought renewed focus on the use of alternate surface channel materials from the III–V compound semiconductor family. The performance of the traditional MOSFET device structure is dominated by defects at the semiconductor/oxide interface, which in turn requires a high quality semiconductor surface. In this review, reflecting the authors' current opinion, the recent progress in the understanding of the dielectric/III–V interface is summarized, particularly in regard to the interfacial chemistry that impacts the resultant electrical behavior observed. The first section summarizes the nature of the oxidation states of surface oxides on $In_xGa_{1-x}As$. Then the atomic layer deposition of such oxides on the $In_xGa_{1-x}As$ surface is summarized in view of the interfacial chemical reactions employed. Finally the resultant electrical properties observed are examined, including the effects of substrate orientation. Portions of this review have been published previously [3,4].

1. $In_xGa_{(1-x)}As$ semiconductors and their oxides

Work on gate dielectrics for GaAs MOSFETs extends into the 1960s [5], with the relative complexity of the capacitance–voltage behavior recognized early on for a number of substrate orientations [6]. The early work on gate dielectrics for GaAs entailed studies of surface oxidation through chemical, thermal, anodic, and sputter deposition methods [7,8]. Fundamental studies on the effects of GaAs surface oxidation and the resultant interface states were also reported, highlighting the effects of Fermi level pinning [9]. The prospects and challenges for InGaAs MOSFETs have also been previously summarized [10]. However, with the introduction of atomic layer deposition (ALD) into Si-based IC fabrication for high-k gate dielectric applications [11], a new vista of gate dielectric material choices are now available for consideration in III–V devices.

As $In_xGa_{(1-x)}As$ alloys have a bandgap of ($0.36 \leqslant E_g \leqslant 1.42$ eV) and $E_g \geqslant 14$ kT, these alloys are potentially suitable for many applications with power supply operating voltages $\leqslant 0.5$ V envisioned for short gate lengths ($L_g \leqslant 20$ nm), such as low stand-by power applications. Alloys with an In content greater than 50% are of particular interest for NMOS applications as the bulk electron mobility is very high ($\sim 10^4$ cm^2/Vs) relative to Si ($\sim 10^3$ cm^2/Vs), thus potentially enabling high performance surface channel devices. With the possibility of leveraging existing Si-fabrication investments, interest in the (1 0 0) orientation of these materials is particularly acute and lattice-matched epitaxial growth schemes have been recently demonstrated for $In_xGa_{1-x}As$ devices with an underlying Si(1 0 0) substrate [12,13].

High quality InGaAs is typically grown on various III–V substrates such as GaAs, InP and InAs using epitaxial techniques. The desired indium concentration dictates the substrate choice due to defects such as misfit dislocations. Since the indium atom is larger than gallium, the maximum indium concentration that can be grown on GaAs is limited by strain arising from lattice constant mismatch between the substrate and the InGaAs layer. Replacing 20% of the gallium with indium allows for the growth of a high quality, 20 nm thick $In_{0.2}Ga_{0.8}As$ channel relatively free of misfit dislocations and other defects. Higher content In channels can be achieved through epitaxial growth on substrates with better lattice matching parameters, such as InP.

The viability of field effect electronic devices made of III–V compound semiconductors has long been hindered by the presence of

* Corresponding author. Tel.: +1 972 883 6638; fax: +1 972 883 6629.
E-mail address: rmwallace@utdallas.edu (R.M. Wallace).

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defects at the interface between the semiconductor and gate insulator. Despite having been studied in great detail for more than 30 years, these interfaces and the identification of the bonding configurations that cause the defects has remained challenging [14–17]. In contrast, this issue has been acceptably solved in well established Si-based MOSFETs since the 1960s, and is largely due to the superior thermally grown oxide for Si, *viz.* SiO_2, which forms an interface that can be rendered with an acceptably low (midgap) interface state density ($D_{it} \cong 5 \times 10^{10}/cm^2\,eV$ for $SiO_2/Si(1\,0\,0)$) *after* exposure to hydrogen from, for example, forming gas anneals [18–22]. Problems with MOS devices on GaAs and InGaAs, including frequency dispersion of capacitance and sub-optimal electron mobility, have been attributed to a number of different native surface species including Ga–O bonds, As–O bonds, elemental As, and As and Ga anti-sites [23–25]. An understanding of the specific bonding configurations that arise on III–V semiconductors has great implications for the electronics industry contemplating the move away from Si-channel devices to those with higher mobility, such as $In_xGa_{1-x}As$.

The $In_xGa_{(1-x)}As$ alloy exhibits a variety of surface reconstructions [26]. Since the In–As bond is slightly weaker, free indium and arsenic is readily created on the surface. At temperatures higher than 500 °C, preferential desorption of As_2 is observed leading to the (2×4) reconstruction changing to a (4×2) indium rich surface. In order to observe the (4×4) enriched-As surface reconstruction, one must maintain temperatures below 380 °C. Recent atomic resolution scanning tunneling microscopy studies of the (2×4) reconstruction indicate that the defect density is larger for $In_{0.53}Ga_{0.47}As(1\,0\,0)$ in comparison to $InAs(1\,0\,0)$ [27].

Even at temperatures lower than 500 °C, the surface composition can be manipulated through vacuum annealing as well as exposure to atomic hydrogen under UHV conditions. The loss of indium is reported using *in situ* X-ray photoelectron spectroscopy (XPS) analysis [28]. Fig. 1 shows the Ga3*d*/In4*d* region of the XPS spectrum with various atomic hydrogen exposures. This loss is attributed to the formation of volatile hydrides at these conditions. It is seen that As-oxides and Ga-oxides on the surface can be readily reduced from vacuum annealing and/or exposure to atomic hydrogen [29]. The loss of surface indium is accompanied by the narrowing of indium features in the XPS spectrum. Fig. 1c illustrates this change as the In3*d* peak, obtained after a protective As-cap is desorbed (blue curve), narrows following 30 (red) and 90 (black) minute exposures to atomic hydrogen. The exact chemical state responsible for this shoulder feature is not clear, but it does make the correct indium oxide peak assignment challenging as will be illustrated below.

In addition to the improvement in bulk electrical properties obtained by alloying GaAs with InAs, the $In_xGa_{1-x}As$ surface offers distinct advantages in chemical behavior. Brammertz et al. [30] have shown a comparison of photoluminescence intensity measurements taken on GaAs vs. InGaAs interfaces with their respective native oxides. Their results indicate that replacing just 15% of Ga with In results in a reduction of the surface recombination velocity by an order of magnitude. These results indicate that InGaAs surfaces are expected to be easier to chemically passivate then GaAs. The use of photoluminescence as a tool to screen oxide/III–V materials systems has also been recently summarized [31].

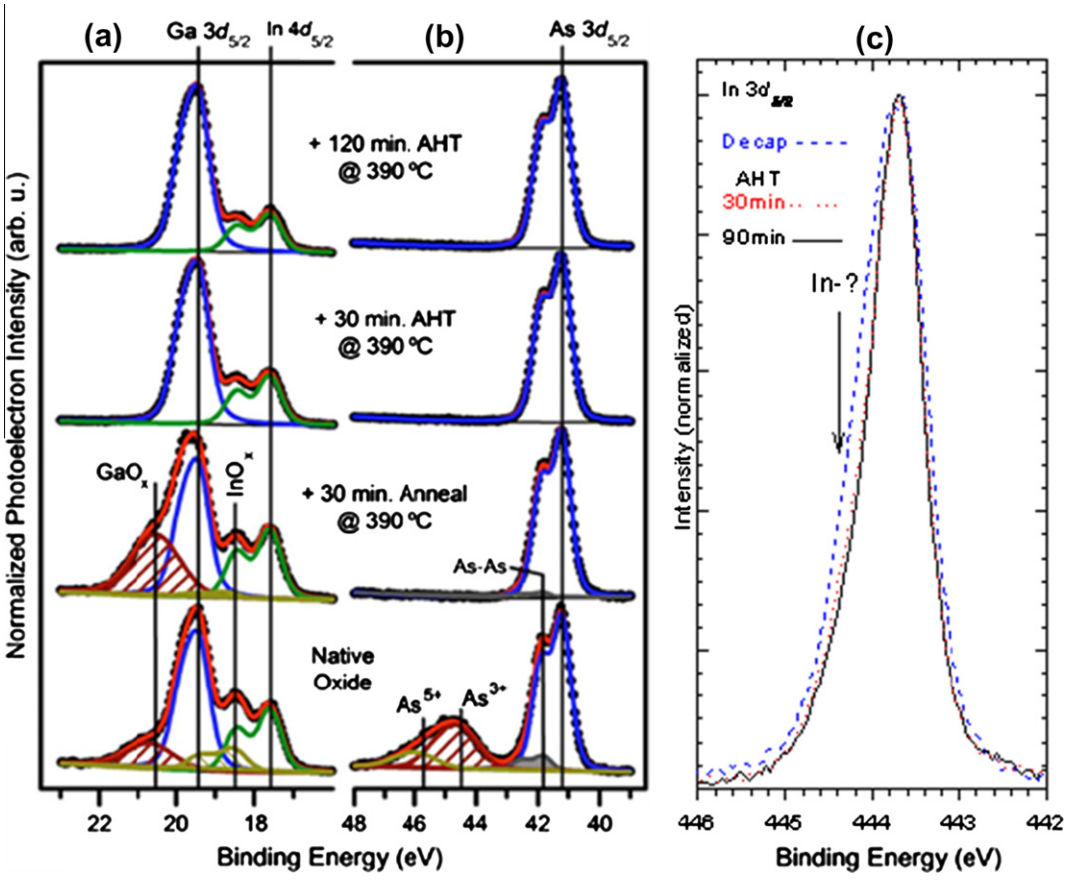

Fig. 1. XPS spectra of $In_{0.2}Ga_{0.8}As$ after annealing/exposure to atomic hydrogen produced by thermal cracking of H_2. (a) From the Ga and In features as well as the (b) As spectra, removal of surface oxides as well as In is detected. (c) The narrowing of the asymmetric In $3d_{5/2}$ line is also evident. "AHT" = atomic hydrogen treatment [28]. Reprinted with permission, © 2008, American Institute of Physics.

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1.1. Stable oxidation states on $In_xGa_{(1-x)}As$

The stable oxides of $In_xGa_{(1-x)}As$ include As_2O_3, As_2O_5, Ga_2O_3, Ga_2O, In_2O_3, In_2O, $GaAsO_4$, and $InAsO_4$ [32]. Table 1 shows the Gibbs free energies [33] for the relevant *bulk* native oxides of $In_xGa_{(1-x)}As$. In discussing the relative stabilities of the As-oxides vs. In-oxides vs. Ga-oxides, a comparison of the $Metal_2O_3$ states shows the trend that the As-oxides are the most unstable while the Ga-oxides are the most stable (this holds true for other oxidation states as well, e.g. $Metal_2O$). While these trends may vary slightly for thin "surface only" oxides, the free energies of formation are a helpful guide in analyzing the progression of native oxides over a monolayer thick when exposed to elevated thermal budgets. Many of these stable oxides are therefore easily removed or converted to the more stable Ga oxides, in particular Ga_2O_3. The stability of this particular oxidation state makes it difficult to remove during typical chemical processing or relatively low temperature thermal desorption [34]. An in-depth study of the critical Ga-oxides [35] is presented in the next section.

For GaAs ($x = 0$), the low temperature grown native oxide (Fig. 2) consists primarily of As 5+, As 3+, Ga 3+, and Ga 1+ oxidation states in addition to a small amount of elemental As [36]. When the oxides are grown at higher temperature, or native/chemical oxides formed at low temperatures are subjected to an increased thermal budget, the composition of the oxide layer changes dramatically. As the Gibbs free energies predict, the less stable As-oxides become less prevalent as temperature increases eventually either evaporating away or being converted to the most stable oxide in this system Ga_2O_3 [34]. As–O bonding can then be further reduced by a post-etch, *in situ* anneal in vacuum up to 450 °C. Analysis of the corresponding O1*s* region for the annealed surface reveals that the O concentration (intensity) for the etched surface and the annealed surface is comparable, indicating no significant loss of oxygen and therefore suggesting that bond conversion from As–O bonding to Ga–O bonding is favored with such treatments. For temperatures above 500 °C, As-oxide is below the level of detection as the oxide is almost completely Ga_2O_3. According to Eq. (1) [32],

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \quad (1)$$

there should also be elemental As created for these higher temperature oxides which is reported in most of the literature. As noted above, this elemental As is located primarily at the interface, although some portion may subsequently diffuse through the Ga_2O_3 to form $GaAsO_4$-like areas. Any As-oxides that may be formed via this elemental As diffusion to the surface is likely to be highly unstable and would therefore evaporate upon heating [37].

InAs ($x = 1$), despite having fundamentally the same phase diagram [38] as GaAs has a different oxide growth structure primarily due to the relative thermodynamic stabilities of the possible native oxides (Fig. 3). Whereas for GaAs, Ga_2O_3 was the most stable of the possible oxides, for InAs the most stable compound is $InAsO_4$ [32]. Therefore, for thermally grown oxides above 350 °C, the oxide consists almost entirely of ternary $InAsO_4$ (although $InAsO_3$ has been suggested as a possibility as well) with minimal elemental As at the interface. For air-grown native oxides, the structure is similar to that of GaAs, with As 5+, As 3+, and In 3+ species present in XPS spectra.

Table 1
List of stable InGaAs-oxides and their bulk oxide Gibbs free energies. Also shown are XPS core-level binding energies of the stable oxides. All binding energies observed by XPS are measured with respect to the semiconductor Fermi level. As such, exact peak positions must be adjusted to take doping concentration, charging, and band bending into consideration. Relative shifts such as the energy difference from the adventitious C 1*s* peak or shifts with respect to the bulk semiconductor peak are commonly used to determine chemical states rather than absolute binding energies.

Oxide	Gibbs free energy, ΔG (kcal/mol)	XPS core-level binding energy (eV)
Ga_2O	−75.3 [33]	1117.3 (2*p*3/2) [35], 19.6 (3*d*) [35]
Ga_2O_3	−238.6 [33]	1117.9 (2*p*3/2) [35], 20.2 (3*d*) [35]
$GaAsO_4$	−212.8 [33]	1118.8 (2*p*3/2) [32], 21.1 (3*d*) [32]
In_2O_3	−198.6 [32]	444.7 (3*d*) [32]
$InAsO_4$	−209.4 [32]	445.3 (3*d*) [32]
As_2O_3	−137.7 [33]	1325.4 (2*p*3/2) [34], 43.7 (3*d*) [34]
As_2O_5	−187 [33]	1326.7 (2*p*3/2) [34], 45.0 (3*d*) [34]

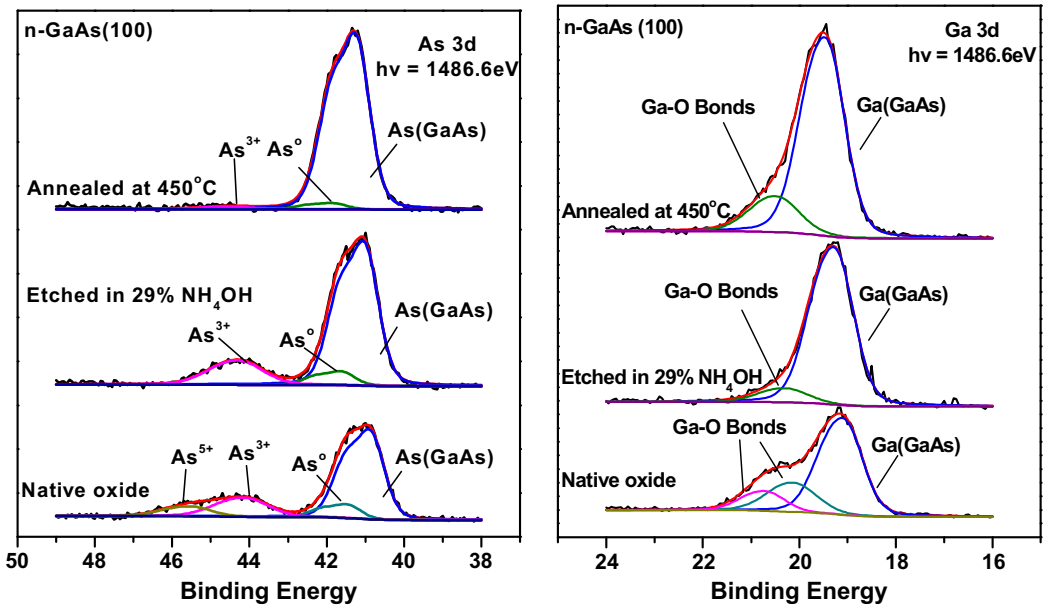

Fig. 2. XPS core-level spectra showing the oxidation states of GaAs native oxide. Two states are observed for both As and Ga. Chemically etching the native oxide removes much of the oxide including all of the As 5+ oxidation state. Anneals at temperatures greater than 350 °C convert all remaining As-oxides to the most thermodynamically stable oxide in the system, Ga_2O_3 [36]. As 0 denotes elemental As–As bonding. Reprinted with permission, © 2009, The Electrochemical Society.

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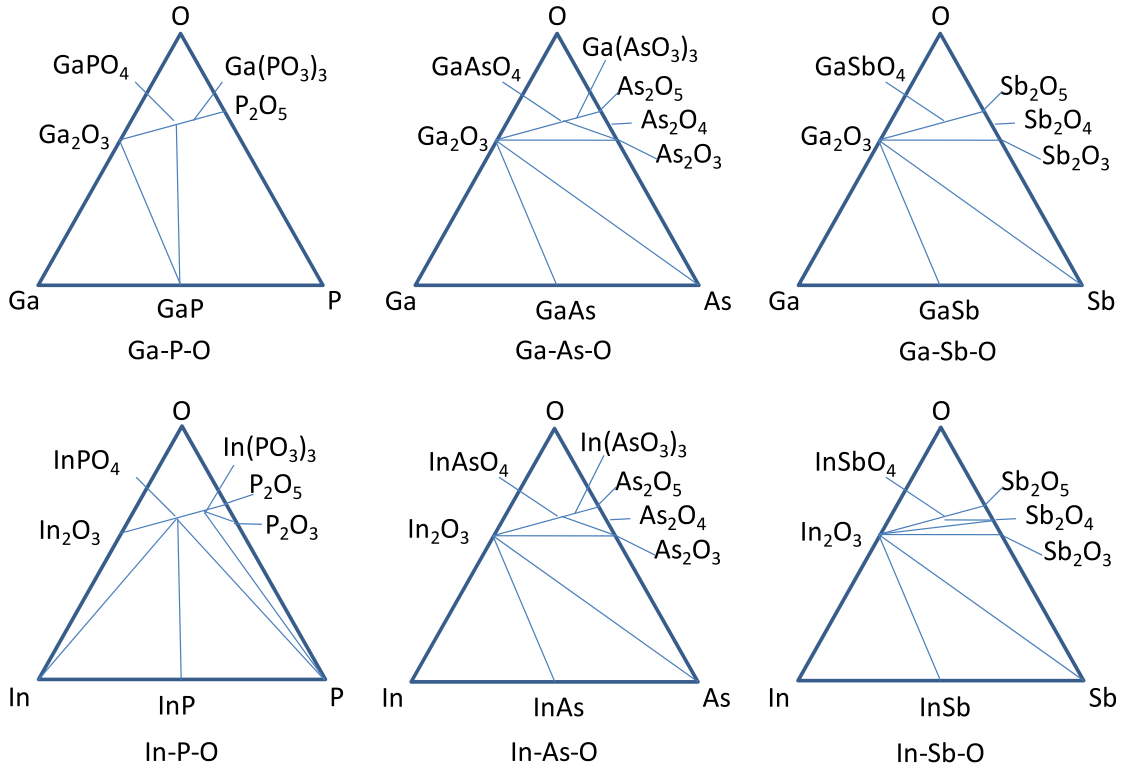

Fig. 3. Phase diagrams for III–V based systems. The similarities between the arsenides and the antimonides is noted [38]. Reprinted with permission, © 1983, Elsevier.

The alloy compounds ($0 < x < 1$) of $In_xGa_{(1-x)}As$ exhibit oxides that are once again consistent with thermodynamic values of stable bulk oxides. Low temperature (air-grown) native oxides consist of a mixture of oxides of each of the substrate elements, As 5+, As 3+, In 3+, Ga 3+ and Ga 1+ as well as a small amount of elemental As. Increasing the thermal budget either by anneal or thermal oxidation removes the As-oxides while increasing the amount of Ga 3+ and In 3+ oxidation states. During this bond reconfiguration, the amount of oxygen that gets transferred to Ga appears to be greater than the amount transferred to In [39]. It is noted that since there is no detectable As oxide at higher temperatures on $In_xGa_{(1-x)}As$ (up to at least $x = 0.65$), $InAsO_4$ is ruled out as a possible interfacial oxide in these systems. Additionally, as In content increases, the amount of air-grown Ga_2O_3 decreases even when normalized to the lower Ga content of these compounds (i.e., Ga_2O_3:GaAs decreases with increasing In content) [40]. This could be due to steric effects in which the increased size of the In atom reduces the available space for O to bond to the interfacial Ga atoms.

It is important to note a major complication with XPS studies of the In-oxides. The line-shape for In, even for a surface that has oxides below the limit of detection, can be asymmetric (Fig. 4) [41]. A useful curve fitting for this type of phenomenon is achieved by using a Doniach–Sunjic line-shape [42]. Using an incorrect line-shape for these spectra can, for example, lead to the misinterpretation of the presence or magnitude of the surface In-oxides.

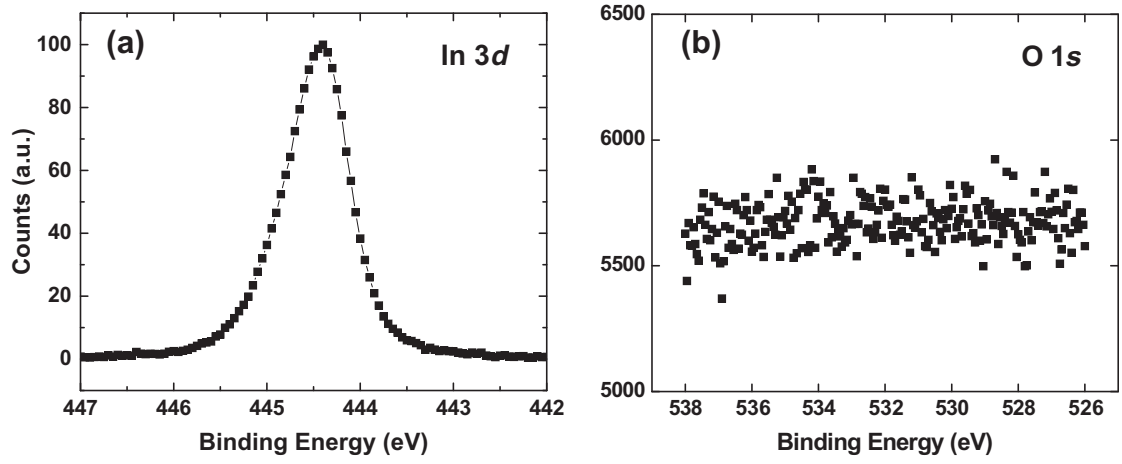

Fig. 4. (a) XPS core-level spectrum showing the asymmetric line-shape of the In feature. This asymmetry is not caused by an oxide as the oxygen (b) is below detectable limits. See [34].

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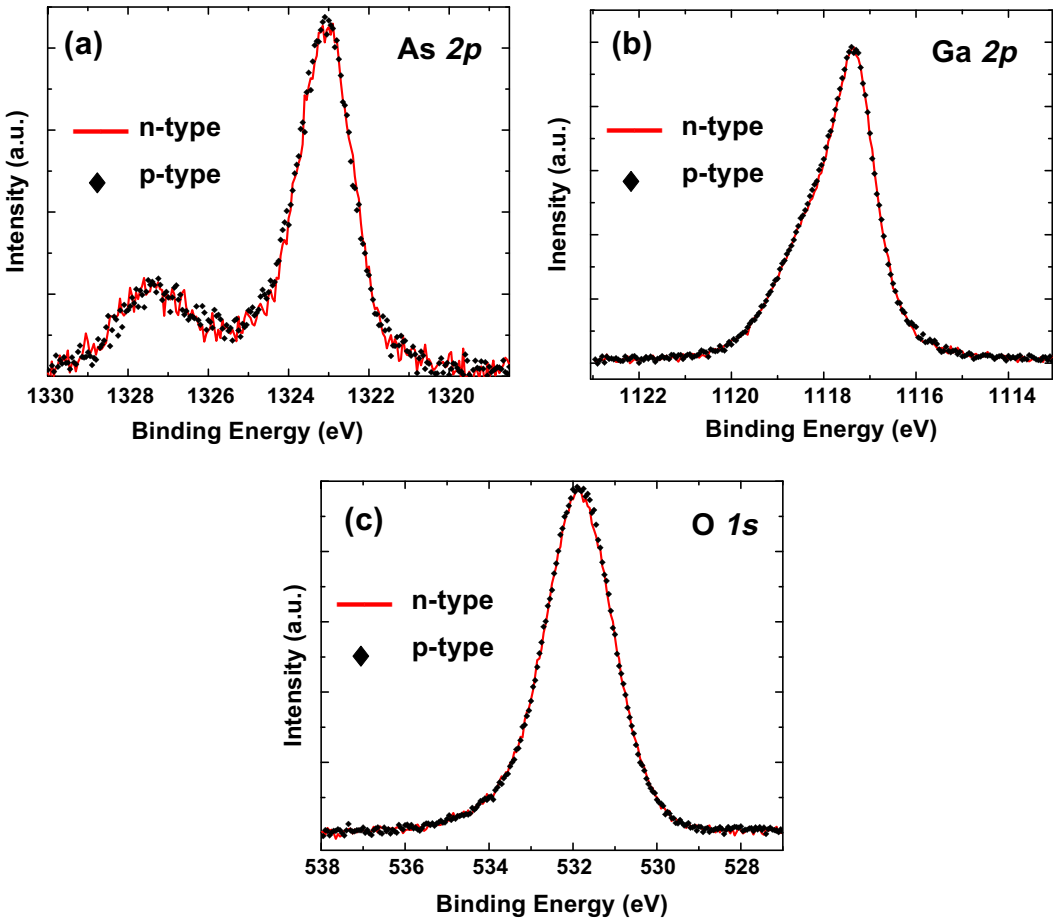

Fig. 5. XPS core-level spectra showing that oxide growth on GaAs does not depend on the semiconductor dopant. Ref. [46]. Reprinted with permission, © 2008, American Institute of Physics.

Exposure of the native oxides of $In_xGa_{(1-x)}As$ to chemical etches (notably HF and NH_4OH) appears to result in the reduction of the As–O bond concentration as well. Particularly of note is the complete removal by this chemical treatment of the As 5+ oxidation state leaving the As 3+ state as the only As–O surface bond (Fig. 2) [43–45]. These etch solutions also reduce the amount of Ga-oxide, but much less efficiently than for the As-oxides.

A critical comparison of the native oxide chemistry on *n*-GaAs and *p*-GaAs has been recently conducted where chemically indistinguishable interfacial oxides were observed upon NH_4OH etching and exposure to laboratory air and light, followed by Al_2O_3 ALD deposition [46]. The background-subtracted, normalized XPS spectra of the two companion GaAs substrates with chemical treatment followed by a 12 min atmospheric exposure fully overlap, clearly showing that the surfaces exhibit the same bonding environment to within detectible limits (Fig. 5). The extent of oxidation on these samples is chemically identical to each other for an *n*-type and *p*-type substrate. This shows that there is no difference detected in the oxidation rate or chemical state of the *n*- or *p*-type substrates as long as they are exposed to identical conditions. Al_2O_3 deposition on these same samples continues to show that *n*-type and *p*-type GaAs interfaces oxidize in identical manners. It is noted that the As *2p* and Ga *2p* spectra are very surface sensitive due to the binding energies of those core level electrons and are therefore particularly useful in analyzing interfacial oxides [41]. All other spectral ranges analyzed (Al *2p*, As *3d*, Ga *3d*, C *1s*) also show identical chemical states for both *n*-type and *p*-type substrates.

1.2. Ga-suboxides

Since the As-oxides can easily be removed with chemical or thermal treatment, the role of the most stable bound Ga native oxides, GaO_x, is of particular interest. Throughout the analysis described above, it is clear that residual Ga-oxides appear to be present at some level. To clarify the role of Ga-oxides, several experiments were conducted to control the Ga oxidation states on GaAs and $In_xGa_{(1-x)}As$ [35,36]. The accurate identification of the oxidation states of Ga is often thought to be limited to high photon intensity synchrotron photoelectron emission spectroscopy (PES) data and is usually only applied to the Ga 3*d* spectrum due to beam energy and monochrometer constraints. Nevertheless, such PES studies can provide superior depth resolution as the incident photon energy can be tuned so that the resultant photoelectron can have very low (<10 eV) kinetic energy. The study of this spectrum with typical laboratory-based X-ray sources results in energetic photoelectrons (photoelectron kinetic energy KE ≈ 1465 eV for an Al Kα X-ray source) resulting in a significant decrease in sensitivity to photoelectrons originating from the near surface region. In contrast, the Ga 2*p* spectrum (KE ≈ 369 eV) exhibits considerable surface sensitivity, but is notoriously difficult to deconvolve into individual chemical (oxidation) states due to the broad Gaussian widths of the peaks in conjunction with the proximity of the chemical state peak positions. Moreover, the Ga 2*p* extreme surface sensitivity makes *ex situ* studies difficult due to the ultra-thin films necessary for photoelectron transparency and the susceptibility of the film to spurious contamination and oxidation due to environ-

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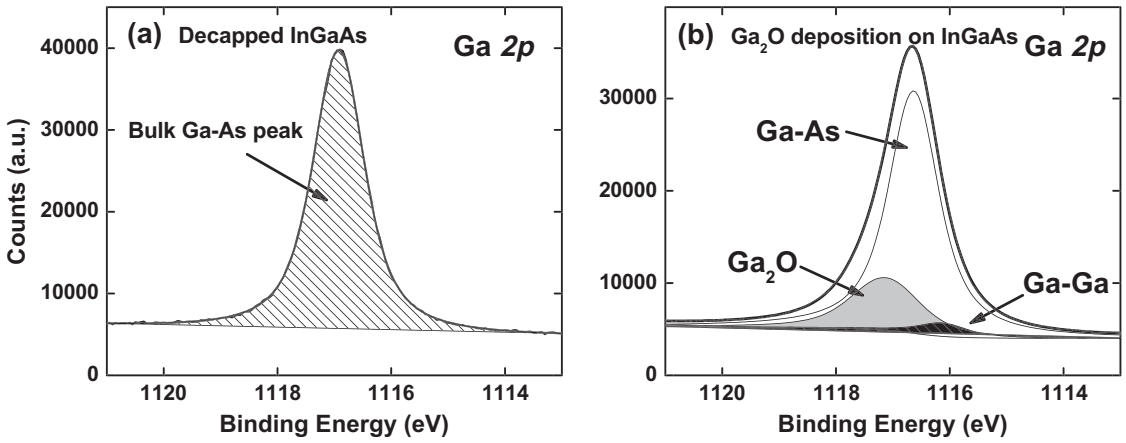

Fig. 6. (a) Ga 2*p* XPS spectrum for an As capped $In_{0.53}Ga_{0.47}As$ substrate following thermal desorption of the As cap. An oxygen and carbon free surface is produced allowing precise measurement of the position (1116.7 eV) and FWHM of the bulk peak. All XPS fits included a Shirley background subtraction. (b) Ga 2*p* XPS spectrum of an $In_{0.53}Ga_{0.47}As$ substrate following decapping and Ga_2O deposition. Ref. [36]. Reprinted with permission, © 2009, The Electrochemical Society.

mental considerations. Such *ex situ* studies are common in conjunction with PES, as the dedicated beamline endstations with extensive *in situ* growth capabilities are sparse, and beam time constraints limit the ability to perform studies lasting many days or weeks on a single sample. However, the unambiguous identification of these bonding states is crucial in terms of the relation to potential defects at the interface with the III–V semiconductor. Therefore *in situ* laboratory-based XPS and *ex situ* synchrotron-based PES may be seen as having a strong complementary relationship in the study of this materials system.

As seen in Fig. 6a, *in situ* analysis of a thermally decapped InGaAs surface can provide a model binding energy reference (i.e. chemical state) and an associated linewidth for the Ga 2*p* spectra of the Ga–As bond unperturbed by spurious chemical contaminants. Analysis of other relevant photoelectron regions for this sample (*viz.* As, In, O, C – not shown) indicate that no oxidized species or spurious C is detected [36]. Similar results are obtained for hydrogen-cleaned or decapped GaAs surfaces as well.

Subsequent *in situ* room temperature exposure of the decapped InGaAs surface to a flux of molecular Ga_2O (Fig. 6b) from a Ga_2O_3 powder charge in an Ir effusion cell source [47–49] results in a photoelectron feature which is asymmetric and measurably broader than that for the freshly decapped surface. Moreover, only a small concomitant O 1*s* feature was detected from this sample and no As–O bonding or spurious C was detected (not shown). Utilizing the spectra for the freshly decapped surface as a model for the unperturbed Ga lineshape, the associated spectral fit was then applied to the Ga_2O-exposed surface spectra, and it was determined that a minimum of two additional spectral features were required to fit the raw data with similar precision. The feature appearing at 0.55 eV above the bulk peak is therefore attributed to the Ga 1+ oxidation state, originating from Ga_2O present on the surface, while a barely detectable feature at ~1116.1 eV is attributed to Ga–Ga bonding originating from the powder (rather than polycrystalline) source used in this experiment. Again, similar results are obtained for GaAs as well.

As noted above, higher oxidation states are seen on $In_xGa_{(1-x)}As$ surfaces as well. Ga–O bonds are known to exist in chemical states that manifest themselves with binding energies around 1–2 eV above the bulk Ga–As peak. Chemically treating a native oxide with NH_4OH leaves a surface oxide that exhibits a large shoulder on the high binding energy side of the bulk peak. The accurate analysis of this spectrum requires two oxidation states of Ga, the Ga 1+ oxidation state (Ga_2O) and the Ga 3+ oxidation state (Ga_2O_3) as shown in Fig. 7. Using the previously determined parameters for the bulk peak and the Ga_2O surface oxide, the peak position for the Ga 3+ oxidation state is determined and is found to be 1.2 eV above the bulk peak, precisely where photoelectron studies of Ga_2O_3 powders place it [32]. There is also a higher binding energy state that is sometimes seen in the Ga 2*p* spectra which arises at 1.6 eV above the bulk peak and is seen only on samples with relatively thick oxides. Possible identities for this oxidation state include $GaAsO_4$, $Ga(AsO_3)_3$ as well as $Ga(OH)_3$ [32]. This state is removed easily with chemical treatment.

Deconvolution of the spectra after careful analysis of a number of *in situ* and *ex situ* surface preparations suggests that Ga-suboxides (Ga 1+:Ga_2O) are likely stable on *all* substrates that have had any exposure to oxygen, hydroxyls, etc. despite its relatively high (less stable) Gibbs free energy. For example, the HF-last GaAs surface has residual Ga oxides on the surface, mainly Ga 3+ and Ga 1+ (Fig. 7). These states were deconvoluted using the control sample procedure outlined above. The suboxides are found specifically at the substrate interface [35] suggesting that the formation energies in this regime are not governed by bulk oxide values for up to one monolayer but rather are perturbed due to the other elements nearby. Such suboxide species have been previously identified as crucial for low defect densities in MBE-grown dielectrics on GaAs

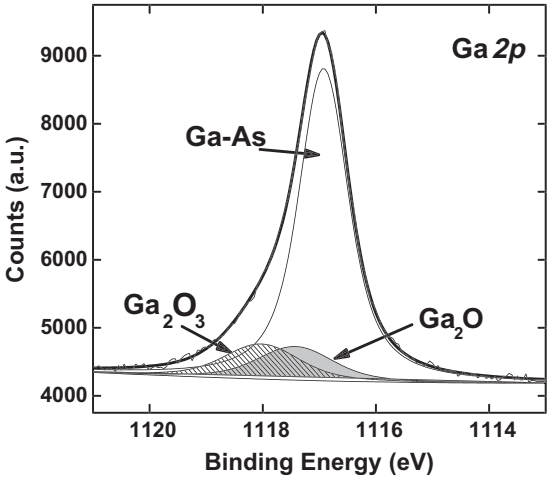

Fig. 7. XPS core-level spectrum showing the two interfacial oxidation states of Ga. The suboxide is present for any surface exposed to oxygen or hydroxyls. See [4,35,36].

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Table 2
ALD precursors and oxidizers studied on $In_xGa_{(1-x)}As$ surfaces. ^{i}Pr = isopropyl, fmd = formidinate.

Dielectric/substrate	Precursor	Vapor pressure [200]			Oxidizer/nitridizer	T_{dep} (°C)	T_{max} (°C)	Ref.
		20 °C	100 °C	200 °C				
Al_2O_3/*n*-GaAs	$Al(CH_3)_3$ [TMA]	8.6	315	–	H_2O	300	600 O_2	[102,103]
Al_2O_3/*n*-InGaAs	$Al(CH_3)_3$ [TMA]	8.6	315	–	H_2O	300	550 O_2	[201]
Al_2O_3/*p*-GaAs	Al(CH3)3 [TMA]	8.6	315	–	$(CH_3)_2CHOH$	400	–	[207]
AlN/*n*-, *p*-InGaAs	$Al(N(CH_3)_2)_3$ [TDMA-Al]				NH_3	250	550 N_2	[202]
HfO2/*p*-InGaAs	$HfCl_4$	10^{-6}	0.006	5.1	H_2O	320	500 O_2, N_2	[203]
HfO_2/*n*-InGaAs	$Hf(NCH_3C_2H_5)_4$ [TEMA-Hf]	0.005	1.7	155	H_2O	200	–	[138]
HfO_2/*n*-, *p*-GaAs	$Hf(N(CH_3)_2)_4$ [TDMA-Hf]	0.06	15	1074	H_2O	200	500 N_2	[204]
Hf-aluminate/*n*-, *p*-GaAs	$Al(CH_3)_3$	8.6	315	–	H_2O	300	600 N_2	[205,206]
	$HfCl_4$	10^{-6}	0.006	5.1				
La-aluminate/*n*-InGaAs	$Al(CH_3)_3$	8.6	315	–	H_2O	200	–	[101]
	$La(^{i}PrNCHN^{i}Pr)_3$ [($^{i}Pr_2$-fmd)3-La]	0.008	0.06	0.256				

using scanning tunneling microscopy (STM) methods [47,50], but have been difficult to measure conclusively using complementary characterization methods conducted under *ex situ* conditions such as high-resolution transmission electron microscopy [49,51], high-resolution electron energy loss spectroscopy [52,53] or XPS [54]. These oxidation states play a critical role in device characteristics as is presented in detail in a later section [35,40].

2. Oxide deposition on InGaAs substrates by ALD[1]

2.1. Preparation of III–V substrate surfaces

It is well known that surface preparation [55] (sometimes also described as "passivation" in the context of device technologies) of any substrate affects the subsequent ALD process for dielectric deposition. A number of surface treatments have been examined on III–V (1 0 0) surfaces (GaAs, in particular), and are now under examination for dielectrics deposited by ALD. Previous (typically wet) chemical surface preparation studies include the effects of chalcogenides [56] e.g. sulfur: $(NH_4)_2S_x$ solutions [57–60], Na_2S solutions [61,62], H_2SO_4 solutions [63], H_2S/S_2 exposures [64], selenium [65], and tellurium [66], HCl solutions [67,68], HF solutions [44,69], hydroxide solutions [43,70,71], as well as combinations of these [72,73]. Alternative treatments (typically performed in vacuum) include vacuum annealing [74], As-flux passivation (capping) and desorption (de-capping) [75], hydrogen plasmas [76,15], atomic (thermally dissociated) hydrogen [77,78], as well as the deposition of overlayers such as silicon and germanium on the III–V surface [79–85].

At this time, systematic surface preparation studies on $In_xGa_{1-x}As$ are relatively less complete, and thus the subject of current research. Many of these investigations utilize similar surface treatments to that employed for GaAs surfaces. The addition of In generally results in the formation of In-oxides on the surface, with a formation energy reported to be intermediate to that of AsO_x and GaO_x [32]. Thus thin native oxides on this surface generally exhibit oxides associated with all three of the constituent elements, and so similar oxide-etch chemistries may be anticipated. However, relative to GaAs, the details on the surface preparation of InGaAs are less established, and so various surface preparation methods are currently under investigation on this surface including wet chemical approaches [86,87], thermal vacuum annealing [29], As-capping and decapping [88], exposure to H-plasmas [87,89,90] and thermally-cracked atomic H [28], as well as exposure to molecular species including $As[N(CH_3)_2]_3$ [91], and H_2S [92].

[1] Portions of this section have been previously published in [3].

2.2. Atomic layer deposition (ALD) on InGaAs substrate surfaces

The ALD process parameters (reactant delivery and deposition temperatures, purge and exposure times, etc.) are frequently decided by the precursor characteristics, such as vapor pressure, decomposition behavior, sticking coefficient and reaction chemistry. The ALD deposition process should not cause unintentional thermal instability of III–V substrates. Elemental As desorption occurs from GaAs surfaces [93] in vacuum at $T > 400$ °C and from $T > 300$ °C for InAs [94]. In segregation at the surface has been reported at 480 °C for InGaAs [95]. Metal precursors utilized on III–V surfaces can be divided into two main groups: metalorganic and inorganic precursors. Halide precursors, such as $HfCl_4$, are the most common inorganic precursors used for CVD and ALD applications. They are typically highly reactive and thermally stable (up to 750 °C). However halides are typically solid phase with relatively low volatility (except $TiCl_4$). HfO_2 films grown by ALD using $HfCl_4$ and water below 300–350 °C were reported to have high residual chlorine and hydrogen content (2–5 at.%) [96]. Alkyls, such as trimethyl-aluminum (TMA), are ideal metalorganic precursors containing direct bonding between the metal ion and carbon, while alkoxides and amides have oxygen and nitrogen bonding between the metal and alkyl groups, respectively. They are highly volatile and very reactive with water through hydrolysis. On the other hand, they often decompose at a relatively low temperature. For example, both TMA and Tetrakis(ethylmethylamido)hafnium (TEMA-Hf) decompose at temperatures higher than 275 °C [97,98]. The chelation of C (β-diketonates), O (cyclopentadienyls) and N (amidinates) with alkyls to a metal enhances thermal stability compared to single bond precursors, while they frequently have low vapor pressures at deposition temperatures due to their bulky ligands.

Water is the most commonly used oxygen source providing an hydroxyl terminated surface in metal oxide ALD. Water frequently needs a long purge time due to its sticking coefficient with surfaces, while an alternative oxidizer, e.g. ozone, is easily purged out of the chamber and it potentially improves the throughput of an ALD process. It was also reported that an ozone process with Tetrakis(dimethylamino)hafnium (TDMA-Hf) at 300 °C on Si enhances electrical characteristics of HfO_2 films and reduces C contamination in the films as well [204]. However, there are potential concerns on O_3 with III–V substrates regarding undesirable interface oxide formation due to its strong oxidation reaction and possible residual carbonate formation at low temperature [141].

A number of precursors have been reported for ALD deposition of dielectrics on III–V surfaces. Representative examples, typically the first published reports, are summarized in Table 2 with the associated dielectric produced, precursors reported to date, oxidiz-

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ing agent, deposition temperature (T_{dep}), and maximum post-deposition temperature (T_{max}) and annealing ambient.

As of this writing (late-2010), Al_2O_3, HfO_2 and their alloys constitute the majority of reports for ALD on III–V substrates. Given the available precursors developed, additional ALD metal oxides will likely be evaluated for gate dielectrics of III–V substrates soon. Particularly, the recent development of amidinates and cyclopentadienyls precursors enables La_2O_3, Lu_2O_3, Gd_2O_3 and their nanolaminate oxides using ALD [99–101].

2.2.1. ALD on GaAs

The first reported depletion mode MOSFET work utilizing ALD dielectrics directly on GaAs(1 0 0) is by Ye and coworkers [102,103] with 8–16 nm thick Al_2O_3. The TMA/water chemistry utilized to obtain the Al_2O_3 layer was conducted on a GaAs surface exposed to the laboratory ambient after MBE growth, thus initially having a thin native oxide layer (likely with spurious organic contamination from the air exposure) consisting of Ga- and As-oxides. It was noted in this work that the ALD process removes the native oxide and excess As on the GaAs surface, resulting in a ~0.6 nm Ga-oxide interfacial layer. Capacitor measurements indicated interface state densities $D_{it} \sim 10^{12}/cm^2$ eV for this gate stack, which should be compared to the benchmark stack for GaAs: $Gd_2O_3/Ga_2O_3/GaAs$ grown by molecular beam epitaxy (MBE) methods which yields $D_{it} \sim 5 \times 10^{10}/cm^2$ eV [104].

A subsequent more detailed study by Frank et al., examining HfO_2 as well as Al_2O_3 deposition by ALD, indicated that the surface oxides are indeed affected by the ALD process [105]. A small reduction of the GaAs surface native oxide content was reported for "vacuum pre-annealing" (i.e. annealing at 300 °C prior to ALD deposition) indicating that little native oxide "thinning" from such annealing was detected from *ex situ* analysis, consistent with prior reports. A native oxide thickness of ~2.5 nm was reported for the GaAs surface. In the case of TMA/water chemistry ALD at 300 °C, an amorphous, 4 nm Al_2O_3 layer was observed from deposition on either the native oxide or an HF-last surface. An interfacial layer, reported to contain significant Ga_2O content, was observed to be ~1 nm thick for the Al_2O_3 deposition, while a thicker interfacial layer (~2–2.5 nm) was observed from the HfO_2 deposition using a $HfCl_4$/water chemistry ALD. These investigators note a relatively thinner interfacial layer from the Al_2O_3 deposition suggests that volatile interfacial layer products may be formed or conversion of interfacial oxides to Al_2O_3 occurs during the ALD process. The difference in the behavior of the ALD precursors was attributed to the enhanced reactivity of $Al(CH_3)_3$ compared to $HfCl_4$ based upon formation enthalpies.

This "self cleaning" interfacial oxide reaction has been subsequently observed by others on GaAs [105–108]. Dalapati and coworkers also examined capacitors using Al_2O_3 (TMA/water), HfO_2 ($HfCl_4$/water) and nanolaminated mixtures by ALD on HCl + $(NH_4)_2S$ treated GaAs(1 0 0) surfaces [105]. The capacitance–voltage (*C–V*) behavior was studied at room temperature, demonstrating higher frequency dispersion for capacitors on *n*-GaAs vs. *p*-GaAs, consistent with reports published nearly 30 years ago on anodic native oxides [6,109]. Generally, the maximum capacitance ("C_{ox}") observed in a *C–V* measurement is observed to decrease as the measurement frequency is increased. Such behavior has also been more recently observed by others as well utilizing PVD [24] and ALD [34,110] dielectrics, and the utilization of Si (or Ge) interfacial "passivation" layers noted above, and/or post-deposition annealing, reduces the observed dispersion behavior on GaAs [111]. This is discussed further in Section 3.1.

Dalapati et al. [105], also examined the chemical nature of the interface using *ex situ* X-ray photoelectron spectroscopy in conjunction with thin (~1.5 nm) Al_2O_3, HfO_2 and Al_2O_3/HfO_2 ("HfAlO") nanolaminates. It was found that Ga- and As-oxides were detected at the interface, and the *C–V* behavior for all three stacks investigated was attributed to the interfacial oxide layer, with HfAlO exhibiting the better behavior and a thinner interfacial layer for *p*-GaAs substrates. In the case of *n*-GaAs substrates, they report that interfacial oxidation is relatively suppressed for all dielectrics investigated, with the interfacial layer associated with the HfAlO stack essentially indistinguishable from the *p*-GaAs case. Taken together, the results suggest a dopant-dependent oxidation process [112,113] in conjunction with the ALD chemistry employed [106]. However, as noted previously, recent studies of chemically identical oxides on *n*-GaAs and *p*-GaAs, followed by Al_2O_3 deposition by ALD, suggests that the difference in *C–V* behavior stems from the differences in the capture time constants for electrons and holes rather than any dopant-dependent interface state effects [46].

However, there can be significant differences in the chemical species identified at the GaAs interface by XPS dependent upon the surface preparation or whether the interface studies are conducted *ex situ* or *in situ*. As can be seen in Fig. 8, *in situ* studies of surface native oxides after subsequent ALD processing indicate that such oxides can be actually reduced *below* the limit of XPS detection by the ALD process depending upon the oxidation state/precursor combination employed [45]. The results are even more dramatic for surfaces chemically treated prior to ALD, where the weaker bonded, higher-oxidation states are initially removed completely by wet cleans (e.g., NH_4OH shown in Fig. 8). In contrast, previous literature also indicates that surface oxide species remain after ALD [105,114,115].

This apparent discrepancy in the literature is not surprising as the thin films required for typical XPS analysis must be photoelectron transparent (⩽6 nm). As discussed above, the photoelectron kinetic energy associated with the features (e.g. 3*d* or 3*p* lines) of interest using laboratory X-ray sources are ~1480 eV or much less [41]. Thus very thin films and the interfaces will likely oxidize upon extended exposure to the ambient prior to *ex situ* surface analysis, thus resulting in oxidized interfacial species not *a priori* associated with dielectric growth process itself. However, such results indicate that considerable caution must be exercised when drawing conclusions on correlations of physical characterization results to those obtained electrically such as *C–V* curves. Device processing often entails steps which result in exposure of the gate stack to the cleanroom ambient, and thus *ex situ* studies certainly have relevance in this context. In contrast, *in situ* studies enable a better understanding of the film interface behavior during growth and the impact of controlled oxidation on electrical performance where the devices are constructed under carefully controlled conditions to limit spurious interfacial oxidation.

The data [45] presented in Fig. 8 indicates a reaction mechanism that is consistent with a ligand exchange process [115], whereby Al from the TMA preferentially reacts with the As^{3+} and Ga^{3+} oxidation states, resulting in bond conversion to Al-oxide. In contrast, the reaction with the 3+ oxidation state is less efficient for Hf originating from the TEMA-Hf precursor, yet effective for the 5+ state and indicative of a more complex process. In either case, it is evident that the weakly bonded oxides may be reduced from the ALD process, with the stronger Ga–O bonding, including potential Ga sub-oxide species, remaining at the interface. It therefore seems possible to control a significant portion of the interfacial oxidation through such precursor-mediated reactions, and thus impact detrimental electrical behavior from defects induced by uncontrolled oxidation such as Fermi level pinning and *C–V* frequency dispersion [40,116]. Recently, the use of isopropanol as an oxidizer has been investigated in this context as well for Al_2O_3 deposition [207].

Careful inspection of the Ga–O feature binding energy in the Ga 2*p* spectra shown in Fig. 8 indicates that a general shift *toward* the bulk Ga–As peak is observed upon ALD film growth. Such chemical

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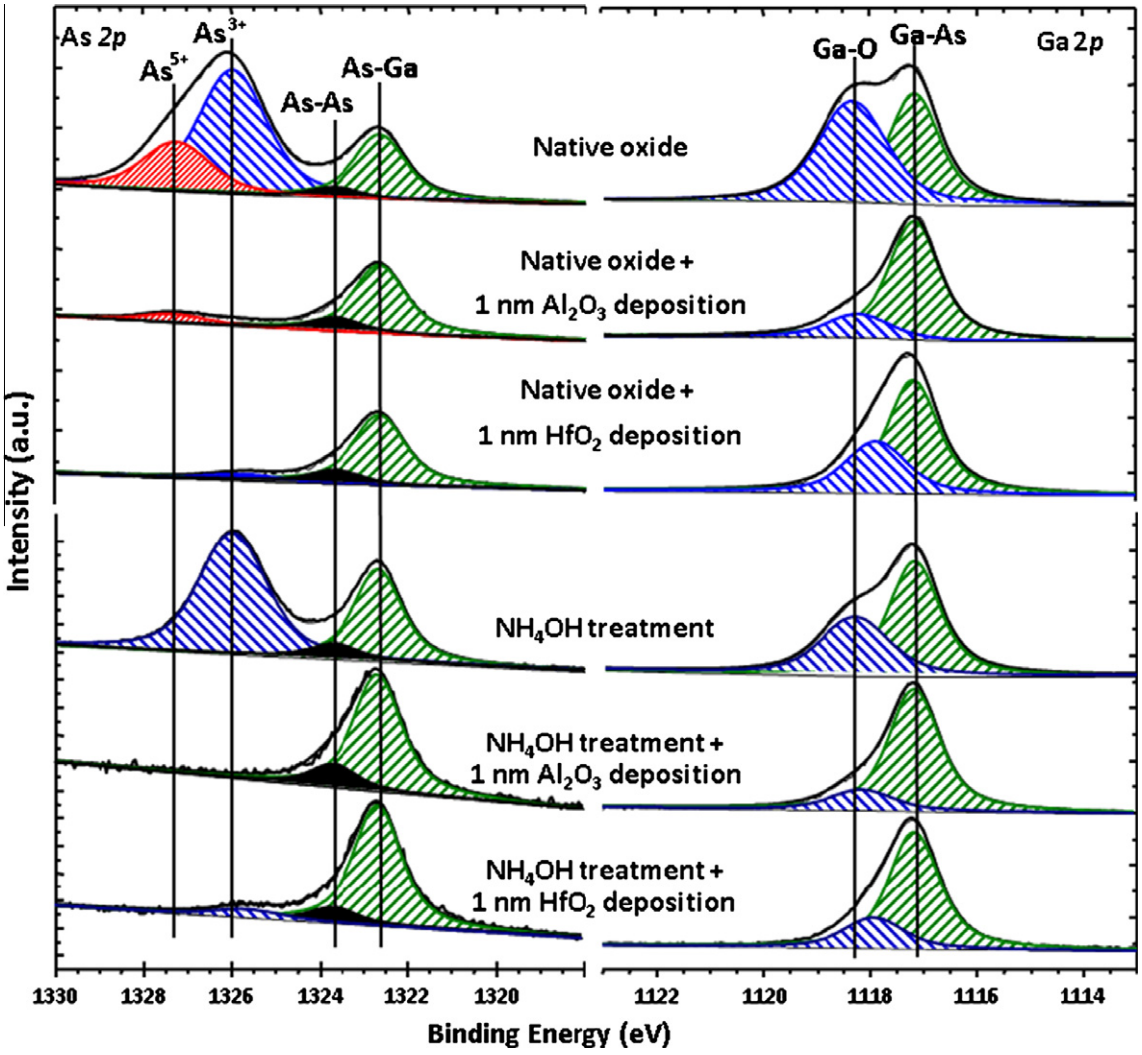

Fig. 8. X-ray photoelectron spectroscopy of the interfacial reactions after atomic layer deposition of Al_2O_3 and HfO_2. The reactions with the surface oxides exhibit precursor specific and oxidation state-specific behavior [140]. Reprinted with permission, © 2009 Elsevier.

shifts may be consistent with M–O–Ga bonding (where M = Al or Hf), the presence of Ga sub-oxides species (such as O–Ga–O; Ga 1+) in addition to Ga 3+(*viz.* Ga_2O_3), as well as band bending effects [46,73].

2.2.2. ALD on InGaAs

The higher bulk mobility and potentially more favorable surface passivation behavior [30] associated with $In_xGa_{1-x}As$ alloys has stimulated recent research on MOSFETs with ALD dielectrics as well. A number of Al_2O_3 ALD studies, most emphasizing device characteristics, have been conducted with various In content including $x = 15\%$ In [105,117], 20% In [100,118–120], 53% In [121,122], 65% In [123], and 100% In [124–126]. Other high-*k* dielectrics deposited by ALD including HfO_2 [101,102,127,128], ZrO_2 [129,130], Hf-aluminates [131,132], and La-aluminates [101,133] have also been recently examined on InGaAs. The interest in aluminates [134,135] stems from a potentially higher gate dielectric permittivity with a minimal (low-k) interfacial layer – an essential aspect when device scaling is taken into account [2,136].

For ALD on $In_{0.2}Ga_{0.8}As$, both "self cleaning" [137–139] and pre-deposition annealing [120] have been recently examined in view of the desire to control interfacial oxidation. Fig. 9 demonstrates, from *in situ* half-cycle ALD studies, that the reaction with the *initial* TMA pulse at 300 °C results in most of the oxide reduction on the $(NH_4)_2S$-treated *n*-$In_{0.2}Ga_{0.8}As$ surface [139,140]. In addition to the suppression of the 3+ oxidation state consistent with a ligand exchange mechanism, it is also seen that As–S bonding is rendered below the limit of detection by this reaction, while Ga–S (and possibly Ga-suboxide) remains throughout the growth process of the resultant 1 nm Al_2O_3 film. Further reduction of the residual oxides and As–As bonding has been recently reported by vacuum annealing chemically treated n- and p-$In_{0.2}Ga_{0.8}As$ surfaces to 380–390 °C *prior* to initiating ALD deposition [28,120]. Exposure of the dielectric stack to forming gas (N_2:H_2) anneals at 450 °C results in the reduction of hydroxyls and a concomitant negative flatband voltage shift [120]. The effect of ozone as an oxidant has also been recently examined, where extensive oxidation is observed [141].

From a surface/interface chemistry perspective, the $In_{0.53}Ga_{0.47}As$ surface (on InP substrates) appears to be among the most studied, and is particularly interesting from a potential transistor performance point of view. Chang et al. examined HfO_2 on this surface produced from TEMA-Hf/H_2O ALD at 200 °C using synchrotron angle-resolved XPS [127]. They report that no detectable In, Ga, nor As species is seen within the HfO_2 film, and that only Ga_2O_3, In_2O_3, and $In(OH)_3$ are detected at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. A conduction-band offset of $\Delta E_C = 1.8 \pm 0.1$ eV and a valence-band offset of $\Delta E_V = 2.9 \pm 0.1$ eV were determined in this work, and a large midgap interface state density $D_{it} \approx 1 \times 10^{12}$ cm^{-2} eV^{-1} was deduced and attributed to the presence of the interfacial oxides.

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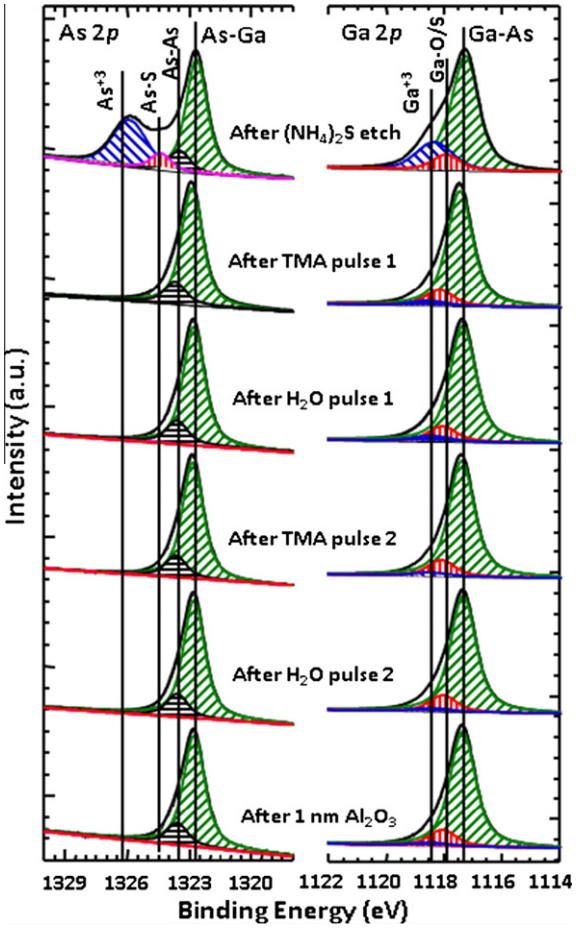

Fig. 9. *In situ* X-ray photoelectron spectroscopy analysis of atomic layer deposition half-cycle reactions for Al_2O_3 on $In_{0.2}Ga_{0.8}As$. TMA, trimethyl-aluminum. From [139]. Reprinted with permission. © 2008, American Institute of Physics.

Lee et al. examined the effects of air-exposure after MBE growth of $In_{0.53}Ga_{0.47}As$/InP and ALD deposited HfO_2 [128]. It was found that limiting exposure to air to 10 min. results in thinner In- and Ga-oxides, while As-oxide was below the limit of detection by XPS. A similar $D_{it} \approx 1 \times 10^{12}\ cm^{-2}\ eV^{-1}$ was deduced from capacitor measurements, and capacitance equivalent oxide thickness (CET) of 1 nm was reported. In contrast, Oh et al. [132], reported that MOCVD studies of HfO_2 films on $In_{0.53}Ga_{0.47}As$ results in no detectable interfacial oxides and cite the deposition approach as a potential cause. A comparison to MOCVD Hf-aluminate formation on this surface also indicated a lower interface state density ($\sim 5 \times 10^{11}/cm^2\ eV$) without detectable interfacial oxides compared to the HfO_2 case ($\sim 9 \times 10^{12}/cm^2\ eV$). Similar band offsets were reported for the $HfO_2/In_{0.53}Ga_{0.47}As$ interface, while $\Delta E_C = 2.4 \pm 0.1$ eV and $\Delta E_V = 3.3 \pm 0.1$ eV for the $HfAlO_x/In_{0.53}Ga_{0.47}As$ interface. Shahrjerdi et al. [202], examined $HfO_2/AlN/In_{0.53}Ga_{0.47}As$ where small, but detectable, As-oxides were observed, in conjunction with Ga- and In-oxides as well. A high $D_{it} \approx 8 \times 10^{12}/cm^2\ eV$ was also deduced from the capacitors fabricated, and the self-aligned transistors fabricated indicated room for further optimization. Taken together these reports suggest that even small amounts of detectable surface oxides results in a significant interface state density.

Control of the interfacial oxides on $In_{0.53}Ga_{0.47}As$ upon gate stack formation has been recently explored along two avenues: precursor selection and interfacial Si layers. Xuan et al. have examined transistor performance using ALD Al_2O_3 directly on $In_{0.53}Ga_{0.47}As$ reporting $D_{it} \sim 10^{12}/cm^2\ eV$ and corrected mobilities as high as $2200\ cm^2/Vs$ [131]. Recent work on La-aluminate deposition by ALD on $In_{0.2}Ga_{0.8}As$ using tris(*N*–*N*′-diisopropylformamidinato)La indicates that formation of higher oxidation states may be controlled effectively through the ligand-exchange reaction mechanism [6]. Only suboxides of Ga were detected in these films. Alternatively, the use of a thin Si layer has been shown to react with $In_xGa_{1-x}As$ surface oxides, as well as subsequent dielectrics deposited by PVD [142] and ALD [40] methods. Essentially, the Si film serves as a "getter" layer for relatively weaker bound surface oxides resulting in more stable SiO_x bond formation. The effect of employing Si interfacial layers is explicitly discussed in the next section.

Scaling of surface channel transistors beyond the 16 nm node (~2020) will necessarily require a suitable high-k dielectric with an equivalent SiO_2 thickness below 1.0 nm which discourages thick low-k interface layers, and so the precursor reaction chemistry route to controlling interfacial defects and their resultant trap states will likely be pursued vigorously. It should also be noted that alternative device architectures, which rely on buried channels for example, are also under investigation [143]. In general, the performance of all III–V field effect transistor architectures to date have yet to be scaled to establish the performance at the 16 nm node and, although buried channel high electron mobility transistors (HEMT) are making significant strides [144], several challenges remain for this technology to be widely adopted for high performance scaled logic applications.

2.2.3. ALD on InAs

Work has been recently completed on the *in situ* examination of ALD Al_2O_3 deposition on InAs(1 0 0) [125]. ALD growth on surfaces prepared with NH_4OH and $(NH_4)_2S$ treatments were examined.

Fig. 10 shows the As $2p_{3/2}$ regions after the initial surface preparation, exposure to the ALD reactor at 300 °C in vacuum, as well as subsequent half-cycle precursor exposures. It is seen that the As-oxide concentration is minimized for the S-treated surfaces relative to that obtained from the hydroxide treatment. Exposure to the ALD reactor ambient (7 Torr, 30 min at 300 °C) results in further reduction of As-oxides for the S-treated surface. In contrast, substantial As 3+ species remain on the surface for the hydroxide-treated surface. This result demonstrates that thermal reduction of such As-oxides under these conditions is dependent upon the initial surface oxide concentration. It is also noted that As–S bonding is reduced below detectable limits with such heating. Subsequent exposure to TMA and water cycles results in no detectable As-oxide formation for the S-passivated InAs, while the detected As 3+ state is reduced after TMA exposure for the hydroxide-treated InAs, similar to that observed previously for GaAs and InGaAs. It is noted that As–As bonding appears to persist throughout the process at levels just above the detection limit.

Fig. 11 shows the corresponding In $3d_{5/2}$ regions. The initial surface appears to have substantially reduced In 3+ oxides for the S-treated surface and the In 1+ and In–S bonds are not distinguishable within the available energy resolution. As all of the S originates from the chemical treatment, the increase of the feature intensity at ~444.3 eV after the 300 °C vacuum exposure is likely a result of In 1+ formation (In_2O). An analogous feature is seen in the hydroxide-treated spectra, which is S-free. Upon exposure to TMA/water cycles, the In 3+ is clearly reduced for both InAs samples, while the In 1+ state persists. The impact of the presence of this chemical state at the interface on the electrical properties has yet to be determined, particularly in view of the prior work correlating Ga oxidation states and electrical behavior described below. The chemical state assignments above appear to be in reasonable agreement with recent synchrotron studies as well [126].

STM studies of In_2O deposition on GaAs(1 0 0) results in this species bonding in the trough areas or insertion into As-dimers

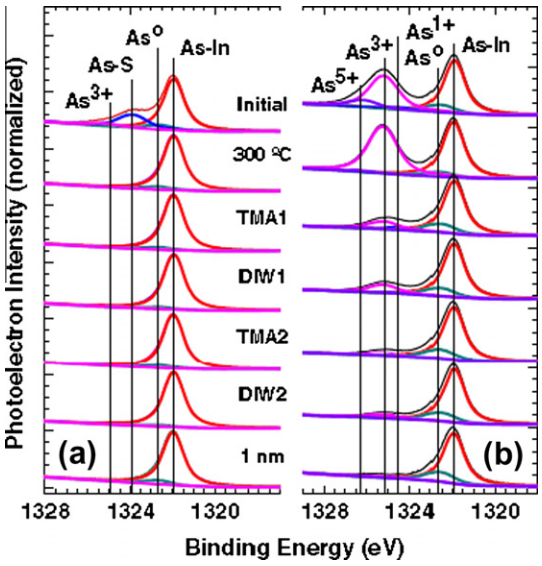

Fig. 10. In $3d_{5/2}$ region region for ALD/XPS half-cycle studies on (a) S-passivated InAs and (b) NH_4OH-etched InAs(1 0 0) [125]. Reprinted with permission, © 2010, American Institute of Physics.

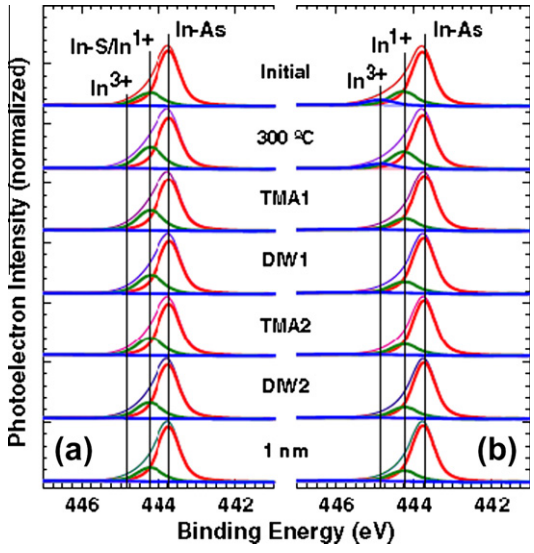

Fig. 11. As $2p_{3/2}$ region region for ALD/XPS half-cycle studies on (a) S-passivated InAs and (b) NH_4OH-etched InAs(1 0 0) [125]. Reprinted with permission, © 2010, American Institute of Physics.

[116]. More recent work has investigated In_2O adsorption on InAs(1 0 0) using STM [145]. The effects of annealing a S-treated InAs(1 0 0) surface above 300 °C has also been investigated recently for doping [146].

It should be noted that these TMA on InGaAs and InAs studies were performed on surfaces that show a mixed As-rich(2×4)/Group III-rich(4×2) surface reconstruction. As will be described in the next section, oxidation induced disorder plays a profound role in the transport properties of InGaAs-based devices fabricated from starting surfaces similar to those just described. Recent STM studies have demonstrated no surface disorder following TMA dosing on fully Group III-rich(4×2) reconstructions (see [208] discussed below). It may thus be possible that, through the appropriate choice of surface reconstruction followed by controlled precursor chemistry, this disorder may be reduced – at least on the basis of UHV studies.

3. Electrical behavior of oxides on III–V and interfacial chemistry

For over 30 years, there has been a significant effort on development of MOS devices with various oxides on compound semiconductors. The electrical behavior of these MOS devices intimately depends on details of processing conditions (e.g. substrate type, surface preparation, dielectric deposition technique, post-deposition anneal). Therefore, it is impossible to review in a cohesive manner all of the literature available regarding the electrical behavior of oxides on III–V semiconductors. Instead, the intent of this section is to describe a few salient features of the electrical behavior of oxides on III–V semiconductors with respect to interfacial chemistry and that will be critical for the ongoing development of $In_xGa_{1-x}As$ MOSFETs.

3.1. C–V measurements and issues

Capacitance–voltage (*C–V*) measurements are a staple in the traditional characterization of MOS devices and materials [147]. However, application of the technique to III–V systems requires considerable care, as described extensively by Passlack [148,149] and Martens, Brammertz et al. [150–154]. In this section, the issues associated with electrical measurements obtained are discussed in view of the interfacial chemistry described in previous sections.

3.1.1. Frequency dispersion

One of the commonly observed anomalous phenomena is that of strong frequency dispersion of the *C–V* characteristics in maximum capacitance as shown in Fig. 12. In this case, both *n*-type ($2–4 \times 10^{17}$ cm^{-3} Si doped) and *p*-type ($2–4 \times 10^{17}$ cm^{-3} Zn doped) GaAs substrates received a standard degrease (acetone, methanol and IPA for 1 min each) followed by cleaning in 29% NH_4OH for 3 min. A 10 nm Al_2O_3 film was deposited using a Cambridge Nanotech Savannah-100 ALD chamber using TMA and H_2O at 300 °C as the gate oxide. A post deposition anneal (PDA) was performed at 600 °C in N_2 for 60 s. TaN (150 nm) was RF sputtered through a shadow mask as the gate metal to form MOS capacitors. An electron-beam evaporated Ni/Au/Ge alloy annealed at 425 °C was used as a back side Ohmic contact. The frequency dispersion of maximum capacitance is more prominent in *n*-type GaAs compared to *p*-type GaAs MOS capacitors. This behavior has been observed on numerous III–V semiconductors [117,155,156]. For $In_xGa_{1-x}As$, the effect is primarily observed for low Indium concentration and is typically not observed for $x = 0.53$ and above.

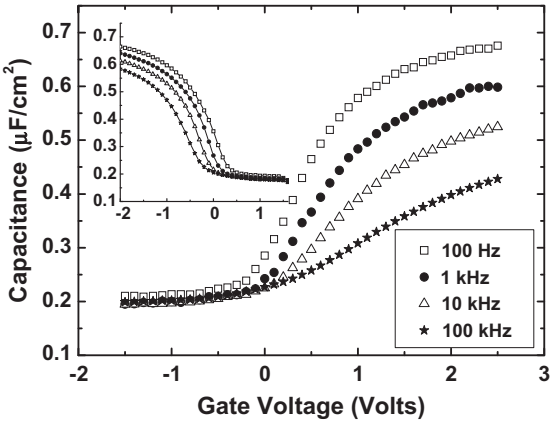

Fig. 12. Commonly observed frequency dispersion in accumulation for TaN/Al_2O_3 stack on both n- and *p*-type (inset) GaAs MOS capacitor structures. The capacitor area is 7.85×10^{-5} cm^2.

One of the possible causes for frequency dispersion in maximum capacitance is that of series resistance (contact, substrate, cabling) altering the measured C–V [157]. However, there are several reasons that series resistance cannot explain the dispersion behavior observed here. Given device capacitance (C_c), parallel conductance (G_c) and series resistance (R_s), the measured capacitance (C_m) has the following dependence with measurement frequency (ω)

$$C_m = \frac{C_c}{(G_c R_s + 1)^2 + \omega^2 (C_c R_s)^2}. \quad (1)$$

Frequency dispersion due to series resistance depends on ω^{-2} which is not observed in the measured results. To provide an independent measure of series resistance, the gate dielectric of the MOS capacitor was broken down by going to extremely high positive bias. The series resistance was measured to be approximately 20 Ω. This value is consistent with separate measurements of resistivity of the TaN, resistivity of the GaAs, and contact resistance measurements of the AuGeNi backside contact. Using this value of series resistance, a parallel conductance (obtained from the derivative of the tunneling current–voltage characteristic) and a reasonable estimate for the C_c–V_g relationship, no dispersion is obtained in modeled C_m–V_g behavior for a frequency of 1 MHz. Therefore, series resistance cannot explain the observed dispersion.

Previous researchers have ascribed this anomalous dispersion behavior to a high density of interface states and associated Fermi level pinning [24,117,156,158,159,163,164]. Fig. 13 shows modeled n-GaAs C–V characteristics including classical interface state capacitance with an extremely high interface state density of 1×10^{13} cm^{-2} eV^{-1} uniformly distributed in energy. C–V characteristics were simulated using a classical model of the total semiconductor charge [160]. Using the surface potential from this solution, the frequency dependent capacitance associated with interfacial defects (C_{it}), averaged over band bending, and for a p-type substrate, was calculated numerically using the traditional approach [147]

$$C_{it} = \frac{qD_{it}(2\pi\sigma_s^2)^{-1/2}}{2\omega\tau_p} \int_{-\infty}^{\infty} \exp\left(\frac{-\upsilon^2}{2\sigma_s^2}\right) \exp(-\upsilon) \tan^{-1}(2\omega\tau_p \times \exp(\upsilon)) d\upsilon \quad (2)$$

$$\text{with } \tau_p = \frac{1}{\bar{v}\sigma_p p_s} \quad (3)$$

where σ_s^2 is the variance of band bending in units of kT/q, ω is the measurement frequency in radians, τ_p is the characteristic capture time constant for holes, υ is band bending, $\bar{v}$ is the thermal velocity of the carriers (typically 10^7 cm/s in silicon at room temperature), σ_p is the capture cross-section for holes, and p_s is the density of free holes at the substrate surface. The total capacitance for the MOS capacitor (C_{tot}) at a given gate voltage (V_g) is then calculated using

$$C_{tot} = ((C_{it} + C_{sub})^{-1} + C_{ox}^{-1})^{-1}. \quad (4)$$

The results show a frequency-dependent kink in the depletion portion of the curve similar to that of silicon but quite different than the measured GaAs behavior. In accumulation, the free electron density (n_s) at the semiconductor surface is large which implies that the trapping time constant given by Eq. (3) will be very small. Therefore, all of the interface states can respond to the frequencies of interest, and C_{it} is approximately equal to qD_{it}. In strong depletion, n_s is very small so that τ_n is very large. Therefore, no interface trap response occurs for the frequencies of interest and C_{it} approaches zero. In the gate bias range between strong accumulation and strong depletion, there is limited interface trap response, and the value of C_{it} is between these two extreme cases. Even the use of physically unrealistic parameters (e.g. capture cross-section of 10^{-4} cm^2) or different energy distributions within the classical interface state capacitance framework cannot reproduce the measured behavior of many compound semiconductors [161].

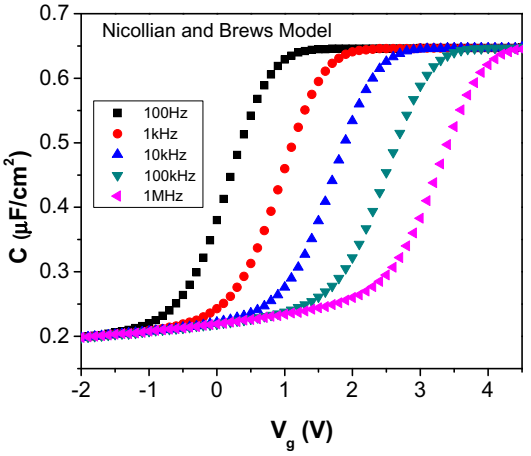

Fig. 13. Modeled GaAs C–V characteristics including classical interface state capacitance (Eq. (2)). See [34].

3.1.2. Hasegawa and Sawada C_{it} model

Hasegawa and Sawada have previously developed a model that can explain the behavior [155,156,163]. It is assumed in the classical treatment of interface state capacitance that defects distributed away from the interface (into the dielectric) cannot respond to the small signal associated with the capacitance measurement. However, Hasegawa and Sawada performed a time domain analysis of Deep Level Transient Spectroscopy (DLTS) measurements of interface states which suggests trapping time constants not consistent with this assumption. The trapping time constants suggest an interfacial region with a conduction band 0.33 eV lower than that associated with crystalline GaAs. They suggest that this region is associated with a thin disordered interfacial layer at the interface of III–V semiconductors and the related disorder-induced gap states (DIGS) where the defects are distributed in both energy and space. A similar low resistivity interfacial region has also been suggested by Passlack to explain the dispersion behavior [148]. Hasegawa and Sawada found that the dispersion results can be reproduced if one assumes an exponentially decaying spatial distribution of traps into the dielectric,

$$N_T(x) = N_{T0} \exp(-\alpha x), \quad (5)$$

where $N_T(x)$ is the trap density as a function of position and α is the decay constant. Assuming tunneling into these defects (after Preier [162]), the following relationship was obtained for the interface state capacitance:

$$C_{it} = \frac{q^2 N_{T0}}{2\kappa_0} (\omega\tau_0)^{(\alpha/2\kappa_0)} \int_0^{1/\omega\tau_0} z^{(\alpha/2\kappa_0)} \tan^{-1}(z^{-1}) dz \quad (6)$$

$$\text{assuming, } \tau(x) = \tau_0 \exp(2\kappa_0 x) \quad (7)$$

where κ_0 is the quantum–mechanical decay constant of electron wave function, and τ_0 is the time constant of the trap located at the interface.

Fig. 14 shows the simulated interface state capacitance plots of an n-type and p-type GaAs MOS capacitor using this Hasegawa-Sawada model [178]. Donor type D_{it} was assumed to be in the lower half of the gap and acceptor type D_{it} in the upper half of the bandgap. The difference between the classical model and the tunneling model is immediately apparent. The C_{it} has a frequency dependence that varies with each decade frequency change. The

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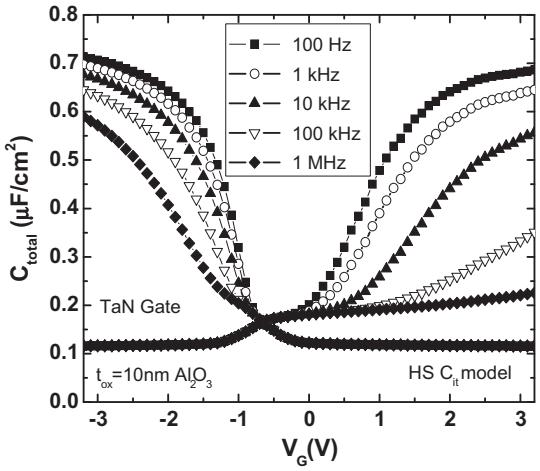

Fig. 14. Simulated *C–V* characteristics of MOS capacitors on both *n*-type and *p*-type GaAs using the Hasegawa–Sawada C_{it} model. The model capacitance shows a frequency dispersion similar to the experimentally observed phenomena. After [178].

values of $\alpha = 50$ Å and $k_0 = 2$ Å were used in these calculations. As the total capacitance is dominated by C_{it} rather than C_{sub}, the C_{total}–V_g plot shows a frequency dependence of the maximum capacitance.

The frequency dependent capacitance characteristics shown in Fig. 14 are quite similar to the experimentally observed frequency dispersion for GaAs MOS capacitors (e.g. Figs. 12 and 15b). The disparity in dispersion of *n*-type vs. *p*-type GaAs is primarily related to the difference in trapping time constants for *n*-type vs. *p*-type (differences in effective density of states for electrons and holes) and the energy distribution of interface states [46].

3.1.3. Detection of free carriers

An important factor necessary to observe dispersion in the capacitance is that the substrate capacitance must be small as compared to the interface state capacitance. With low to moderate interface state density, the total capacitance for all frequencies merges in accumulation and, potentially, inversion due to the substrate capacitance becoming much larger than interface state capacitance. To observe frequency dispersion, the interface state capacitance in Eq. (2) must be larger than the substrate capacitance. This means that the observation of maximum capacitance in a low frequency capacitance–voltage curve does not necessarily indicate the presence of free carriers [34,109,150,167]. This statement is valid for both majority and minority carrier response. For majority carriers, the substrate capacitance does not have a dependence on measurement frequency ($F \approx 10^2$–10^6 Hz). For minority carriers, the substrate capacitance of a capacitor is limited by the time constant for minority carrier generation. Therefore, the minority carrier (inversion) substrate capacitance depends on frequency as well as sweep rate [159]. The maximum capacitance in inversion as a function of frequency is sometimes used to infer the presence of inversion. However, the interface trap time constants and associated capacitance response as a function of frequency demonstrates that this methodology cannot be used to necessarily infer inversion.

3.2. Interface states of $In_xGa_{1-x}As$

The interface state density of $In_xGa_{1-x}As$ is extremely important from a technological point of view. Although there are subtle differences in interface states with different dielectrics and interfacial cleans, the most salient differences are observed by applying an interfacial "passivation" layer such as amorphous Silicon and by changing Indium concentration. The following will provide a brief review of the impact of these experimental parameters.

3.2.1. Effect of Silicon interfacial passivation layer (IPL)

Interfacial passivation layers (e.g. amorphous Silicon) between the dielectric and III–V semiconductor have been explored previously [163,164] and has been reinvestigated for thin (~1–2 nm) films recently [24,34,142,150,166,209]. Fig. 15d shows the *C–V*

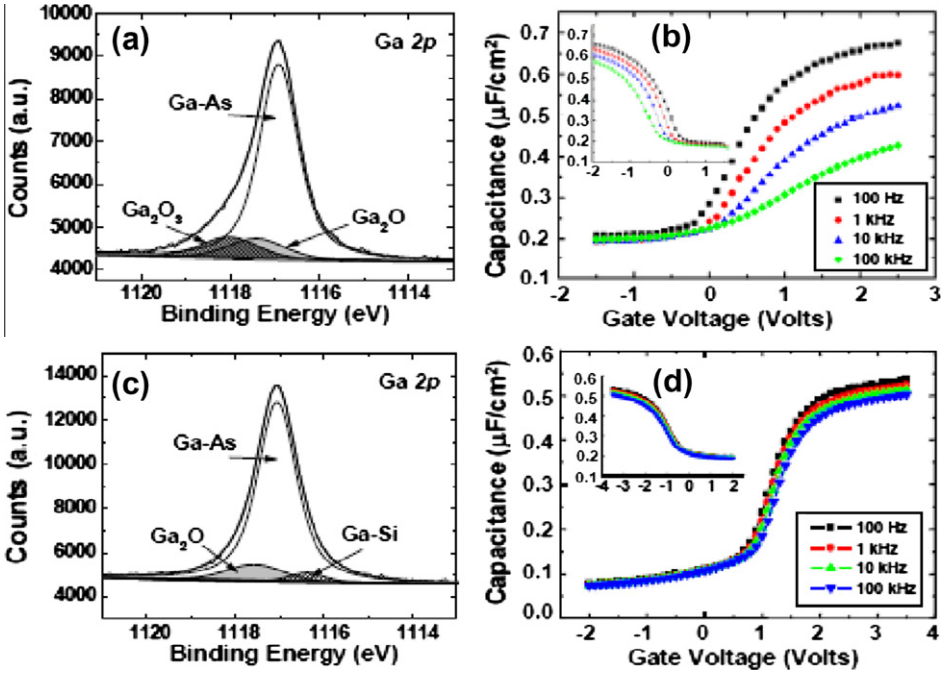

Fig. 15. Capacitance–voltage characteristics of GaAs MOS capacitors and corresponding XPS spectra. (a) XPS of ~1 nm ALD Al_2O_3 directly on GaAs, (b) corresponding CV curves for *n*-type (inset *p*-type) GaAs with ~11 nm ALD Al_2O_3, (c) same as (a) with ~1.2 nm PECVD amorphous Silicon interlayer and ~1 nm of ALD Al_2O_3, and (d) corresponding CV curves to (c) for *n*-type (inset *p*-type) GaAs with ~11 nm ALD Al_2O_3. After [165].

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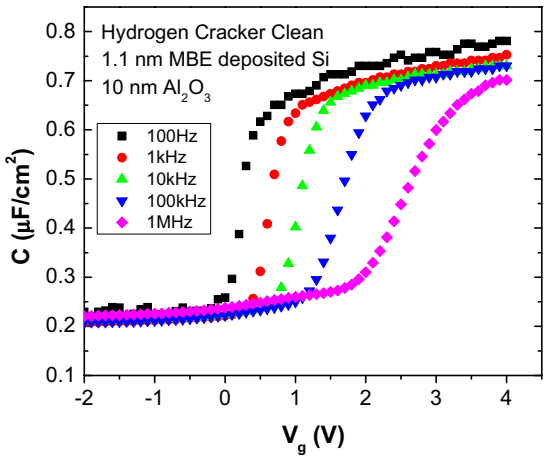

Fig. 16. Capacitance–voltage characteristics of GaAs MOS capacitors with ~1.1 nm MBE deposited Silicon interlayer and ~10 nm of ALD Al2O3. After [4], reprinted with permission Springer© 2010.

characteristics for GaAs MOS capacitors with the presence of an amorphous Silicon IPL deposited using PECVD (100 sccm of 2% SiH_4/He, 400 sccm of He, 50 W, 200 °C). This deposition condition results in approximately 1.2 nm of amorphous silicon. It is clear that the dispersion effect is reduced substantially due to the presence of this interfacial layer. Measurements at elevated temperatures show a similar reduction [36].

The associated Ga 2*p* XPS spectra for these interfaces are also presented in Fig. 15a and c [35,36,165]. In addition to a complete absence of detectable As-oxides at these interfaces (not shown here) due to either the ALD "self-cleaning" phenomenon [45] or the gettering reaction of the Si IPL with surface oxides to form Si–O species [165], it is seen (Fig. 15c) that the presence of the silicon interlayer dramatically reduces the presence of the Ga 3+ oxidation state, while leaving a detectable Ga 1+ oxidation state. It is therefore proposed that the higher oxidation states of Ga (and not those of As) are related to the species that cause high D_{it} for devices similarly fabricated, and hence Fermi level pinning (low substrate capacitance), either from a direct removal of defect states induced from Ga 3+ or from a resultant bonding reconfiguration, such as the formation of undimerized As, when Ga_2O_3 is present [50]. It is again noted that the Ga_2O bonding arrangement remains for *all* interfaces that have been exposed to oxidizing species at some point in the fabrication process, suggesting that the Ga 1+ oxidation state is *not* the species primarily responsible for Fermi level pinning. This observation is consistent with prior reports utilizing Ga_2O deposition on GaAs by MBE methods with improved electrical characteristics [47,51]. Transport characteristics of $In_xGa_{1-x}As$ MOSFETs with and without a silicon interlayer are consistent with these *C–V* results. Drastically improved MOSFET performance can be achieved using an amorphous silicon passivation layer [40]. An extracted peak mobility >3600 cm^2/Vs is achieved for $In_{0.53}Ga_{0.47}As$ with an amorphous silicon interlayer upon correction of interface state capacitance [166].

Although a lower defect density is one of the requirements necessary to reduce frequency dispersion of the maximum capacitance, another critical requirement is to alter the time constant of these defects. The Hasegawa–Sawada model alters the typical interface state time constant by permitting trapping and detrapping in a thin disordered interfacial layer and the related DIGS. Fig. 16 shows the experimental *C–V* characteristics for GaAs MOS capacitors with conditions similar to that of Fig. 15 except the amorphous Silicon interlayer is formed using *in situ* MBE methods [34]. Although the interface state density is very high and results in a shift in the transition region with frequency, the maximum capacitance shows vastly reduced dispersion. This behavior can be reproduced using the classical interface state model as shown in Fig. 13. The results suggest that the formation of the Ga 3+ oxidation state occurs in conjunction with a disordered interfacial layer. The disorder induced gap states (DIGS) have time constants which permit dispersion of the maximum capacitance. The silicon interlayer reduces the DIGS, but typical interface states are still possible.

3.3. Effect of Indium concentration

The Indium concentration also dramatically influences the measured interface state density. Fig. 17 shows *C–V* characteristics for ALD HfO_2 on $In_{0.53}Ga_{0.47}As$ and GaAs from O'Conner et al. [167]. It is important to note that the frequency dispersion observed for the ALD HfO_2 film on GaAs is very similar to the results of Fig. 12 for ALD Al_2O_3. This provides further evidence that the most important parameter controlling interfacial defect density is the oxygen bonding and that details associated with the specific dielectric used are a second-order effect. It is noted in that work that the frequency dispersion of maximum capacitance for GaAs, $In_{0.15}Ga_{0.85}As$ and $In_{0.30}Ga_{0.70}As$ are very similar suggesting very high interfacial defect density. However, the frequency dispersion of maximum capacitance for $In_{0.53}Ga_{0.47}As$ is dramatically reduced as observed in Fig. 17a. The *C–V* results as a function of Indium concentration are consistent with transport data from $In_xGa_{1-x}As$ MOSFETs. The maximum drive current for $In_{0.53}Ga_{0.47}As$ is $\sim 5 \times 10^7$ higher than $In_{0.20}Ga_{0.70}As$ with no silicon interlayer [40]. This difference is related to the extremely small inversion

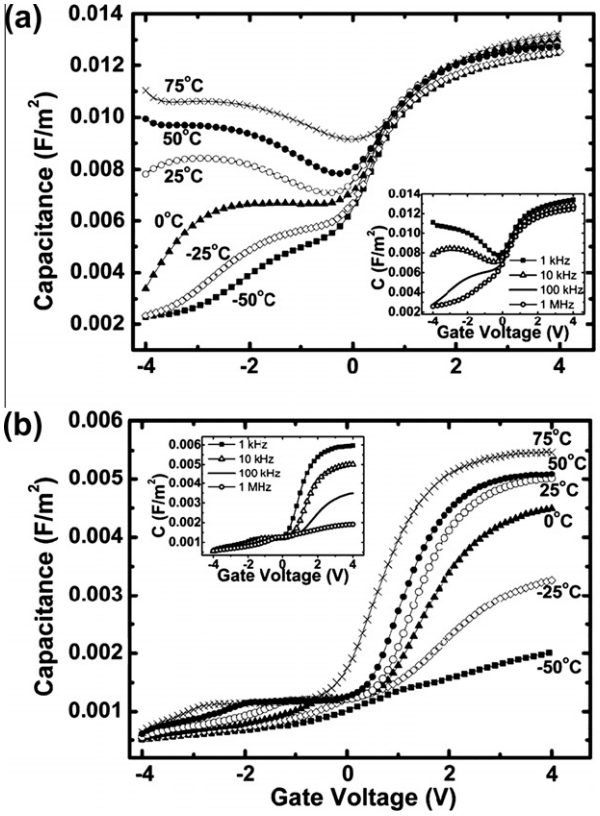

Fig. 17. 10 kHz capacitance–voltage response with varying temperature (−50 to 75 °C) of (a) unpassivated Pd/9.5 nm ALD HfO_2 on $In_{0.53}Ga_{0.47}As$ and (b) unpassivated Pd/11.4 nm ALD HfO_2 on GaAs. The insets show corresponding room temperature capacitance–voltage frequency variation (1 kHz to 1 MHz) in unpassivated $In_{0.53}Ga_{0.47}As$ and GaAs devices, respectively. From [167]. Reprinted with permission, © 2009, American Institute of Physics.

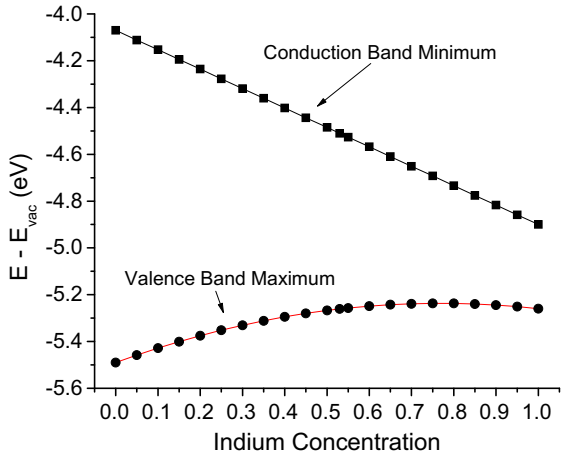

Fig. 18. $In_xGa_{1-x}As$ conduction band minimum and valence band maximum referenced to vacuum as a function of Indium concentration (x) [4]. Reprinted with permission, © 2010 Springer.

charge density of $In_{0.20}Ga_{0.70}As$ due to pinning of the Fermi level by the DIGS.

There are two possible explanations for this behavior. The first is that the primary defect responsible for the dispersion in maximum capacitance is in the upper half of the bandgap of GaAs such that the defect is within the conduction band for $In_{0.53}Ga_{0.47}As$. Fig. 18 shows the conduction band minimum and valence band maximum of $In_xGa_{1-x}As$ as a function of Indium concentration. The electron affinity (conduction band minimum) for $In_{0.53}Ga_{0.47}As$, $In_{0.30}Ga_{0.70}As$, and GaAs is ~4.51 eV ~4.32 eV, and ~4.07 eV [168,169]. Assuming that the defect energy with respect to vacuum is independent of Indium concentration, the defect responsible for frequency dispersion of the maximum capacitance would be in this energy range (~4.07 to ~4.51 eV). The second possible explanation is that the density of interfacial defects decreases with increasing Indium concentration. XPS results shown in the previous section indicate that the density of the Ga 3+ oxidation state is indeed reduced with increasing Indium concentration, as the gallium concentration is concomitantly reduced. The likely associated decrease in DIGS would result in reduced frequency dispersion of the maximum capacitance.

While DIGS associated with Ga will decrease with decreasing Ga content, this does not necessarily preclude DIGS associated with other bonds such as As–As. The presence of Ga 3+ appears to be a signature of disorder resulting in defects in the upper half of the gap. However, As–As bonds and associated midgap defects are observed with and without the presence of disorder (with and without a silicon interlayer). Several researchers have demonstrated slight reductions in the midgap defect density. Hwang et al. have shown a factor of two reduction in midgap interface state capacitance of $HfO_2/In0_{.53}Ga_{0.47}As$ MOS capacitors with a forming gas anneal [170]. Trinh et al. have suggested a strong inversion response in the C–V characteristics of $Al_2O_3/In0_{.53}Ga_{0.47}As$ MOS capacitors using a combination of wet sulfide and dry (multiple pulse "pretreatment") trimethyl aluminum surface treatment along with pure hydrogen annealing [171]. This has also been investigated recently using a combination of UHV STM and *in situ* XPS, suggesting that some portion of the defect/trap population may be reduced through such TMA pretreatments [172]. Finally, recent work employing chemical beam deposition methods with precursors that incorporate both metal and oxygen simultaneously have provided interesting high-k dielectric film growth routes and a promising electrical capacitor response [173]. The influence of interfacial In-oxides (which as noted above appears to be a minority interfacial species) on such states remains a topic of further investigation.

3.4. Transistor behavior

As noted above, the incorporation of a Si interfacial layer has been shown to improve C–V response characteristics, as well as the reduction of the Ga 3+ oxidation state [35]. Recent first-principles calculations suggest that such oxide-rich surface states may result in electrically active defects within the band gap such as As-dimers resulting in dangling-bond states [174,175]. Such species were similarly predicted in earlier tight-binding models of defects in amorphous III–V semiconductors [176,177] and may be related to the "disordered interface" model discussed above.

The correlation of the oxidation states observed on $In_xGa_{(1-x)}As$ and transistor behavior has also been recently investigated [40]. An example is shown in Fig. 19 for $HfO_2/In_xGa_{(1-x)}As(1\ 0\ 0)$ for $x = 0.53$ and 0.65using various interfacial treatments [178]. Results for the $In_{0.65}Ga_{0.35}As$ devices demonstrate much higher drive current compared to $In_{0.53}Ga_{0.47}As$ devices which can be attributed to their lower bandgap, higher intrinsic mobility and possibly lower D_{it}. Moreover, devices with an a-Si IPL exhibit the highest drive current whereas $(NH_4)_2S$ surface cleaned devices show higher drive current and trans-conductance compared to HF cleaned devices.

Fig. 20 shows the extracted μ_{eff} using the inversion charge corrected by removing the D_{it} response [179]. The fit of the split-CV data and integration to determine N_{inv} is performed to ensure error in μ_{eff} of less than 10%. Devices with an a-Si IPL exhibit the highest μ_{eff} while the $(NH_4)_2S$ cleaned devices show higher μ_{eff} than the HF cleaned devices. More negative V_t, increased mV/decade SS and increased μ_{eff} for the a-Si IPL cases are all consistent with channel compensation by a-Si. Charge pumping results show that the improved performance of the devices with an a-Si IPL and $(NH_4)_2S$ clean over HF cleaned devices cannot be related to the reduction in D_{it} near E_i. XPS suggests that devices with HF clean have a higher

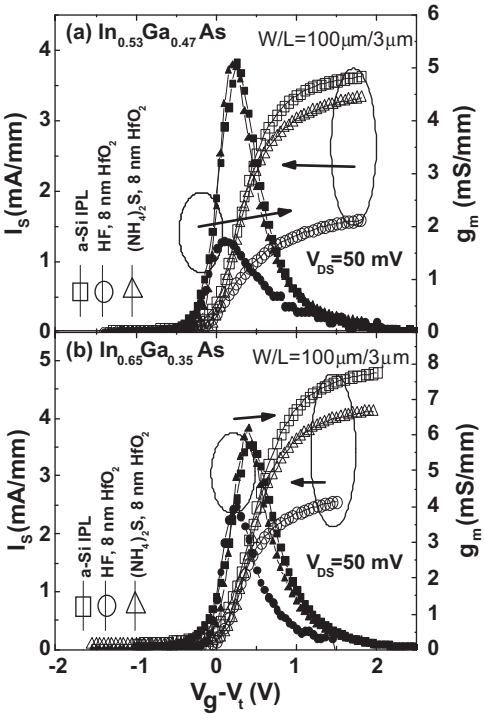

Fig. 19. Comparison of I_s–V_g and g_m–V_g characteristics of (a) $x = 0.53$ and (b) $x = 0.65$ $In_xGa_{(1-x)}As$ MOSFETs [178]. Reprinted with permission, ©2010, The Electrochemical Society.

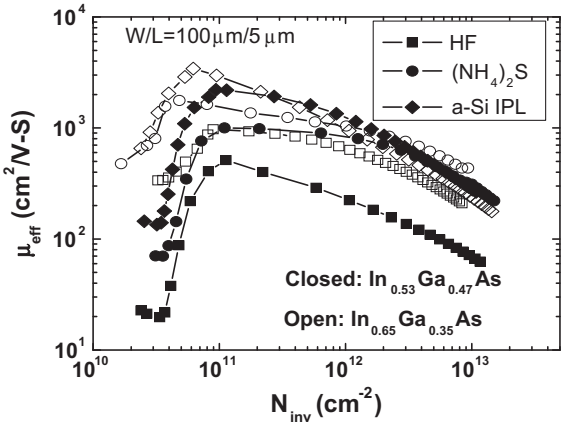

Fig. 20. Comparison of the effective mobility as a function of inversion charge density [178]. Reprinted with permission, ©2010, The Electrochemical Society.

amount of native oxide formation (Ga_2O_3) compared to the $(NH_4)_2S$ cleaned and a-Si IPL devices. This corresponds to higher D_{it} yielding higher scattering and lower mobility [35].

3.5. Effect of substrate orientation

The impact of surface orientation is a topic that has also been studied for some time, particularly for binary III–V systems such as GaAs and InAs [180]. The interaction of surface oxides and other potential dielectrics with the varied bonding available with different surface orientations is expected to impact surface channel field effect devices substantially. A key challenge is to control the surface native oxide formation, where As-oxides and Ga-oxides lead to active interface defects resulting in Fermi level (E_F) pinning, frequency dispersion, and mobility degradation [35,181].

Previous FET studies have largely concentrated on the conventional GaAs(1 0 0) surface orientation. However research indicates that the surface and interfacial properties also depend on the crystal orientation of the substrates [182,183]. For example, the study of the polar GaAs(1 1 1)A (Ga-terminated) surface [184] provides the opportunity to produce surfaces predominantly controlled by interfacial reactions with Ga and thus compare with the technologically important mixed (1 0 0) surface. In particular, studying the surface/interface properties on the major crystallographic orientations of gallium arsenide ((1 0 0), (1 1 0) and (1 1 1)A Ga-terminated and (1 1 1)B As-terminated) can lead to an understanding of these characteristics in order to achieve the desired device performance. A comparison of the Al_2O_3/GaAs interfacial chemical characteristics, and the resultant electrical properties associated with these different crystal orientations has been recently performed [185].

GaAs *n*-type substrates with 2 nm of Al_2O_3 directly deposited by ALD at 300 °C on the four GaAs surface orientations were investigated using a TMA/water chemistry. Surfaces prior to ALD growth were cleaned with HCl and $(NH_4)_2S$. Ex situ analysis of the Al_2O_3/GaAs interfaces was accomplished using monochromatic XPS with Al Kα X-ray source ($h\nu \sim 1486.7$ eV) with a line width of ~0.25 eV and spectrometer pass energy of 15 eV described elsewhere [186]. The take-off angle used was 75° relative to the substrate surface, which is more sensitive to the dielectric/bulk interface region. The *2p* spectra for Ga and As are presented here as they have superior surface sensitivity due to the associated photoelectron kinetic energy for this X-ray source [41]. For comparison, GaAs *n*-MOSFETs were fabricated to analyze the electrical properties for each surface with the same surface preparation prior to ALD growth and the process is described elsewhere [102,105].

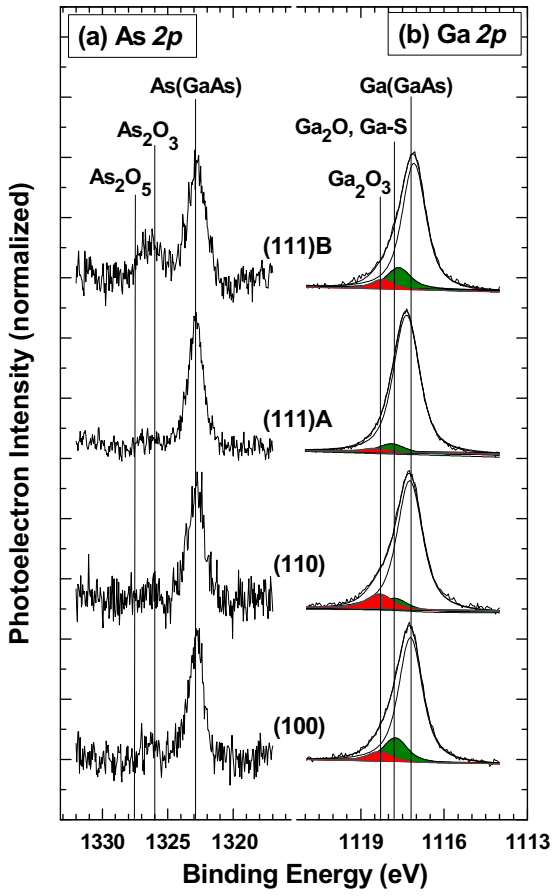

Fig. 21. Normalized (a) As 2p and (b) Ga 2p XPS peaks of 2 nm of Al_2O_3/GaAs interfaces with different crystal orientations. A higher binding energy chemical component appears in the As 2p spectra for As-terminated (1 1 1)B (~1326.5 eV) corresponds to As–O bonding. The Ga 2p spectra shows a significant difference in the formation of Ga–O bonding, depending of the surface orientation employed. The Ga-terminated (1 1 1)A surface has minimal Ga-oxides.

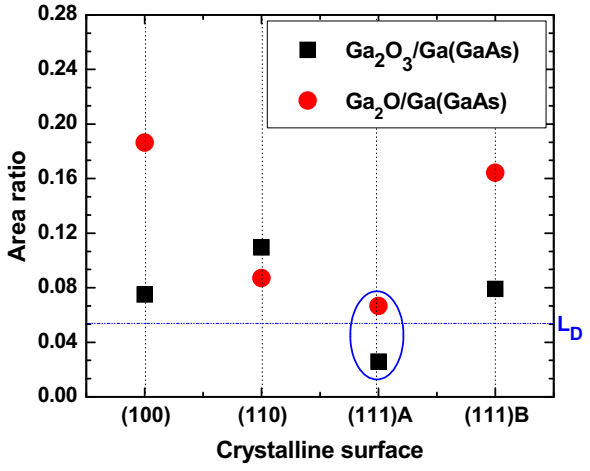

Fig. 22. XPS Intensity ratios of Ga_2O_3 and Ga_2O states relative to the bulk. The (1 1 1)A surface shows Ga–O bonds near or below the detection limit (L_D) of XPS.

Fig. 21a shows the As *2p* spectra of the 2 nm Al_2O_3/GaAs interface deposited on the four crystallographic surfaces. The (1 1 1)B surface has a peak at 1326.5 eV which corresponds to As–O bonding [187]. For the other surfaces, this peak is less obvious as its

intensity is near the detection limit. Fig. 21b shows the associated Ga *2p* XPS spectra. Deconvolution of the Ga *2p* peak shows the presence of the two oxidation states at ~0.55 eV and ~1.1 eV corresponding to Ga^{1+} (or Ga_2O) and Ga^{3+} (or Ga_2O_3) higher from the GaAs bulk [139,188]. However, Ga–S bonding from the surface treatment overlaps with Ga^{1+} due its similar binding energy ~0.75 eV higher than the bulk [189,190]. The Ga-terminated (1 1 1)A surface exhibits the least concentration of Ga-oxides compared to the other surface orientations. Consistent with prior work [190], it is noted that the area ratio for Ga-oxides relative to the bulk Ga–As peak (Fig. 22) shows a reduction of the Ga^{3+} (Ga_2O_3) feature, similar to the As^{3+} case. For the (1 1 1)A surface, the Ga^{3+} intensity is very near the detection limit, in contrast to that observed for the (1 1 0) surface which has the maximum concentration of this oxidation state for the surfaces investigated.

Fig. 23a shows the Al *2p* spectra for these surfaces and indicates the presence of the interfacial formation of aluminum oxide (~75.3 eV) [190]. This result is confirmed from the O *1s* feature shown in Fig. 23b. It is also noted that *all* of the orientations indicate fluorine and carbon contamination at the submonolayer level (not shown) with the (1 1 1)A surface having lowest concentration among the surfaces investigated (<4 at.% for F). The origin of these species, based upon angle resolved measurements, is attributed to the exposure to the atmosphere prior to analysis (C) and from the ALD reactor (F).

Fig. 24 illustrates the I–V characteristics of a 4 μm-gate-length inversion-mode GaAs *n*-MOSFET (1–4.5 × 10^{17}/cm^3) on companion (1 0 0), (1 1 0), (1 1 1)A surfaces prepared as described earlier [102]. The maximum saturation drain current (at the gate-source bias V_{GS} = 4 V) for GaAs(1 0 0) is $I_{D,sat}$ = 3.5 × 10^{-4} μA/μm and for GaAs(1 1 0) is $I_{D,sat}$ = 1.2 × 10^{-3} μA/μm. In contrast, the MOSFET on the (c) GaAs(1 1 1)A surface shows a $I_{D,sat}$ = 30 μA/μm, larger by a factor of 85,000× or 25,000× respectively of the other two surfaces. The *n*-MOSFET on GaAs(1 1 1)B, which exhibits an abundance of As-oxide at the interface (Fig. 21a), indicates that essentially a zero drain current is obtained (not shown). Fig. 24d shows the effective mobility from a 20 μm gate length *n*-MOSFET on GaAs(1 1 1)A. The maximum effective mobility of 1402 cm^2/V

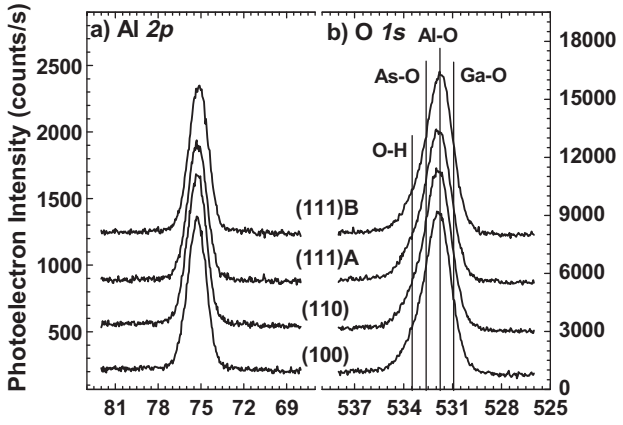

Fig. 23. (a) Al 2p and (b) O 1s XPS features for the four surfaces. Both features indicate the interfacial formation of Al_2O_3.

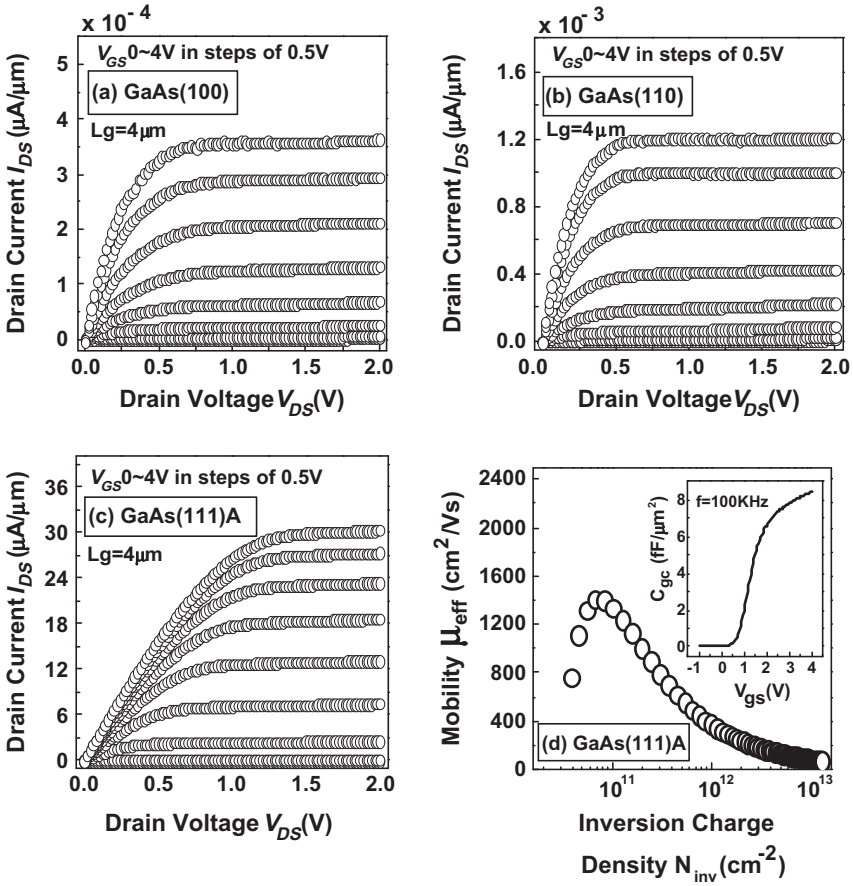

Fig. 24. Output characteristics (I_{DS}–V_{DS}) for Al2O3/GaAs (a) (1 0 0), (b) (1 1 0) and (c) (1 1 1)A n-MOSFETs with 4 μm-gate length. Al_2O_3/GaAs(1 1 1)A n-MOSFET present higher drain current (~30 μA/μm) over the other surfaces. (d) The effective mobility μ_{eff} from 20 μm gate length n-MOSFET on GaAs(1 1 1)A. The peak electron effective mobility is 1402 cm^2/Vs. The inset shows the *C–V* data for the inversion charge at 100 kHz. After [185].

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is extracted from the transconductance (G_m) vs. gate bias characteristic at a drain-source voltage V_{DS} = 0.05 V (not shown). The inset shows the capacitance–voltage (C–V) at 100 kHz for the inversion charge. Further details on the electrical characteristics of the associated devices are presented in Ref. [185].

These results show that the GaAs (1 1 1)A surface, with an unpinned E_F, is very different compared to the other surfaces. Previous work demonstrated that lower inversion currents are the result of E_F pinning [150] and this effect appears to be observed here for the (1 0 0), (1 1 0) and (1 1 1)B surfaces. The improved I–V behavior is in agreement with the XPS data interpretation that the minimized oxide formation at the interface of the (1 1 1)A surface, and in particular of the reduction of the Ga 3+ oxide by the ALD chemical process, leads to defect reduction [185]. The reduction of the Ga 3+ state has been shown previously to correlate to a reduction of the C–V frequency dispersion and D_{it}, resulting in an unpinned E_F [34]. As noted earlier, the Ga 1+ oxidation state (Ga_2O) has been shown to not cause E_F pinning [35,191]. Also, the interface defect density is reduced with the resultant low concentration of the As 3+ as well. This reduction of As–O and Ga–O bonds, especially As 3+ and Ga 3+, is consistent with the previously reported "self-cleaning" oxidation–reduction effect of the TMA precursor on the (1 0 0) surface during ALD, which may be more effective on the (1 1 1)A surface than others [45,102,139,185]. Recent work has also suggested an improvement in electrical behavior is observed for $In_{0.53}Ga_{0.47}As$(1 0 0) interfaces incorporating F [192]. Further work examining the role of the F, detected at the interface on all of these GaAs surfaces, is required, in view of recent first-principles modeling of the effect on gap states as well [182,183]. Finally, very recent reports suggest that mobility boosts are observed for $In_{0.53}Ga_{0.47}As$(1 1 1)A surface [193], which may be related to better interface roughness control as well as interfacial oxide formation [40].

This work highlights the importance of controlling oxide formation for high-mobility III–V device behavior through studying the crystallographic surface orientation-dependence of the surface oxidation and the correlated MOSFET device performance. It is found that the GaAs(1 1 1)A surface, which presents a minimal concentration of As-oxides and Ga-oxides after the self-cleaning by ALD, results in an unpinned E_F, with superior drain current relative to other surface orientations.

4. Conclusions

Despite having been studied in great detail for more than 30 years, the dielectric/III–V semiconductor interfaces and the identification of the bonding configurations that cause the defects has remained challenging. Problems with metal–oxide–semiconductor devices on GaAs and InGaAs, including frequency dispersion of capacitance and sub-optimal electron mobility, have been attributed to a number of different defects. Recent research indicates that avoiding surface and interfacial defect formation is critical in every step of device fabrication. This includes the right surface reconstruction as well as the formation of particular species of interfacial oxides, either through direct deposition or alternatively through targeted reduction of native oxides during ALD of high-k dielectrics. The work summarized here has shed considerable light on the relationship of the interfacial chemistry to a significant portion of the electrically-active defect population.

Further work is now underway exploring the effect of separating the dielectrics layer and the underlying channel through the use of epitaxial barriers [194,195]. This approach, essentially a highly-scaled version of a buried channel device such as a high electron mobility transistor (HEMT), is expected to enable a high quality channel/barrier interface while decoupling some of the scattering effects that can be introduced by high-k dielectrics. Recent work [12,13,196–198] suggests that this approach may be fruitful when benchmarked to Si-based transistors at larger dimensions [199].

Regardless of the approach, it is clear that many challenges remain to successfully integrate InGaAs into high-volume Si-based CMOS technology where costs are closely managed. The talents of scientists and engineers from many disciplines will again be utilized to meet this challenge, just as in the case of the successful integration of high-k dielectrics on Si.

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