III-V CMOS Devices and Circuits with High-Quality Atomic-Layer-Epitaxial La$_2$O$_3$/GaAs Interface

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Introduction

GaAs, as the most studied III-V semiconductor, has been long-time considered to replace Si in logic applications [1]. In order to achieve a thermodynamically stable dielectric on GaAs with a high quality interface, tremendous efforts have been made by different passivation techniques [2-9] since its first publication in 1965 [10]. Recently, we reported high-performance GaAs nMOSFETs with single crystalline La-based oxide dielectrics [11, 12], showing breakthrough in the drive current. In this work, we demonstrate, for the first time, high-performance GaAs-based CMOS devices and circuits (inverters, NAND and NOR logic gates, and five-stage ring oscillators). These devices were enabled by the high-quality interface of single-crystalline La$_2$O$_3$ grown on GaAs(111)A by atomic layer epitaxy (ALE).

Experiments

Fig. 1(a) shows the schematics of nMOSFET and pMOSFET fabricated in this work on a common semi-insulating GaAs (111)A substrate with a common ALE high-k dielectric. The detailed process flow is depicted in Fig. 1(e). The epitaxial La$_2$O$_3$ thick films employed here were deposited using lanthanum trist(N,N-diisopropyllformamidinate) and H$_2$O as precursors at 385°C, while the amorphous Al$_2$O$_3$, capping layer was deposited with precursors of trimethylaluminum (TMA) and H$_2$O at 300°C. Uniform epitaxial layers were grown by the employment of long purging times (40 s – 80 s). The Al$_2$O$_3$ capping layer is applied to protect the La$_2$O$_3$ from reacting with the air. The fabricated GaAs MOSFETs in the integrated circuits have a nominal gate length varying from 1 to 8 µm, and the gate width ratios of nMOSFETs to pMOSFETs in GaAs CMOS inverters vary from 1:3 to 1:10. The capacitors were fabricated on n-type GaAs(111)A substrates of doping $5\times10^{17}$ cm$^{-3}$ and n-type GaAs(111)A substrates of doping $6\times10^{17}$ cm$^{-3}$, with 8nm La$_2$O$_3$ epitaxial oxide layer and 6nm Al$_2$O$_3$ capping layer.

Results and Discussion

Fig. 1(b) shows the atomic structure of the epitaxial La$_2$O$_3$/GaAs interface. The epitaxial structure of La$_2$O$_3$ was confirmed by the electron diffraction pattern and HRXRD results (Fig. 1(c)). The coupled 2θ scans suggest that the lattice mismatch of La$_2$O$_3$ on GaAs(111)A is only 0.04%, if relaxed epitaxy is assumed. A HRTEM image of the epitaxial interface, taken from a sample with 20nm La$_2$O$_3$ after 860°C annealing, is shown in Fig. 1(d), which further evidences that a flat and thermodynamically stable La$_2$O$_3$/GaAs(111)A interface, as shown in Fig. 1(d), which further evidences that a flat and thermodynamically stable dielectric on GaAs with a high quality inter-/v. Both p-type and n-type high frequency and quasi-static CV characteristics are plotted in Fig. 4(a). The high-frequency CV curves taken from 1kHz to 1MHz show small frequency dispersion at accumulation regions. Surface potentials were determined from the quasi-static CV characteristics using Berglund’s equation. The surface potential movement is about 0.94 eV at a gate bias of 1.5 V calculated from p-type CV, while from the n-type CV the surface potential movement is determined to be -1.06 eV at a gate bias of -2 V. The room temperature conductance method was employed to determine $D_s$, which is greatly reduced compared to the amorphous Al$_2$O$_3$/GaAs(111)A interface, as shown in Fig. 4(b). The temperature-dependent electron effective mobility is shown in Fig. 4(c). The slight increase of the mobility in moderate $N_d$ is due to less phonon scattering while the decreasing mobility at low $N_d$ suggests strong influence of Coulomb scattering. For GaAs based logic circuits, the inverter voltage transfer characteristics are plotted in Fig. 5(a), measured at different supply voltages ($V_{dd}$ = 2, 2.5 and 3 V). The corresponding inverter gain dependences on $V_{dd}$ are shown in Fig. 5(b), and a gain of ~12 is obtained with $V_{dd}$ = 3 V. The GaAs CMOS logic circuit operation is further demonstrated by NAND and NOR logic gates. The measured NAND and NOR logic gates outputs are plotted in Fig. 6(a-b), respectively. The supply voltage $V_{dd}$ used in the logic gates is 2.5 V, and for both input and output voltages the logic “1” is corresponding to ~2.5 V while the logic “0” is corresponding to ~0 V (GND). Four combinations of input states “1 1”, “0 1”, “1 0” and “0 0” and corresponding output results are highlighted. Fig. 7(a) shows a five stage ring oscillator and the corresponding output characteristics. The output power spectrum of the same oscillator is given in Fig. 7(b) and an oscillation frequency of 3.87 MHz is obtained at $V_{dd}$=2.75 V. The fundamental oscillation frequency increases from 0.35 MHz to 3.87 MHz as $V_{dd}$ increases from 1 to 2.75 V.

Conclusion

By realizing a high-quality epitaxial La$_2$O$_3$/GaAs(111)A interface, we demonstrate GaAs CMOS devices and integrated circuits including nMOSFETs, pMOSFETs, CMOS inverters, NAND and NOR logic gates and five-stage ring oscillators for the first time. As an exercise of III-V CMOS circuits on a common substrate with a common gate dielectric, it provides a route to realize ultimate high-mobility CMOS on Si if long-time expected breakthroughs of III-V epi-growth on Si occur.

References

Fig. 1 (a) Schematics of a GaAs pMOSFET and an nMOSFET in this work. (b) Atomic structure view of the single crystalline La$_2$O$_3$ layer over GaAs(111)A surface. (c) High-resolution X-ray omega-two theta coupled scan for La$_2$O$_3$ on GaAs(111)A. The lattice mismatch between the GaAs substrate and the La$_2$O$_3$, epitaxial film is determined to be ~0.04%. (d) HR-TEM image of a La$_2$O$_3$/GaAs(111)A epitaxial interface. A flat and sharp interface (denoted by the white dash line) can be observed. (e) Process sequence for the fabrication of GaAs[111]A MOS circuits. The epitaxial interface is formed by ALD 4nm single crystalline La$_2$O$_3$, followed by 4nm ALD amorphous Al$_2$O$_3$ as an encapsulation layer. Si and Zn were used for N+ region and P+ region ion implantation, respectively.

Fig. 2 (a) Output characteristics for a $L_g$=1µm GaAs(111)A nMOSFET with GaAs/La$_2$O$_3$ epitaxial interface. (b) Transfer curves of the same device in (a). A low SS of 74 mV/dec is obtained. (c) Effective electron mobility extracted from a $L_g$=8µm nMOSFET.

Fig. 4 (a) Quasistatic and high-frequency C-V curves of both p-type and n-type capacitors with Al$_2$O$_3$/GaAs epitaxial interface. (b) $D_f$ distribution of both amorphous Al$_2$O$_3$/GaAs(111)A and epitaxial La$_2$O$_3$/GaAs(111)A interfaces. (c) Electron mobility vs charge density relation in various temperatures.

Fig. 6 (a) $V_o$ and $V_{in}$ of the GaAs CMOS NOR logic gate. Four combinations of input states and corresponding output states are marked. (b) $V_o$ and $V_{in}$ of the GaAs CMOS NAND logic gate.

Fig. 7 (a) Illustration, circuit schematic, optical micrograph and output characteristics of a GaAs CMOS five-stage ring oscillator. (b) Measured output power spectrum of a five-stage GaAs CMOS ring oscillator.