RTN and Low Frequency Noise on Ultra-scaled Near-ballistic Ge Nanowire nMOSFETs

Wangran Wu1,2,3, Heng Wu1, Mengwei Si1, Nathan Conrad1, Yi Zhao2,3 and Peide D. Ye*1
1School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, U.S.A.
2School of Electronic Science and Engineering, Nanjing University, Nanjing, 210093, China
3State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou, 310027, China
#Email: yep@purdue.edu

Abstract

In this work, we present the first observation of random telegraph noise (RTN) in ultra-scaled Ge nanowire (NW) nMOSFETs. The impacts of NW geometry, channel length, EOT, and channel doping on low frequency noise are studied comprehensively. It is confirmed that the low frequency noise with 1/f characteristics is attributed to the mobility fluctuation in ultra-scaled Ge NW nMOSFETs. The low frequency noise decreases when the channel length scales down from 80 nm to 40 nm because of the near-ballistic transport of electrons.

Introduction

Ge channel is one of the promising candidates for future ultimate CMOS applications because Ge has high and balanced electron and hole mobility, good compatibility with Si large-scale-integration technologies and great potential for voltage scaling [1-2]. Ge CMOS has been intensively studied in the past decade and highly scaled Ge NW CMOS has been demonstrated to offer excellent performance [3-5]. However, advanced high-k/Ge gate stacks with scaled EOT and superior MOS interfaces are still needed to develop Ge CMOS manufacturing technology with high reliability [6]. The conventional C–V method and charge pumping method cannot be applied to ultra-small devices without a body contact. It is increasingly hard to directly measure the interface and oxide property when the devices are aggressively scaled down to sub-100 nm. Therefore, low frequency noise and RTN can be used as alternate probes for device characterization and process optimization since noise measurement is not limited by the small gate capacitance [7-9]. In the meanwhile, low frequency noise and RTN have serious impacts in scaled non-volatile memories and logic circuits [10-11]. Several groups have reported low frequency noise study of long channel Ge MOSFETs [12-13]. There is still no study on low frequency noise and RTN of highly scaled Ge MOSFETs with sub-100 nm gate length.

In this paper, we: 1) report the first observation of RTN in ultra-scaled Ge NW nMOSFETs and extract the basic parameters of the devices; 2) systematically study the properties of low frequency noise on Ge NW nMOSFETs with various NW geometries (NW width, NW height, channel length); 3) study the channel area, S Vg increases with the decrease in W NW and H NW because of the near-ballistic transport of electrons.

Results and Discussion

A. RTN characteristics

Figs. 3-4 show the good output and transfer characteristics of a Ge NW nMOSFET with L NW of 40 nm and EOT of 2 nm. Typical RTN signal of drain current (I d) with signal trap and two traps are illustrated in Fig. 5. Two and four distinct current switching levels are observed in the two devices with the same device dimension. The trap number n can be estimated from current fluctuation levels N via 2 n-1<N≤2n. The corresponding histograms of I d with two and four peaks are shown in Fig. 6. The histograms show the superposition of RTN signal and mobility fluctuation (1/f) noise. Average time constants in single trap RTN, such as capture time constant (τ c) and emission time constant (τ e), are extracted by exponential fitting to time constants distributions (Fig. 7). τ c and τ e may change with gate voltage (V gs) because of the move of Fermi level. Clear RTN signals were observed when V gs was near threshold voltage (V th). The relation between τ c, τ e, τ c/τ e and V gs is shown in Fig. 8. The negative correlation between τ c/τ e and V gs indicates that the electrons’ trapping and de-trapping occurring between channel and gate oxide [9]. The depth of this trap from the interface (x T) in the gate oxide can be calculated according to the formula in Fig. 8. For the trap in 1# device of Fig. 5, x T changes from 0.6TOX (oxide thickness) to 20 nm oxide thickness, indicating that it is a deep trap.

B. Low frequency noise

Fig. 9 shows the power spectrum density (PSD) of I d (SId) in 1# device of Fig. 5 under different gate voltages. Typical Lorentzian spectrum with 1/f characteristics is observed. The low frequency noise increases with higher V gs. The normalized SId/Id (SId/Id) between two devices, sharing the same device dimension, with and without RTN signal is compared in Fig. 10. The noise spectrum of device without RTN shows 1/f characteristics. The low frequency noise results (SId, SId) in Figs. 11-16 are obtained in devices without RTN at a frequency of 10 Hz and each group of the data contains experimental results from several devices sharing the same device dimension. Figs. 11-12 show the normalized SId (SId/Id) as a function of L NW. The clear L NW dependence agrees well with the mobility fluctuation model [14]. Fig. 12 presents the input gate noise (SId/Sg0/g0) normalized by channel area (W ch·L ch·S Vg) versus L NW. The normalized SId decreases when the L NW scales down, while the classical theory indicates W ch·L ch·S Vg shall be independent of channel area [14]. The anomalous scaling trend of low frequency noise can be attributed to the near-ballistic transport of electrons in the channel. Because of the electron’s long mean free path in Ge, electrons encounter less scattering at smaller L NW. Therefore, the scattering induced mobility fluctuation decreases at small L NW, thus the normalized SId reduces. Similar results were also observed in highly scaled InGaAs MOSFETs as reported in Ref. [15]. Also, the parabolic increase of SId confirms again the low frequency noise is attributed to the mobility fluctuation other than the carrier number fluctuation [16]. Since scattering is an important source of low frequency noise, SId is smaller in IM NW MOSFETs because the relative lower channel doping would induce less Coulomb scattering (Fig. 13). SId decreases in device with smaller EOT because of the enhancement of gate control (Fig. 14). The change in NW geometries affects the low frequency noise due to the change of channel area. Since low frequency noise is inversely proportional to the channel area, SId increases with the decrease in W NW and H NW (Figs. 15-16). The advantage of device performance, the increase of H NW promises the enhancement of on-state performance, i.e., I d and g m per pitch area, and the suppression of low frequency noise.

Conclusion

We report the first observation of RTN in Ge NW nMOSFETs. The mobility fluctuation is confirmed to be the source of low frequency noise in ultra-scaled Ge NW nMOSFETs other than the carrier number fluctuation. Because of the long mean free path of electrons in Ge, the low frequency noise is suppressed at shorter channel due to the near-ballistic transport at sub-100 nm region. Therefore, ultra-scaled Ge NW MOSFETs with low channel doping, small EOT and high H NW promise the performance enhancement as well as the suppression of low frequency noise.

Reference

Fig. 1 Fabrication process flow of the Ge NW nMOSFETs.

Fig. 2 Schematic diagram of the Ge NW nMOSFETs. The cross-section view shows the accumulation mode (AM), inversion mode (IM) nMOSFETs and the key geometry parameters.

Fig. 3 Output characteristics of a 40 nm Lch NW nMOSFET with an EOT of 2 nm.

Fig. 4 Transfer characteristics of the same device in Fig. 3. SS of 91 mV/dec is achieved at Vds=0.5V.

Fig. 5 I_D fluctuation due to RTN with single trap (upper) and two traps (lower) in two different Ge nMOSFETs having the same device dimension (1#, 2#).

Fig. 6 Histograms of the RTN signal in 1# and 2# devices shown in Fig. 5. Two and four peaks are observed respectively.

Fig. 7 Distribution of capture and emission time (t_c, t_e) constants of RTN signal in 1# device of Fig. 5. t_c and t_e are calculated by fitting.

Fig. 8 t_c, t_e and t_c/t_e corresponding to different gate voltages in 1# device of Fig. 5. The trap depth (x_T) can be obtained.

Fig. 9 S_Y of RTN signal in 1# device of Fig. 5 at different gate voltages, showing 1/f characteristics.

Fig. 10 Normalized S_Y of two devices, having the same device dimension, with and w/o RTN. S_Y in device w/o RTN shows 1/f characteristics.

Fig. 11 Normalized S_Y versus I_D of devices w/o RTN. 1/I_D dependence indicates mobility fluctuation induced noise.

Fig. 12 S_Y normalized by W_m*L_m of devices (w/o RTN) with different values of L_m. Normalized S_Y decreases with scaling down of L_m.

Fig. 13 S_Y versus I_D in AM and IM nMOSFETs. S_Y is smaller in IM nMOSFETs because of the less Coulomb scattering in the channel.

Fig. 14 S_Y versus I_D in devices with different EOT. S_Y decreases with the scaling down of EOT because of the enhanced gate control.

Fig. 15 S_Y versus I_D in devices with different W_NW. S_Y increases with the scaling down of W_NW because of the decrease of the gate areas.

Fig. 16 S_Y versus I_D in devices with different H_NW. S_Y increases with the decrease in H_NW because of the decrease of the gate areas.