Ultra-Fast Operation of BEOL-Compatible Atomic-Layer-Deposited In$_2$O$_3$ Fe-FETs: Achieving Memory Performance Enhancement with Memory Window of 2.5 V and High Endurance > 10$^9$ Cycles without $V_T$ Drift Penalty

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Abstract

In this work, we report the ultra-fast operation of back-end-of-line (BEOL) compatible Fe-FETs with atomic layer deposition (ALD) In$_2$O$_3$ and Hf$_2$O$_3$ (HZO) as channel semiconductor and ferroelectric gate insulator with channel length ($L_{ch}$) scaled down to 7 nm, enabled by ultra-fast I-V (UFIV) and pulse I-V measurements. It is found that device memory characteristics benefit from the ultra-shortness down to 10 ns level, by a suppression of trapping effect while maintaining fast FE switching speed. High memory performance is achieved, exhibiting a wide memory window of 2.5 V and a high endurance exceeding 10$^9$ cycles without $V_T$ drift penalty. These results suggest that oxide semiconductor Fe-FETs are promising toward monolithic 3D integration for in-memory computing at ultra-fast operation speed.

Introduction

Ferroelectric field-effect transistor (Fe-FET) based on ALD-grown ferroelectric hafnium oxide (HZO) [1] is a promising non-volatile memory device candidate due to the superior performance including scalability, fast operation speed [2-5], as well as CMOS and back-end-of-line (BEOL) compatibility [6,7]. Recently, oxide semiconductor Fe-FETs with BEOL compatible oxide semiconductor channels such as In$_2$O$_3$ [8], W-doped In$_2$O$_3$ [9], and Indium-Gallium-Zinc-Oxide (IGZO) [10] have attracted great attention for their promising applications in monolithic 3D integration toward in-memory computing. However, despite of the ultra-short $L_{ch}$ from MD frp of 500 ns to 50 µs, because pulse scheme has de-trapping during pulse time (BT) and relaxation of FE during pulse falling time. Fig. 11 shows that such phenomenon is observed at a wide range of $L_{ch}$, at $V_{DS}$ of 0.1 V with $V_{DS}$ of 500 ns. Less MW difference at long-channel devices is observed, which is likely a result of MW reduction itself at long-channel devices in general. Fig. 12 demonstrates the negligible dependency of MW on $V_{DS}$ for both long-channel and short-channel devices under UFIV tests. This suggests that a reduced $V_{DS}$ would be preferred with the same MW and better reliability characteristics by suppressing drain-induced degradation.

Experimental

Fig. 2 and 3 show the device schematic diagram and fabrication process flow of BEOL compatible ALD In$_2$O$_3$ Fe-FETs. The details of fabrication process can be referred to our previous work [8]. A control group of devices w/o Al$_2$O$_3$ interfacial layer (IL) is also included. Demonstration of ultra-short 7 nm $L_{ch}$ devices can be found at TEM images reported previously [8]. Fig. 4 presents P-V loop of FE-HZO film w/o and w/Al$_2$O$_3$ IL. A degradation of ferroelectricity is observed in stack w/o Al$_2$O$_3$ IL, because less FE-phase (O-phase) portion is formed in FE HZO without induced strain from top Al$_2$O$_3$ capping during annealing for FE formation.

Results and Discussion

Fig. 5 illustrates the waveforms applied using two different fast measurement schemes: UFIV and pulse I-V. An B1530A WFGMU is exploited to generate waveform and perform ultra-fast measurements with averaging time down to 10 ns. The shortest measurement delay (MD) for UFIV is 20 ns with rise time (RT) of 10 ns to achieve decent resolution. The average time (AT) is fixed at 10 ns for UFIV and 100 ns for pulse I-V unless otherwise stated, which are minimum times to achieve a sufficient signal resolution. Fig. 6 rules out the appearance of $\Delta V_T$ from fast test conditions by measuring a MOSFET with negligible hysteresis. Fig. 7 displays the corresponding $L_{ch}$ vs $V_{GS}$ characteristics of an ultra-short 7 nm ALD In$_2$O$_3$ Fe-FET with $L_{ch}$ of 7 nm and Al$_2$O$_3$ of 1 nm at $V_{DS}$ of 0.1 V, utilizing UFIV scheme with MD of 20 ns and $V_{DS}$ step of 0.2 V. A wide memory window (MW) of 2.5 V is achieved, greater than that of 2.2 V at conventional DC test with MD and AT of about ms level. Fig. 8 shows an evolution of $V_{T}$-vs-$V_{GS}$ characteristics with MD from 20 ns to 200 µs of an In$_2$O$_3$ Fe-FET with $L_{ch}$ of 200 nm at $V_{DS}$ of 0.1 V, demonstrating a clear MW reduction with longer MD. Fig. 9(a) and (b) plot the dependence of $V_{DS}$ on MD under UFIV tests for Fe-FETs w/ and w/o Al$_2$O$_3$ IL, respectively, illustrating that the reduction of MW with increasing MD is irreversible. This phenomenon can be interpreted as a result of different formation of FE/DE interface and bulk defects trapping/ de-trapping process by shortening MD. The FE switching assisted by leakage current through DE or IL to satisfy charge balance condition at FE/DE interface, is relatively slow as shown in Fig. 9(a). For devices w/o DE IL, charge primarily gets trapped at Fe/In$_2$O$_3$ interface, while the charge balance condition can be quickly satisfied, and thereby showing reduced $L_{ch}$ dependence in Fig. 9(b). Longer channel devices show more MD dependence since the traps in the middle of the devices take longer time to respond. The reduction of MW of Fe-FETs w/o IL compared with that with IL is mainly because of reduced ferroelectricity of HZO film, as illustrated in Fig. 4. It is also observed that the short-channel devices have enhanced MW than long-channel ones [8], indicating that trapping is less effective in short Fe-FETs.

Conclusion

In conclusion, ultra-fast operation of back-end-of-line (BEOL) compatible Fe-FETs with $L_{ch}$ down to 7 nm, enabled by ultra-fast I-V and pulse I-V measurement schemes, is systematically investigated. We achieved an enhancement of MW to 2.5 V by reducing staying time in UFIV down to 20 ns, and boosted endurance performance to 10$^9$ cycles without $V_T$ drift penalty. Ultra-fast operation to ~ few 10 ns is found to be beneficial to Fe-FET’s memory performance by suppressing charge trapping while sufficient FE switching at a fast speed.

Acknowledgement

The work is mainly supported by SRC/CDAR/A JUMP ASCENT Center, SRC nCore IMPACT Center and AFOSR.

Reference

**Fig. 1.** Schematic diagram of charge distribution in a typical Fe-FET with DE IL.

**Fig. 2.** Schematic diagram of a BEOL-compatible InO₃ Fe-FET.

**Fig. 3.** Fabrication process flow of the InO₃ Fe-FETs. Control group w/o Al₂O₃ IL is utilized.

**Fig. 4.** P-V loops of representative capacitors w/ and w/o Al₂O₃ IL. HZO w/o IL capping representing degraded ferroelectricity.

**Fig. 5.** Waveform of two ultra-fast test schemes: (a) ultra-fast I-V and (b) pulse I-V. The minimum measurement delay is 20 ns for UFIV and ~200 ns for pulse I-V. The average time is fixed at 10 ns for UFIV and 100 ns for pulse I-V unless elsewhere stated. UFIV is measured by $V_{GS}$ fast sweep with each step of 0.1 V or 0.2 V. The total sweep time for 2V as Fig.8 below is about 500 ns.

**Fig. 6.** Characterization of hysteresis in the transfer curve of InO₃ MOSFETs, where $\Delta V_T$ is negligible.

**Fig. 7.** $I_D-V_{GS}$ characteristics of an ALD InO₃ Fe-FET with $L_{ch}$ of 7 nm, Al₂O₃ of 1 nm at $V_{DS}$ of 0.1 V under UFIV with MD=20 ns and total sweep time 800 ns, highlighting a memory window of 2.5 V.

**Fig. 8.** $I_D-V_{GS}$ characteristics of a Fe-FET with $L_{ch}$ of 200 nm at $V_{DS}$ of 0.1 V with various MD, showing a clear MW shrinking. The total sweep time is ~500 ns.

**Fig. 9.** Dependence of MW on MD under UFIV scheme for Fe-FETs (a) w/ and (b) w/o Al₂O₃ IL, respectively, demonstrating MW reduction with increasing MD.

**Fig. 10.** MW dependence on MD for UFIV and pulse I-V scheme of a Fe-FET with $L_{ch}$ of 7 nm and Al₂O₃ of 1 nm at $V_{DS}$ of 0.1 V.

**Fig. 11.** Dependence of MW using UFIV and pulse schemes on $L_{ch}$ with Al₂O₃ of 1 nm at $V_{DS}$ of 0.1 V. MD is fixed at 500 ns for both schemes.

**Fig. 12.** MW dependence on $V_{DS}$ of Fe-FETs with $L_{ch}$ of 800 nm and 15 nm at $V_{DS}$ of 0.1 V.

**Fig. 13.** Pulse sequence in endurance test. UFIV scheme with MD of 300 ns is utilized. Trapezoidal pulse is exploited with pulse interval of 500 ns at $V_{DS}$ of 0.03 V.

**Fig. 14.** Endurance performance of short-channel InO₃ Fe-FETs with $L_{ch}$ of 50 nm and 7 nm at $V_{DS}$ of 0.1 V, highlighting $>10^9$ cycles endurance without $V_T$ drift. $V_T$ of 7 nm device shifts to negative due to short-channel effects.