BEOL Compatible Indium-Tin-Oxide Transistors: Switching of Ultrahigh-Density 2-D Electron Gas Over $0.8 \times 10^{14}/cm^2$ at Oxide/Oxide Interface by the Change of Ferroelectric Polarization

Mengwei Si, Anna Murray, Zehao Lin, Joseph Andler, Junkang Li, Jinhyun Noh, Sami Alajlouni, Chang Niu, Xiao Lyu, Dongqi Zheng, Kerry Maize, Ali Shakouri, Suman Datta, *Fellow, IEEE*, Rakesh Agrawal, *Member, IEEE*, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— In this work, we report back-end-of-line (BEOL) compatible indium-tin-oxide (ITO) transistors with ferroelectric (FE) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as gate insulator. A tunable high-density 2-D electron gas over $0.8 \times 10^{14}/cm^2$ is achieved at the HZO/ITO oxide/oxide interface because of the FE polarization, which is confirmed by *I–V*, positive up and negative down (PUND), and Hall measurements. Such high carrier density can be completely modulated and switched on and off by FE polarization switching, enabling high mobility ITO transistor with high ON-current and high ON/OFF ratio.**

***Index Terms*— Back-end-of-line (BEOL) compatible, ferroelectric (FE), hafnium zirconium oxide, high carrier density, indium thin oxide, oxide semiconductor.**

I. Introduction

OXIDE semiconductors are considered as promising channel materials for back-end-of-line (BEOL) compatible transistors for monolithic 3-D integration to maximize the intertier via density [1]. Thin-film transistors (TFTs) with oxide semiconductor channels, such as indium oxide [2]–[4], indium-tin-oxide (ITO) [5]–[8], W-doped In_2O_3 (IWO) [9], indium-gallium-zinc-oxide (IGZO) [10], [11], and indium-aluminum-zinc-oxide (IAZO) [12], recently attract revived attention as potential BEOL compatible transistors. High-performance ITO transistors with ferroelectric (FE) hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO) as gate insulator are recently demonstrated, exhibiting high ON-current over 1 A/mm [8]. Such high on-current density in a tens $cm^2/V{\cdot}s$ mobility material is understood due to the ultrahigh carrier density in ITO channel approaching $10^{14}/cm^2$.

The quest for high carrier density is important in electronic devices, because high carrier density can lead to high current density in semiconductor devices and even induce phase transition, i.e., superconductivity at low temperatures. However, field-effect-induced carrier density in semiconductor is limited to ~ 1–$2 \times 10^{13}/cm^2$, due to the conventional dielectric break down. The polarization in FE material can offer high polarization charge density more than $10^{14}/cm^2$ [13]–[19], which can be used to generate high-density 2-D electron gas on semiconductor with a low trap density interface. The demonstrated HZO/ITO oxide/oxide interface has a high 2-D electron density even beyond GaN-based polar semiconductor interface of ~ 2–$3 \times 10^{13}/cm^2$.

In this work, the carrier density at the HZO/ITO interface was investigated systematically by *I–V*, positive up and negative down (PUND), and Hall measurements. An ultrahigh-density 2-D electron gas over $0.8 \times 10^{14}/cm^2$ is achieved at the HZO/ITO oxide/oxide interface. It is understood that such an ultrahigh carrier density is introduced by the polarization density in FE HZO and low interface trap density at the oxide/oxide interface. The polarization switching in FE HZO also contributes to the on/off switching of ITO transistor, leading to high mobility, high ON-current, and high on/off ratio ITO transistors.

II. Experiments

Fig. 1(a) shows the schematic of an ITO transistor with p+ Si/20-nm FE HZO/3-nm Al_2O_3/ITO gate-stack. The thickness

Manuscript received January 31, 2021; accepted February 17, 2021. This work was supported in part by the Semiconductor Research Corporation (SRC)/Defense Advanced Research Projects Agency (DARPA) the Joint University Microelectronics Program (JUMP) the Applications and Systems-Driven Center for Energy-Efficient Integrated Nano Technologies (ASCENT) and in part by the SRC nanoelectronics COmputing REsearch (nCORE) Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Center. The review of this article was arranged by Editor J. F. Conley. *(Corresponding author: Peide D. Ye.)*

Mengwei Si, Zehao Lin, Junkang Li, Jinhyun Noh, Sami Alajlouni, Chang Niu, Xiao Lyu, Dongqi Zheng, Kerry Maize, Ali Shakouri, and Peide D. Ye are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA, and also with the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Anna Murray and Rakesh Agrawal are with the Davidson School of Chemical Engineering, Purdue University, West Lafayette, IN 47907 USA.

Joseph Andler is with the School of Materials Engineering, Purdue University, West Lafayette, IN 47907 USA.

Suman Datta is with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3061038.

Digital Object Identifier 10.1109/TED.2021.3061038

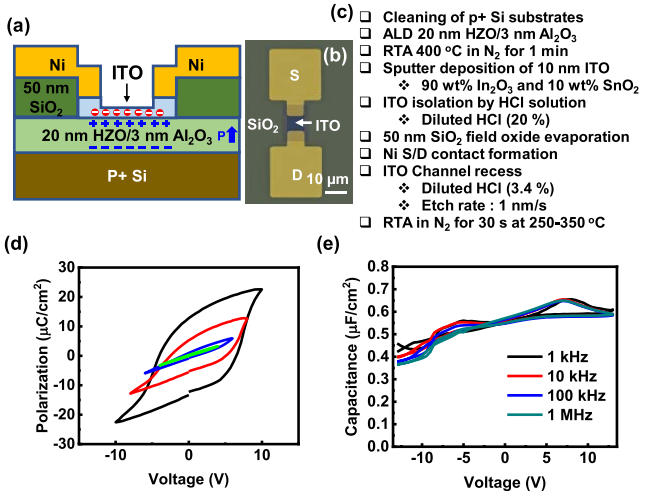

Fig. 1. (a) Schematic of an ITO transistor with 20-nm HZO and 3-nm Al_2O_3 as gate insulator. The thickness of ITO under source/drain ohmic contacts is 10 nm. The thickness of ITO channel is recessed to 2 nm. (b) False-colored SEM image of a fabricated ITO transistor. (c) Fabrication process flow of the ITO transistors. (d) *P*–*V* and (e) *C*–*V* characteristics of Ni/ITO/20-nm HZO/3-nm Al_2O_3/p+ Si capacitor, showing clear FE *P*–*V* and *C*–*V* hysteresis loop. Voltage is applied to p+ Si electrode.

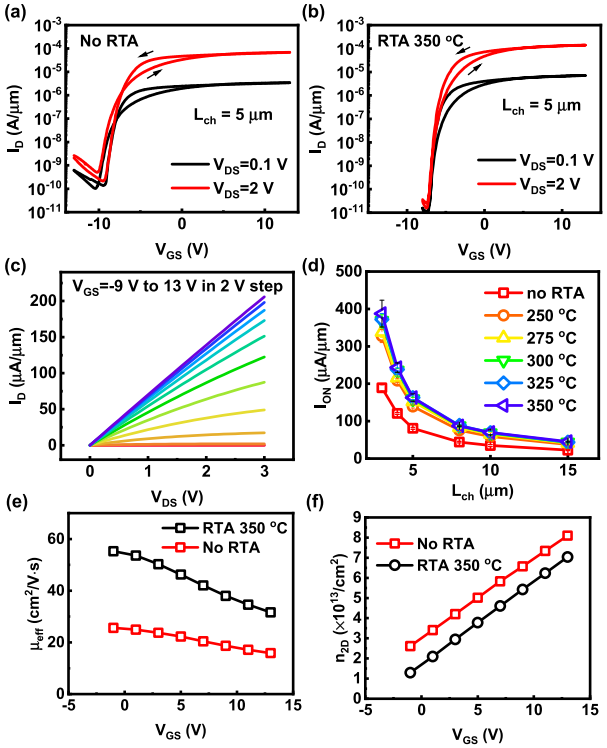

Fig. 2. I_D–V_{GS} characteristics of an ITO transistor with channel length of 5 μm. (a) As-fabricated without annealing and (b) with RTA at 350 °C for 30 s. (c) I_D–V_{DS} characteristics of the same ITO transistor as in (b). No current saturation is observed due to the thick gate dielectric. (d) I_{ON} (at V_{GS} = 13 V and V_{DS} = 2 V) versus channel length of ITO transistors without RTA and with 30 s RTA from 250 °C to 350 °C in 25 °C step. ON-current is improved significantly by RTA. (e) μ_{eff} and (f) n_{2D} versus V_{GS} and of ITO transistors without RTA and with RTA at 350 °C for 30 s. Mobility of ITO channel is improved significantly by RTA. ITO transistor with RTA has smaller carrier density at the same V_{GS} due to V_T shift. Carrier density >0.8 × 10^{14}/cm^2 is achieved.

of ITO under source/drain (S/D) ohmic contacts is 10 nm. The thickness of ITO channel is recessed to 2 nm. 80-nm Ni is used for S/D electrodes. 50-nm SiO_2 under source/drain pad serves as field oxide to reduce the gate leakage current and prevent the polarization switching of FE HZO under S/D pads. Fig. 1(b) shows a false-colored scanning electron microscopy (SEM) image of a fabricated ITO transistor, capturing the ITO channel, Ni electrodes, and SiO_2 for isolation.

Fig. 1(c) shows the fabrication process flow of the ITO transistors. The device fabrication process started with solvent cleaning of p+ Si substrate. 20-nm HZO (Hf:Zr ratio = 1:1) and 3-nm Al_2O_3 were then deposited on p+ Si substrate by atomic layer deposition (ALD) at 200 °C. $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), $(CH_3)_3Al$ (TMA), and H_2O were used as the Hf, Zr, Al, and O precursors. The Al_2O_3 capping is adopted to enhance the FE polarization of HZO and protect HZO during the device processing. After rapid thermal annealing (RTA) at 400 °C in N_2 environment for 1 min, 10-nm ITO was deposited by RF sputtering with a composition of 90 wt% In_2O_3 and 10 wt% SnO_2. Channel isolation was done by wet etching of ITO using hydrochloric acid solution (HCl, 20%). 50-nm SiO_2 was then deposited by e-beam evaporation as field oxide to isolate the source/drain pads. 80-nm Ni was then deposited as S/D ohmic contacts. Diluted HCl solution (3.4%) was used for channel recess by wet etching. The fabricated devices were then annealed by RTA in N_2 for 30 s at various temperatures.

Fig. 1(d) shows *P*–*V* characteristics of Ni/ITO/3-nm Al_2O_3/20-nm HZO/p+ Si capacitor, showing clear FE *P*–*V* hysteresis loop, where the voltage is applied to the p+ Si electrode. *C*–*V* characteristics from 1 kHz to 1 MHz are show in Fig. 1(e), exhibiting a typical FE *C*–*V* hysteresis loop. Capacitance at negative voltages is smaller than positive voltage due to the depletion of the 10-nm ITO.

III. Results and Discussion

Fig. 2(a) shows the I_D–V_{GS} characteristics of an as-fabricated ITO transistor with channel length (L_{ch}) of 5 μm without RTA. Fig. 2(b) shows the I_D–V_{GS} characteristics of an ITO transistor with same L_{ch} of 5 μm and with RTA at 350 °C for 30 s. The ITO transistor after annealing has larger ON-current (I_{ON}), smaller OFF-current (I_{OFF}), higher on/off ratio, and smaller subthreshold slope (SS), compared with device without RTA, suggesting a reduced interface trap density after annealing. The ITO transistor after annealing also shows a clean counterclockwise I_D–V_{GS} hysteresis loop, as a result of FE polarization switching. The cross of clockwise and counterclockwise loop in the I_D–V_{GS} of ITO transistor without RTA in Fig. 2(a) partly comes from interface trap effect [8], indicating RTA can effectively reduce the interface trap density in ITO transistors. Fig. 2(c) shows I_D–V_{DS} characteristics of the same ITO transistor as in Fig. 2(b). A high I_{ON} of 0.21 A/mm is achieved even on this L_{ch} = 5 μm long channel device. Statistical comparison of I_{ON} (at V_{GS} = 13 V and V_{DS} = 2 V) versus L_{ch} of ITO transistors without RTA

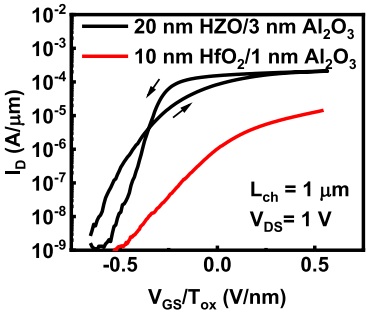

Fig. 3. Comparison of I_D versus V_{GS}/T_{ox} characteristics of ITO transistors with FE HZO or dielectric HfO_2 as gate insulator, without annealing and with $L_{ch} = 1$ μm at $V_{DS} = 1$ V. FE polarization is needed to switch on and off the ITO channel.

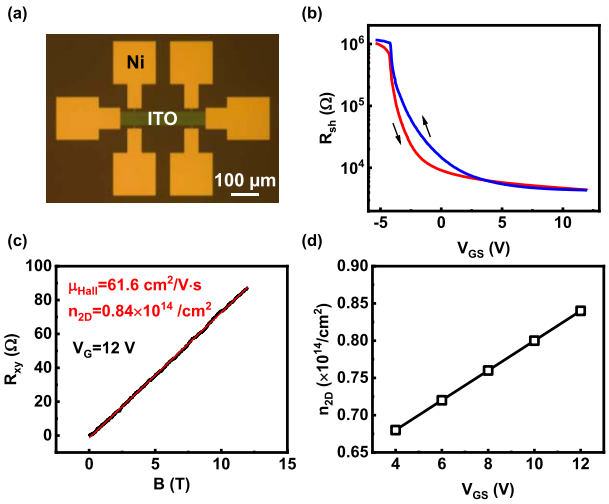

Fig. 4. (a) Hall bar structure in the experiments. (b) Sheet resistance versus gate voltage in Hall measurement at cryogenic temperature. (c) R_{xy} versus B-field in Hall measurement of the same device as in (b). Switching of high carrier density of 0.84 $\times$ 10^{14}/cm^2 is achieved at cryogenic temperature. (d) Carrier density versus gate voltages in Hall measurement.

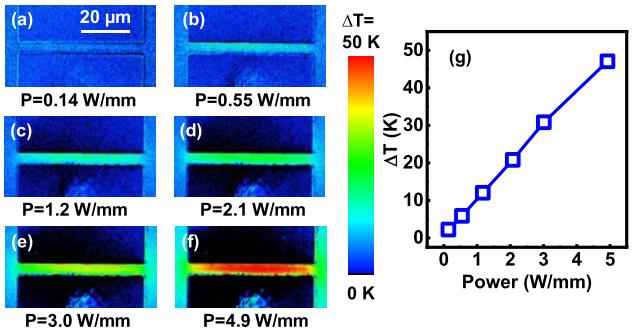

Fig. 5. (a)–(f) Temperature increase map of channel region at different power of an ITO transistor by thermo-reflectance imaging. (g) Temperature increase versus power characteristics of the same thermo-reflectance imaging measurement.

and with 30 s RTA from 250 °C to 350 °C in 25 °C step are summarized in Fig. 2(d), where each data point is the average of at least five devices. ON-current is found to improve significantly by RTA.

Fig. 2(e) compares the effective mobility (μ_{eff}) versus V_{GS} of ITO transistors without RTA and with RTA at 350 °C for 30 s, extracted from I–V characteristics. Drain currents can be estimated according to $I_D = n_{2D} q \mu E$, where n_{2D} is the 2-D carrier density, q is the elementary charge, μ is the mobility, and E is the source to drain electric field. E is estimated as V_{DS}/L_{ch} due to the long channel and low V_{DS} of 0.1 V. Fig. 2(f) shows the n_{2D} versus V_{GS} calculation of ITO transistors without RTA and with RTA at 350 °C for 30 s, according to this equation. A high-density 2-D electron gas over 0.8 $\times$ 10^{14}/cm^2 is the simple estimation of n_{2D} highly depending on the accuracy of mobility extraction. The extraction of mobility here does not consider the impact of contact resistance and interface/bulk traps so that mobility may be underestimated and carrier density may be overestimated. Hall measurement discussed next is a more accurate proof of carrier density in ITO transistors. It can be seen that the mobility of ITO channel is improved significantly by RTA, while carrier density is reduced slightly due to the threshold voltage (V_T) shift. Therefore, the drain current enhancement by RTA is mostly benefited by mobility improvement to as high as 55 cm^2/Vs, much higher than the previously reported mobility value [8].

Fig. 3 shows the comparison of I_D versus V_{GS}/T_{ox} characteristics of ITO transistors with FE HZO or dielectric HfO_2 as gate insulator, where T_{ox} is the gate oxide thickness, which clearly indicates field effect is not as effective as FE polarization to modulate the ITO channel. FE polarization is needed to achieve high drain current in the ITO transistors in this work. Similar comparison was also reported in [8].

To directly measure n_{2D} of the ITO transistors, Hall measurements were performed to characterize the carrier density at cryogenic temperatures. Fig. 4(b) shows the sheet resistance (R_{sh}) versus V_{GS} measured from Hall bar structure [Fig. 4(a)], showing the device can be switched on and off. Fig. 4(c) shows R_{xy} versus B-field at $V_{GS} = 12$ V in Hall measurement of the same device as in Fig. 4(b). Switching of ultrahigh-density 2-D electron gas of 0.84 $\times$ 10^{14}/cm^2 is confirmed by Hall measurement. Fig. 4(d) shows n_{2D} versus V_{GS} in Hall measurement of the same device as in Fig. 4(b), showing the effect of gate modulation.

The self-heating effect is evaluated to study the impact of high carrier density on thermal dissipation [20]. Fig. 5(a)–(f) shows the temperature increase (ΔT) map and ΔT versus power characteristics of ITO channel region at different power by a thermo-reflectance imaging. ΔT of 47 K is achieved at a high power of 4.9 W/mm.

To understand the origin of the high-density 2-D electron gas in the ITO transistor with FE gating, a PUND measurement is performed. Fig. 6(a) illustrates the measurement setup and pulse sequence. S/D is connected to the ground and the PUND voltage signal is applied to the gate. HZO under both S/D contact and channel can trigger FE switching in the PUND measurements and the impact of area under S/D needs to be eliminated from the measurements, as shown in Fig. 6(b). An experimental PUND voltage signal is shown in Fig. 6(c). A negative preset voltage pulse is first applied to polarize

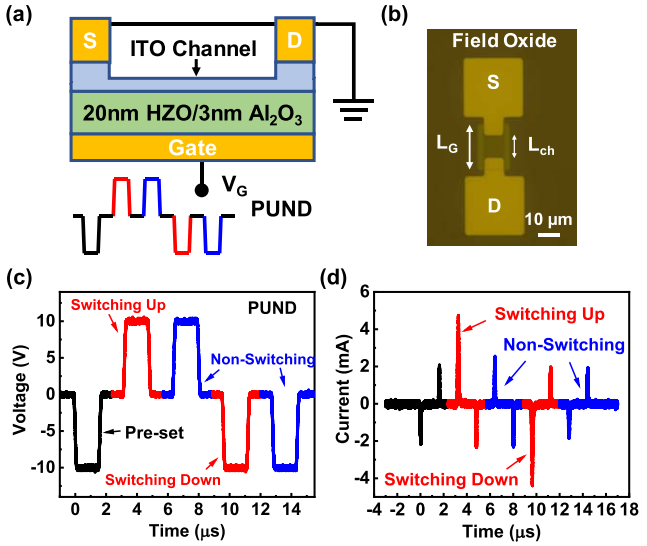

Fig. 6. (a) Illustration of PUND measurement on ITO transistor. The thickness of ITO under source/drain is 10 nm, while ITO channel is 2 nm. (b) Photograph image of a fabricated ITO transistor. The gate length (L_G) and channel length (L_{ch}) are different, where the impact of overlap area needs to be eliminated from the measurements. Experimental PUND (c) voltage and (d) current signals, including the preset pulse, switching pulse, and nonswitching pulse.

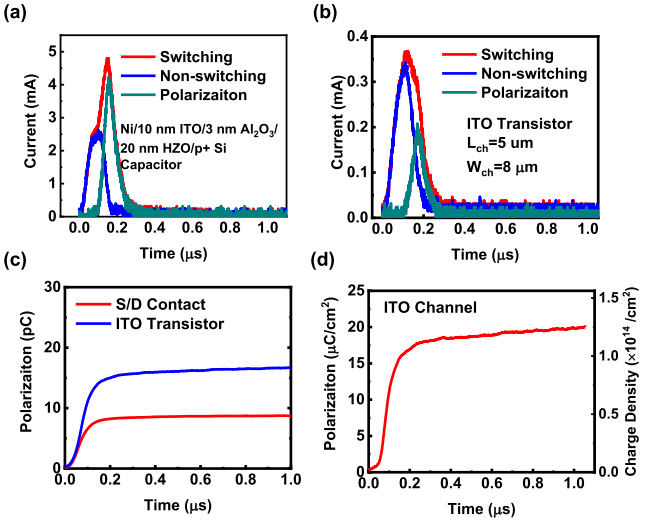

Fig. 7. Transient switching current response, nonswitching current response, and the polarization switching current of (a) a Ni/10-nm ITO/3-nm Al_2O_3/20-nm HZO/p+ Si capacitor and (b) ITO transistor with channel length of 5 μm and channel width of 8 μm. (c) Transient polarization charge of S/D contacts and ITO transistor achieved from the integration of transient polarization switching currents. The transient polarization charges of S/D contacts are calculated according to S/D contact area. (d) Transient polarization charge density of the channel of ITO transistor. High polarization switching of charge density $>1 \times 10^{14}$ is achieved, which contribute to the high carrier density $>0.8 \times 10^{14}$ in ITO channel.

down the FE HZO. Then, a positive switching voltage pulse is applied to switch up the FE HZO, leading to a large switching current response, as show in Fig. 6(d). Then, a second positive nonswitching voltage pulse is applied to measure the charging of dielectric components. Therefore, FE polarization switching can be extracted and charging due to the dielectric components has no contribution to the polarization measurement results. Another two negative voltage pulses are applied to measure the polarization switching down response. This method and setup are discussed in great details in previous work [15].

Fig. 7(a) shows the transient switching current response, nonswitching current response, and the polarization switching current of a Ni/10-nm ITO/3-nm Al_2O_3/20-nm HZO/p+ Si capacitor. This structure is the same as the stack in S/D ohmic contacts region. Fig. 7(b) shows the transient switching current response, nonswitching current response, and the polarization switching current of ITO transistor with L_{ch} of 5 μm and channel width of 8 μm. Note that the nonswitching components here are relatively larger because of the charging of the area under test pads, the impact of which is eliminated in the polarization switching current by PUND. The total polarization switching here includes both from the S/D contacts and channel. By subtracting polarization charge in S/D contact region from the total polarization switching [as shown in Fig. 7(c)], the transient polarization switching in ITO channel region can be obtained, as shown in Fig. 7(d). A polarization charge switching over 10^{14}/cm^2 is obtained, which is larger than n_{2D} of ITO channel in transport. The extra charges are trapped at the HZO/Al_2O_3 interface and bulk trap states to compensate the charge balance [14], [17]–[19] and not contribute to transport charges. Therefore, the FE polarization can induce ultrahigh-density electron charges in ITO because

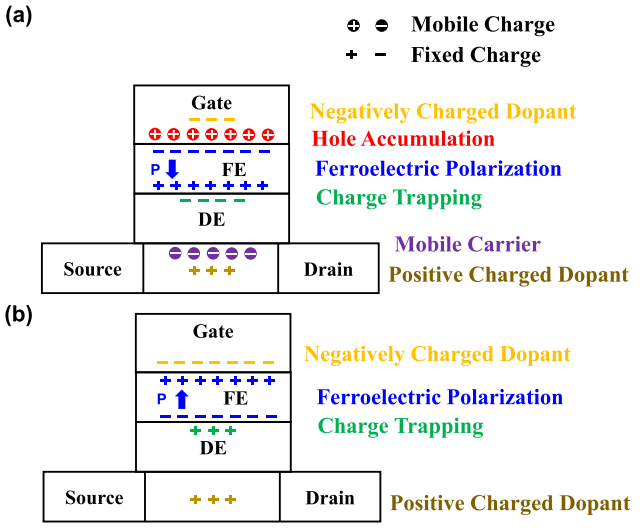

Fig. 8. Charge balance in a Fe-FET with FE/DE stack as gate insulator in polarization (a) down and (b) up states.

the trap density at HZO/Al_2O_3 and Al_2O_3/ITO interfaces is relatively low compared with the mobile carrier density and the FE polarization charge density.

Here, an in-depth analysis on the charge balance of Fe-FET with FE/ dielectric (DE) stack as gate insulator is provided. The charge components of a metal/FE/DE/semiconductor system include: 1) hole accumulation in the p+ Si gate electrode; 2) negatively charged dopants in the p+ Si gate electrode (therefore, gate electrode can be negatively charged due to depletion); 3) FE polarization; 4) charge trapping, for example, at FE/DE interface; 5) mobile electrons in semiconductor

channel; and 6) positively charged dopants in semiconductor channel (oxygen vacancies in ITO in this work). These are the charge sources providing the essential charge balance, as shown in Fig. 8. In polarization down state: 1) gate electrode is positively charged due to hole accumulation; 2) channel is negatively charged due to mobile electrons; and 3) FE/DE interface is negatively charged by charge trapping (so that DE layer is not broken down by high polarization charge density [14]). In polarization up state: 1) gate electrode is negatively charged due to dopants in the space charge region; 2) channel is positively charged due to positively charged dopants and the depletion of mobile electrons; and 3) FE/DE interface is positively charged by charge trapping. Mobile carriers and positively charged dopants in semiconductor channel are not sufficient to balance the polarization charge density $>10^{14}/\text{cm}^2$. Therefore, charge trapping at FE/DE interface must exist. And because of the charge trapping or the leakage-assisted switching mechanism [14], the memory window or threshold voltage of FeFETs cannot be simply understood by coercive voltages in P–V curve.

IV. Conclusion

In conclusion, a BEOL compatible ITO transistor with high-density 2-D electron gas over $0.8 \times 10^{14}/\text{cm}^2$ at the HZO/ITO oxide/oxide interface is demonstrated. Such high-density 2-D electron gas is induced by the FE polarization and can be switched on and off by FE polarization switching, resulting in high mobility, high ON-current, and high on/off ratio ITO transistors. The large tunable 2-D electron gas density by FE polarization provides a viable route to realize high charge density transistors with high on/off ratio, which can be potentially employed for superconducting devices and nonvolatile memory devices. More importantly, the ALD FE hafnium oxides and sputtered ITO thin films are fully compatible with Si CMOS BEOL process, unlike other approaches such as ion liquid gating, so that massive production is achievable.

References

[1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, "Back-end-of-line compatible transistors for monolithic 3-D integration," *IEEE Micro*, vol. 39, no. 6, pp. 8–15, Nov. 2019, doi: 10.1109/MM.2019.2942978.

[2] M. Si *et al.*, "Why In_2O_3 can make 0.7 nm atomic layer thin transistors," *Nano Lett.*, vol. 21, no. 1, pp. 500–505, 2021, doi: 10.1021/acs.nanolett.0c03967.

[3] M. Si, Z. Lin, A. Charnas, and P. D. Ye, "Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 v," *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 184–187, Feb. 2021, doi: 10.1109/LED.2020.3043430.

[4] M. Si, A. Charnas, Z. Lin, and P. D. Ye, "Enhancement-mode atomic-layer-deposited In_2O_3 transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 v by low-temperature annealing and stability in hydrogen environment," *IEEE Trans. Electron Devices*, early access, Jan. 29, 2021, doi: 10.1109/TED.2021.3053229.

[5] T. Miyasako, M. Senoo, and E. Tokumitsu, "Ferroelectric-gate thin-film transistors using indium-tin-oxide channel with large charge controllability," *Appl. Phys. Lett.*, vol. 86, no. 16, Apr. 2005, Art. no. 162902, doi: 10.1063/1.1905800.

[6] A. Lu, J. Sun, J. Jiang, and Q. Wan, "One-shadow-mask self-assembled ultralow-voltage coplanar homojunction thin-film transistors," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1137–1139, Oct. 2010, doi: 10.1109/LED.2010.2061834.

[7] S. Li *et al.*, "Nanometre-thin indium tin oxide for advanced high-performance electronics," *Nature Mater.*, vol. 18, no. 10, pp. 1091–1097, Oct. 2019, doi: 10.1038/s41563-019-0455-8.

[8] M. Si *et al.*, "Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating," *ACS Nano*, vol. 14, no. 9, pp. 11542–11547, Sep. 2020, doi: 10.1021/acsnano.0c03978.

[9] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, "BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with I_{on} = 370μA/μm, SS = 73mV/dec and I_{on}/I_{off} ratio > 4×10^9," in *Proc. Symp. VLSI Technol.*, vol. 2020, pp. 1–2.

[10] S. Samanta, K. Ran, C. Sun, C. Wang, A. Voon-Yew Thean, and X. Gong, "Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high $G_{m.Max}$ of 125 μS/μm at VDS of 1V and ION of 350 μA/μm," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[11] J. Wu, F. Mo, T. Saraya, T. Hiramoto, and M. Kobayashi, "A monolithic 3D integration of RRAM array with oxide semiconductor FET for in-memory computing in quantized neural network AI applications," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[12] H. Fujiwara, Y. Sato, N. Saito, T. Ueda, and K. Ikeda, "Surrounding gate vertical-channel FET with gate length of 40 nm using BEOL compatible high-thermal-tolerance in-al-zn oxide channel," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[13] J. Müller *et al.*, "Ferroelectricity in simple binary ZrO2 and HfO2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, Aug. 2012, doi: 10.1021/nl302049k.

[14] M. Si, X. Lyu, and P. D. Ye, "Ferroelectric polarization switching of hafnium zirconium oxide in a ferroelectric/dielectric stack," *ACS Appl. Electron. Mater.*, vol. 1, no. 5, pp. 745–751, May 2019, doi: 10.1021/acsaelm.9b00092.

[15] M. Si *et al.*, "Ultrafast measurements of polarization switching dynamics on ferroelectric and anti-ferroelectric hafnium zirconium oxide," *Appl. Phys. Lett.*, vol. 115, no. 7, Aug. 2019, Art. no. 072107, doi: 10.1063/1.5098786.

[16] X. Lyu, M. Si, X. Sun, M. A. Capano, H. Wang, and P. D. Ye, "Ferroelectric and anti-ferroelectric hafnium zirconium oxide: Scaling limit, switching speed and record high polarization density," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. T44–T45, doi: 10.23919/VLSIT.2019.8776548.

[17] K. Toprasertpong, M. Takenaka, and S. Takagi, "Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and hall techniques?: Revealing FeFET operation," in *IEDM Tech. Dig.*, Dec. 2019, pp. 570–573, doi: 10.1109/IEDM19573.2019.8993664.

[18] M. Si, Z. Lin, J. Noh, J. Li, W. Chung, and P. D. Ye, "The impact of channel semiconductor on the memory characteristics of ferroelectric field-effect transistor," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 849–864, 2020, doi: 10.1109/JEDS.2020.3012901.

[19] H. W. Park, J. Lee, and C. S. Hwang, "Review of ferroelectric field-effect transistors for three-dimensional storage applications," *Nano Select*, pp. 1–21, Jan. 2021, doi: 10.1002/nano.202000281.

[20] R. Chavez *et al.*, "Thermoreflectance imaging of percolation effects and dynamic resistance in indium tin oxide nanoparticle layers," *J. Appl. Phys.*, vol. 112, no. 8, Oct. 2012, Art. no. 083705, doi: 10.1063/1.4757960.