0.1-µm InAlN/GaN High Electron-Mobility Transistors for Power Amplifiers Operating at 71–76 and 81–86 GHz: Impact of Passivation and Gate Recess

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Abstract—We have developed 0.1-µm gate-length InAlN/GaN high electron-mobility transistors (HEMTs) for millimeter-wave (MMW) power applications, particularly at 71–76 and 81–86 GHz bands. The impacts of depth and width of the gate recess groove on electrical performance have been analyzed and compared. Competing passivation technologies, atomic layer deposition (ALD) aluminum oxide ($\text{Al}_2\text{O}_3$) and plasma-enhanced chemical vapor deposition (PECVD) SiN, have also been assessed in terms of dc, pulsed-$I_\text{V}$, and high-frequency characteristics. It has been found that while PECVD SiN-passivated HEMTs and the monolithic microwave integrated circuits (MMICs) demonstrating an output power ($P_{\text{out}}$) of 1–2 W and a power added efficiency (PAE) of 6%–19% in the frequency range of 76–96 GHz [1]–[4]. As a new contender for next-generation millimeter-wave (MMW) PAs, the HEMT based on InAlN/GaN heterojunction, lattice matched to SiC substrate, has recently generated a lot of interest. This is largely due to its high sheet carrier density that would allow more aggressive gate-length scaling without excessive compromise in aspect ratio, excellent thermal stability as reported in [5] and [6], and the resulting potential reliability advantage as well. Some encouraging progress has been made; for instance, InAlN/GaN HEMTs have shown good power performance at 30–40 GHz [7]–[9]. The key to achieving excellent power performance in the MMW range is to address the conflict between the thinner gate layer required by the short gate length needed for high-frequency operation and the increasingly adverse impact of surface traps on the current-carrying channel layer. Apparently, the most straightforward strategy is to protect the surface of the InAlN/GaN HEMT properly so that trapping effects would be less pronounced [10]–[12] or to keep the channel sufficiently away from the surface to minimize the impact.

In this paper, we will report the short gate-length InAlN/GaN HEMTs developed for PAs targeting E-band (71–76 and 81–86 GHz) applications. A gate length of 0.1 µm has been selected to meet the requirement of high operating frequency while keeping short channel effects to a minimum. Atomic layer deposition (ALD) aluminum oxide ($\text{Al}_2\text{O}_3$) and plasma-enhanced chemical vapor deposition (PECVD) SiN have been evaluated and compared as competing passivation technologies. Meanwhile, the use of a gate recess process has also been investigated as an important technical solution to improving the power performance of InAlN/GaN HEMTs. This is because gate recess etching would allow the adoption of a thicker top barrier for devices while still maintaining an excellent aspect ratio by placing the gate electrode sufficiently close to the channel.
II. Fabrication Technology

The 0.1-μm InAlN/GaN HEMTs were fabricated based on the InAlN/GaN heterostructure grown by metalorganic chemical vapor deposition on 4-in semi-insulating SiC substrates. The epitaxial structure includes a thin AlN nucleation layer, an undoped AlGaN buffer, an undoped GaN channel layer less than 100 nm, a nominally 1-nm undoped AlN layer, and a nominally 5-nm undoped InAlN gate layer with 17% indium. The device has a source–drain spacing of 2 μm, and the 0.1-μm Γ-gate is placed at about 0.5 μm from the source. For recessed devices, BCl3 plasma was used to remove about 3-nm recess InAlN barrier layer before the gate metallization, thus reducing the gate-to-channel distance to 3 from 6 nm. More details on the fabrication process can be found in [13]. To further enhance the MMW performance, the SiC substrate is thinned down to 2 mil, enabling the fabrication of 15 μm × 25 μm slot via holes for realizing low inductance and more compact devices to facilitate MMW MMIC design [14].

Three wafers have been included for this paper: Wafer A was passivated with ALD Al2O3 as described in [15], while Wafers B and C were passivated with PECVD SiN. The thicknesses of dielectric passivation films for Wafers A and B differ by approximately 5%; the passivation layer on Wafer C is approximately 30% thinner than Wafer B. The total thicknesses of passivation layers are below 100 nm for all the three wafers in order to extract more gain from devices for operation at E-band. Meanwhile, for each of the three wafers, two types of devices were fabricated:

1) the unrecessed, whose epitaxial layer was not recess etched before the gate metal deposition;
2) the recessed, which was etched both vertically (∼3 nm) and laterally using BCl3 plasma before the gate metallization onto the InAlN layer.

While the lateral recess widths are comparable to the gate length of devices for all the three wafers, Wafer A has the widest recess groove; in comparison, the recess widths of Wafers B and C are about 20% and 30% smaller, respectively.

Also included in the discussion is a special type of device, which was recessed only vertically under the gate without a lateral etching. This is to facilitate the analysis of the individual impact of vertical and lateral recess on the electrical performance of the devices.

III. Device Results and Discussion

A. Output and Transfer Characteristics

Generally speaking, the passivation technique does not result in an apparent difference in dc characteristics. Fig. 1(a) and (b) is the IV and transfer characteristics of the Al2O3-passivated (Wafer A, dotted lines) and SiN-passivated HEMTs (Wafers B and C, plotted with solid and dashed lines, respectively) without gate recess. The Al2O3-passivated device shows a maximum drain current (I_max) of about 1.8 A/mm at a gate bias Vgs of 1 V and a drain bias Vds of 10 V, a few percentage points higher than those of the SiN-passivated devices. In addition to the same sharp pinch off characteristics, similar maximum extrinsic transconductances (g_max) as high as 770, 745, and 755 mS/mm, which are within a range of approximately 3%, have been achieved for the Al2O3-passivated and SiN-passivated devices on Wafers A, B, and C, respectively, at a Vds of 10 V.

A comparison of the transfer characteristics of the unrecessed Al2O3- and SiN-passivated devices at different drain biases indicates that these two passivation technologies hardly change their scaling behaviors. For example, devices on Wafers A and B display not only a similarly small Vpo shift of about 340 and 330 mV when Vds is increased from 2 to 10 V, but also a similarly low subthreshold swing of 111 and 94 mV/decade at Vds = 2 V and 122 and 102 mV/decade at Vds = 10 V, as well as a similarly low drain-induced barrier lowering of 60 and 52 mV/V at Vds = 4 V and 42 and 43 mV/V at Vds = 10 V, respectively.

In Fig. 2, the recessed devices on Wafers B and C show a very similar I_max of about 1.6 A/mm at Vgs = 2 V and Vds = 10 V and g_max of about 940 S/mm. Wafer A, however, shows a 20% lower I_max, primarily due to its deeper etching.
in comparison with the other two wafers. The slightly deeper etching is also largely responsible for the approximate 0.85 V increase in \( V_{gs} \). This difference is largely due to the process variation as it was etched with nominally the same recipe, giving rise to a 2-nm gate-to-channel distance for the recessed devices on this wafer.

### B. Breakdown Voltage

In Fig. 3, the unrecessed device of Wafer A typically has an off-state breakdown voltage \( BV \), defined as the gate–drain voltage at which a gate current \( I_g \) of 1 mA/mm is reached with the source electrode floating, of about 50 V before passivation. With the gate recess, the device shows a BV slightly over 60 V.

This BV increase with lateral recess width is similar to that of GaAs- and InP-based HEMTs, with enhanced BV resulting from an enlarged lateral recess. However, the above relatively high BV of InAlN/GaN HEMTs would largely disappear after the passivation layer is deposited. Furthermore, the devices with SiN passivation (e.g., Wafer C as shown in Fig. 3) actually exhibited a similar degradation in BV after the passivation process, essentially coinciding with their \( Al_2O_3 \)-passivated counterparts; this is attributed to the conduction path at the interface between the InAlN surface and the passivation layers.

It can also be noted that the recessed \( Al_2O_3 \)-passivated device shows several volts higher BV than the unrecessed one. This small difference between the recessed and unrecessed devices also holds true for their SiN-passivated counterparts on Wafer B, indicating the contribution of lateral recess to higher BV.

It is apparent that there is a need to enhance the breakdown voltage of the InAlN/GaN HEMTs so that they can deliver higher output power at a higher bias or operate more reliably. The most straightforward approach is to modify the passivation process including the pretreatment process. However, this can be made complicated because any adjustment to the passivation would have an impact not only on the breakdown but also on pulsed-\( IV \).

### C. Pulsed-\( IV \) Characteristics

In addition to the passivation process, the lateral recess width shows a much more pronounced impact on the pulsed drain current level as well as its collapse, in particular at a relatively low \( V_{ds} \) ranging from 2.5 to 5 V. For the two SiN-passivated wafers, it can also be noted that the device on Wafer C shows a slightly larger current collapse than Wafer B in the low \( V_{ds} \) regime, which can probably be traced back to its thinner passivation layer, as mentioned in Section II.

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the devices in Fig. 6 all have the same lateral recess width (of zero) as they are only vertically recessed. Clearly as a result, it is the lateral recess width, rather than the vertical recess depth, that is the leading factor in determining the pulsed-IV characteristics. It would be even more revealing to compare the devices in Fig. 6 with their counterparts with lateral recess in Fig. 5: All devices in Fig. 6 without lateral recess have higher pulsed drain currents than their recessed counterparts in Fig. 5 to a varied degree depending on the lateral recess width, no matter how deep the gate recess is.

Not surprisingly, a more careful examination of the pulsed-IV shown in Fig. 6 further discloses that Wafer A has the smallest collapse in pulsed drain current, which further indicates that a better passivation is offered by the ALD Al₂O₃ film. In addition, Wafer C has shown a larger pulsed drain current collapse than Wafer B, which probably could be attributed, at least in part, to its thinner SiN passivation layer, similar to the unrecessed FET on Wafer C shown in Fig. 4(c).

Finally, it is also interesting to notice that $V_{po}$ can also be affected by the gate recess width if one compares devices in Fig. 5 and their counterparts in Fig. 6. It should be noted that the recessed devices with different lateral widths on the same wafer were recessed in the same etching run. Furthermore, the etching process was designed to be performed in self-limiting cycles so that the variation in depths of recess grooves due to either sizes or locations would be minimized. As a result, good uniformity in the recess depth can be achieved, leading to $V_{po}$ standard deviations typically smaller than 150 mV across 4-in wafers for devices with the same topology. Therefore, the $V_{po}$ difference of approximately 0.7 V between the corresponding pairs of devices in Figs. 5 and 6 cannot be fully explained only with the variation in the recess depth as one would intuitively do at the first glimpse; we would attribute the above observed $V_{po}$ difference, at least in part, to the difference in recess width. Similar phenomena were actually reported in InAlAs/InGaAs HEMTs previously [16], [17], which was attributed to the interface traps affecting the sheet carrier density in the channel. In GaN HEMTs, traps are both higher in density and closer to the channel when not passivated properly, and thus have a much more significant influence on the density of the 2DEG channel in comparison with HEMTs based on InAlAs/InGaAs or AlGaAs/InGaAs heterojunctions grown on InP or GaAs substrates. The increased parasitic access resistances resulting from both the lowered sheet carrier density and the enlarged width of the lateral recess areas would be likely to reduce the voltage drop that is actually applied to the intrinsic transistor including the gate and its fringing areas, thus contributing to $V_{po}$ values as shown in Fig. 5 more positive than those of their counterparts without lateral recess as shown in Fig. 6.

D. Small-Signal Characteristics

Fig. 7 shows the current and power gains obtained from on-wafer S-parameter measurement on $2 \times 35 \mu m$ unrecessed devices on Wafers A, B, and C over the frequency of 0.5–110 GHz when biased at a $V_{ds}$ of 10 V and a drain current of 500 mA/mm. All the three HEMTs show a similar current gain cutoff frequency of about 100 GHz and a maximum

![Fig. 5. Pulsed-IV characteristics for recessed 0.1-μm InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The devices were measured at quiescent points of $V_{gs} = 0$ V and $V_{ds} = 0$ V (open symbols) and $V_{gs} = -5$ V and $V_{ds} = 10$ V (solid symbols). The $V_{gs}$ for the top curves is 2 V and the $V_{ds}$ step is -1 V for all devices. The pulsed drain current was measured with 200-ns pulse width and 2-ms separation.](image)

![Fig. 6. Pulsed-IV characteristics for 0.1-μm InAlN/GaN HEMTs with only vertical gate recess on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The devices were measured at quiescent points of $V_{gs} = 0$ V and $V_{ds} = 0$ V (open symbols) and $V_{gs} = -5$ V and $V_{ds} = 10$ V (solid symbols). The $V_{gs}$ for the top curves is 2 V and the $V_{ds}$ step is -1 V for all devices. The pulsed drain current was measured with 200-ns pulse width and 2-ms separation.](image)
Fig. 7. Current gain and power gain over 0.5–110 GHz for unrecessed 0.1-\( \mu \)m InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The measurement was performed at a \( V_{ds} \) of 10 V and a drain current of 500 mA/mm on 2 \times 35 \( \mu \)m devices on all the three wafers.

Fig. 8. MAG at 86 GHz as a function of the drain current for unrecessed (solid lines) and recessed (dashed lines) 0.1-\( \mu \)m InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The measurement was performed at a \( V_{ds} \) of 10 V on 2 \times 35 \( \mu \)m devices on all the three wafers.

oscillation frequency of approximately 200 GHz. A more careful examination of the maximum available gain (MAG), however, reveals that Wafers B and C have about 0.3 dB lower and 0.2 dB higher MAG than Wafer A at 86 GHz under the above bias condition, respectively.

To better evaluate the impact of passivation and gate recess on the small-signal power gain, we have plotted the MAG at 86 GHz as a function of the drain current for unrecessed (solid lines) and recessed (dashed lines) 0.1-\( \mu \)m InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The measurement was performed at a \( V_{ds} \) of 10 V on 2 \times 35 \( \mu \)m devices on all the three wafers.

Several PAs have been designed for optimum output power performance operating at 71–76 and 81–86 GHz with the 0.1-\( \mu \)m InAlN/GaN HEMTs discussed in the previous sections. Their performance has been summarized in Table I and compared with those of the state-of-the-art PAs reported in the past a few years, which are exclusively powered by HEMTs based on AlGaN/GaN heterojunction.

First, the two-stage balanced amplifier based on the unrecessed HEMTs on Wafer A with ALD-Al\(_2\)O\(_3\) passivation demonstrates a \( P_{out} \) of 1.43 W with an associated PAE of 12.7% at 86 GHz at a 1.5-dB gain compression (where the amplifier is not being driven fully into compression due to limitations of the test setup). This performance is better than the 1.3 W and 6% at 75 GHz of a three-stage PA in [1], comparable to the 0.84 W and 14.7% at 88 GHz of a three-stage PA in [2], as well as the 1.7 W and 11% at 91 GHz of a three-stage PA optimized for high power in [3]; it has lower output power and PAE than that reported in [4], which is a three-stage PA based on 0.14-\( \mu \)m AlGaN/GaN HEMTs with regrown GaN cap for ohmic electrodes with 1-\( \mu \)m spacing.

The performance of this MMIC PA based on unrecessed ALD-Al\(_2\)O\(_3\)-passivated devices also compares favorably with that of the PA that has the same design and unrecessed devices but with SiN passivation on Wafer C, showing about 15% higher \( P_{out} \) (even less compressed by more than 1 dB), more than 2% points higher PAE, and approximately 0.6 dB higher gain. Given the comparable device small-signal equivalent circuits as well as the optimum load impedances for the
above devices with different passivation processes, this MMIC performance comparison can be further interpreted as evidence for the advantage of adopting ALD Al$_2$O$_3$ as the passivation layer at the first order.

When the devices were recessed both vertically and laterally, however, the same two-stage $E$-band amplifier based on SiN passivation devices on Wafer C would show markedly enhanced power performance at 86 GHz. Its $P_{\text{out}}$ of 1.63 W and PAE of 15% are not only approximately 30% and 4.5% points higher than the PA based on unrecessed devices on the same wafer, but also 15% and 2.3% points higher than the PA based on ALD-Al$_2$O$_3$-passivated unrecessed HEMTs on Wafer A. Probably, this should not be a surprise, given its enhanced gain resulting from the gate recess, as well as the excellent pulsed-$IV$ that is effectively retained due to its relatively narrow lateral recess.

In addition, two PAs operating at 71–76 GHz have also been designed with the 0.1-$\mu$m InAlIn/GaN HEMTs. Despite limitations of the test setup, the single-ended PA based on unrecessed ALD-Al$_2$O$_3$-passivated devices shows a $P_{\text{out}}$ of 0.98 W at 76 GHz, which results in a high power density of 1.75 W/mm, essentially attaining the same power density achieved in [4]. The balanced PA version also shows a respectable $P_{\text{out}}$ of 1.4 W at 76 GHz. With the expected power performance improvement with a more accurate device model and enhanced breakdown voltage, it can be expected that the InAlN/GaN HEMT would be a very promising device technology for power application at $E$-band and beyond.

V. CONCLUSION

We have investigated the impacts of passivation and gate recess on the electrical performance of InAlN/GaN HEMTs, in particular, dc characteristics, pulsed-$IV$, small signal gains, and the resulting power performance of MMIC PAs at $E$-band. The ALD-grown Al$_2$O$_3$ appears to offer better passivation to the InAlN surface for enhanced power performance than PECVD SiN. However, the latter still offers acceptable passivation for InAlN and turns out to be very competitive when coupled with a properly designed gate recess groove and SiN thickness. The first-pass results of several PAs at 71–76 and 81–86 GHz clearly show the potential of InAlN/GaN HEMT technology for PAs at 71–110 GHz.

ACKNOWLEDGMENT

The authors would like to thank R. Carnevale and R. Isaak for layout, J. Pare, L. Schlesinger, S. Brun, M. Gerlach, D. Gallagher, J. Hulse, J. Kanjia, W. H. Zhu, and K. Tourigny for processing assistance, J. Lombardi and F. Ducharme for testing, and A. K. Stewart, S. Sweetland, and S. Powell for the program support.

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