# Comprehensive Study of Low-Frequency Noise Origins in Scaled Atomic-Layer-Deposited IGZO TFTs

Sumi Lee, *Graduate Student Member, IEEE*, Chang Niu, *Member, IEEE*, Chun-An Shih, *Graduate Student Member, IEEE*, Jian-Yu Lin, *Graduate Student Member, IEEE*, Zhuocheng Zhang, Yizhi Zhang, Linjia Long, Haiyan Wang, Muhammad A. Alam, *Fellow, IEEE*, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— In this work, we investigate the 1/*f* noise, i.e., low-frequency noise (LFN), characteristics of scaled atomic-layer-deposited indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) focusing on key factors such as: 1) varying indium (In) concentrations; 2) post-thermal annealing; and 3) channel length ($L_{ch}$) scaling. Increasing the In ratio from 2:1:1 to 7:1:1 enhances field-effect mobility ($\mu_{FE}$) from 11.2 to 36.6 cm$^2$/V and reduces LFN by up to 85%, demonstrating the role of In content in improving both electrical performance and noise characteristics. Post-annealing further mitigates LFN, achieving reductions of up to 68%, depending on the IGZO compositions. As $L_{ch}$ scales down, the dominant LFN mechanism shows a tendency to shift from mobility fluctuations ($\Delta\mu$) in long-channel devices ($L_{ch} = 1$ $\mu$m) to carrier number fluctuations ($\Delta$n) in short-channel devices ($L_{ch} =$ 50 nm), as indicated by the distinct dependence of normalized drain-current power spectral density ($S_{ID}/I_D^2$) on gate overdrive voltage. This behavior, supported by LFN measurements at elevated temperatures (~125 °C) and bias temperature instability (BTI) analyses, highlights the increasing influence of near-interface traps in scaled devices.**

***Index Terms*— 1/f noise, atomic layer deposition (ALD), bias temperature instability (BTI), indium–gallium–zinc oxide (IGZO), low-frequency noise (LFN), thin-film transistors (TFTs).**

## I. Introduction

THE relentless demand for higher performance and more energy-efficient electronics has driven extensive research into the miniaturization of semiconductor devices. As traditional planar architectures approach their physical and operational limits, the industry has increasingly turned toward 3-D structures and low-dimensional materials to sustain Moore's law and address scaling challenges [1], [2], [3]. Among these, amorphous oxide semiconductors, particularly indium–gallium–zinc oxide (IGZO), have emerged as promising candidates, offering high mobility, minimal OFF-state currents, and low operating voltages, which make them ideal for low-power and scaled monolithic 3-D integration [4], [5], [6], [7]. The precise thickness control and uniform film deposition achievable through atomic layer deposition (ALD) further enhances IGZO's integration into advanced transistor architectures, including gate-all-around and vertical devices, establishing ALD-deposited IGZO as a key material for next-generation electronics [8], [9], [10]. Despite these advantages, the high trap density inherent to the atomic structure of IGZO affects the interface and within the gate oxide, leading to device instabilities such as threshold voltage ($V_T$) shifts under elevated temperature and bias stress conditions [11], [12]. Therefore, further studies are crucial to address these challenges and enhance the reliability of IGZO as a channel material for scaled transistor applications.

Low-frequency noise (LFN) measurements have long been utilized as a nondestructive method for investigating near-channel gate oxide trap or channel surface trap properties in conventional field-effect transistors [13], [14], [15]. While numerous studies on the LFN characteristics of IGZO thin-film transistors (TFTs) have been reported since the early 2010s, most of the research has been limited to large devices with several micrometer-scale channel dimensions [16], [17], [18]. These studies primarily report absolute values of LFN by extracting Hooge's parameter ($\alpha_H$) under the mobility fluctuation model ($\Delta\mu$), which attributes noise to carrier scattering from channel defects [16], [17]. However, studies on LFN characteristics in highly scaled IGZO TFTs remain limited, and the impact of channel dimension scaling on LFN behavior is not yet fully understood. This knowledge gap necessitates a more detailed understanding of the mechanisms governing LFN in scaled IGZO TFTs.

This study aims to explore the LFN characteristics of scaled ALD IGZO TFTs, emphasizing the interplay between bulk and interface-related traps. By systematically varying the In:Ga:Zn composition and applying thermal annealing, we demonstrate

Received 17 February 2025; revised 3 March 2025; accepted 19 March 2025. This work was supported in part by Samsung Electronics and in part by the National Science Foundation CNS under Grant 2425498. The review of this article was arranged by Editor J.-S. Park. *(Corresponding author: Peide D. Ye.)*

Sumi Lee, Chang Niu, Chun-An Shih, Jian-Yu Lin, Zhuocheng Zhang, Linjia Long, Muhammad A. Alam, and Peide D. Ye are with the Birck Nanotechnology Center and Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Yizhi Zhang and Haiyan Wang are with the School of Materials Engineering, Purdue University, West Lafayette, IN 47907 USA.

Digital Object Identifier 10.1109/TED.2025.3562509

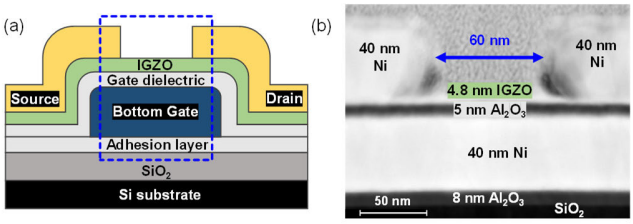


Fig. 1. (a) Device structure of a bottom-gate IGZO TFT fabricated on a Si/$SiO_2$ substrate. (b) Cross-sectional TEM image of IGZO FETs stack with a channel length of 60 nm.

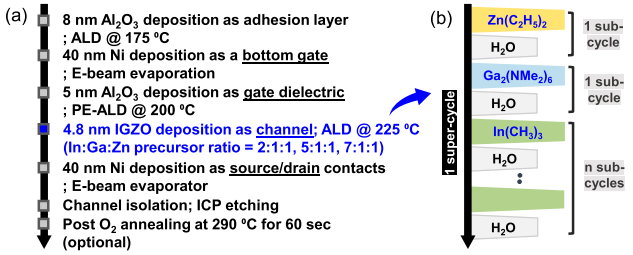


Fig. 2. (a) Key fabrication steps of ALD IGZO TFTs, where the fabrication temperature is kept below 300 °C and (b) illustration of the ALD deposition sequence for IGZO channel having different In:Ga:Zn compositions.

significant improvements in LFN performance, associated with reduced trap densities. Additionally, the study addresses the transition in dominant LFN mechanisms as channel dimensions scale down, employing appropriate models to analyze noise reduction mechanisms for each case. The findings provide insights for the design and optimization of IGZO TFTs to ensure reliable operation in manufacturing technology.

## II. Device Fabrication and Characterization

The bottom-gate IGZO TFTs were fabricated on SiO2/Si substrates with an additional ALD-grown 8-nm Al2O3 adhesion layer ensuring a smooth surface and enhanced adhesion, as shown in Fig. 1. A 40-nm Ni was deposited as the bottom gate using physical vapor deposition via e-beam evaporation. This is followed by the deposition of a 5-nm-thick $Al_2O_3$ gate dielectric using plasma-enhanced atomic layer deposition (PE-ALD) at 200 °C. As depicted in Fig. 2, the 4.8-nm-thick IGZO channel is deposited via ALD at 225 °C, using a supercycle that alternates individual subprecursor steps for In, Zn, and Ga, with $(CH_3)_3$ In (TMIn), $(C_2H_5)_2$Zn (DEZ), and $Ga_2(NMe_2)_6$ precursors. Throughout this article, the In:Ga:Zn ratio (e.g., 2:1:1, 5:1:1, and 7:1:1) denotes the subcycle ratios of each precursor distributed within the supercycle. Subsequently, an e-beam lithography process was then applied for the sharp liftoff of a 40-nm Ni layer to form source/drain contacts, and inductively coupled plasma (ICP) etching was employed to define the channel width ($W_{ch}$); the fabricated TFTs have a fixed $W_{ch}$ of 1 $\mu$m and a channel length ($L_{ch}$) ranging from 1 $\mu$m to 50 nm. Fig. 1(b) illustrates the cross-sectional transmission electron microscopy (TEM) image of the resulting IGZO TFT, with $L_{ch}$ of 60 nm. After fabrication, the devices underwent an annealing process at 290 °C in an oxygen environment for 60 s, which is known to alleviate $V_T$ roll-off in scaled devices and ensure enhancement-mode operation, to assess its effect on LFN performance [19].

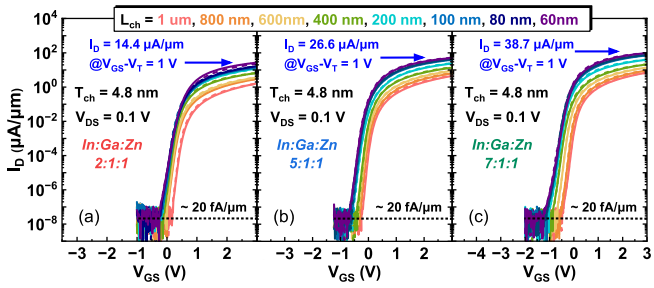


Fig. 3. Transfer characteristics ($I_D$–$V_{GS}$) of IGZO TFTs with varying channel lengths from 1 $\mu$m to 60 nm for each In:Ga:Zn ratio (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1, after oxygen annealing. The channel width ($W_{ch}$) and drain voltage ($V_{DS}$) are fixed at 1 $\mu$m and 1 V, respectively.

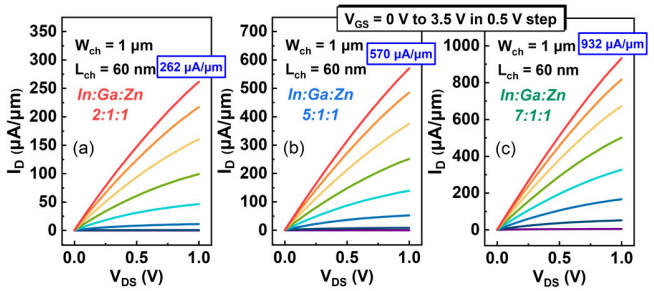


Fig. 4. Output characteristics ($I_D$–$V_{DS}$) of IGZO FETs with $V_{GS}$ ranging from 0 to 3.5 V in 0.5-V steps, measured for short-channel ($L_{ch}$ = 60 nm) devices, for each In:Ga:Zn ratio (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1.

The electrical measurements, including dc characteristics, were carried out using a Keysight B1500 system. The LFN characteristics were measured with a Keysight E4727A Advanced LFN Analyzer (A-LFNA), capable of detecting noise levels at a minimum frequency of 30 mHz, with WaferPro Express software.

## III. Results and Discussion

### A. DC Characteristics

Before discussing the LFN characteristics, this section examines how the In concentration in the IGZO film affects the electrical performance of IGZO TFTs. Fig. 3 presents the transfer characteristics ($I_D$–$V_{GS}$) of IGZO TFTs with varying $L_{ch}$ from 1 $\mu$m to 60 nm for each In:Ga:Zn ratio (i.e., 2:1:1, 5:1:1, and 7:1:1) after a 60-s oxygen annealing. The channel thickness ($T_{ch}$) and $W_{ch}$ are fixed as 4.8 nm and 1 $\mu$m, respectively. A higher In ratio in the IGZO channel correlates with a rise in drain current and lower $V_T$. For a fair comparison, the drain current under the same $V_{GS}$- $V_T$ and $V_D$ conditions is indicated in the figures. Furthermore, the output characteristics ($I_D$–$V_{DS}$) of short-channel devices ($L_{ch}$ = 60 nm) shown in Fig. 4 clearly demonstrate the trend of increasing ON-state current, attributed in part to the enhanced carrier density. The reduction of strong Ga–O bonds in the channel facilitates the formation of oxygen vacancies, acting as shallow donors, consequently boosting carrier density and decreasing $V_T$ (see Table I) [20].

In addition to the rise in drain current, a more pronounced $V_T$ roll-off is observed as the In concentration increases in the channel. To understand this phenomenon, it is important to recognize that $V_T$ roll-off primarily results from additional carriers generated under the source and drain contacts, which

TABLE I
SUMMARY OF ELECTRICAL PARAMETERS IN IGZO TFTs ACROSS DIFFERENT COMPOSITIONS

| In:Ga:Zn | 2:1:1 | | 5:1:1 | | 7:1:1 | |
|---|---|---|---|---|---|---|
| $L_{ch}$ (μm) | 1 | 0.06 | 1 | 0.06 | 1 | 0.06 |
| $V_T$ (V) | 2.08 | 1.50 | 1.52 | 0.97 | 1.11 | 0.26 |
| $\mu_{FE}$ ($cm^2$/Vs) | 11.2 | - | 29.9 | - | 36.6 | - |
| $g_m$ (μS/μm) @$V_{DS}$ = 1V | 8.71 | 119 | 26.9 | 247 | 36.2 | 398 |
| $I_{on}$ (μA/μm) @$V_{GS}$ - $V_T$ = 1V, $V_{DS}$ = 1V | 5.6 | 99 | 18.7 | 192 | 26.5 | 284 |
| $I_{on}/I_{off}$ ($\times 10^9$) @$V_{DS}$ = 1V | 0.5 | 9.7 | 1.8 | 19.4 | 2.7 | 34.6 |

in turn affect the channel carrier density as $L_{ch}$ scales down. These carriers arise from the reaction between the channel oxide and the metal contacts. In IGZO with a higher In ratio, the relatively unstable nature of In–O bonds stimulates the reaction, leading to a greater number of oxygen vacancies beneath the contacts, thereby intensifying the $V_T$ roll-off. Nevertheless, our previous studies have shown that $V_T$ roll-off can be mitigated through post-thermal annealing, suggesting that optimized annealing conditions (e.g., duration and temperature) could further reduce the intensified $V_T$ roll-off associated with higher In content in IGZO channel [19].

Table I summarizes the extracted electrical characteristics of IGZO TFTs for both long ($L_{ch} = 1$ μm) and short ($L_{ch} =$ 60 nm) channels, with more than six devices measured for each case. As the In ratio increases from 2:1:1 to 7:1:1, the field-effect mobility ($\mu_{FE}$) improves from 9.7 to 36.6 $cm^2$/V. This improvement is consistent with previous studies showing that modifying the chemical composition of IGZO enhances carrier mobility [21], [22]. Specifically, increasing the In ratio reduces the In–In distance in IGZO, altering the conduction band minimum (CBM) dispersion governed by In s orbitals [5]. This adjustment in CBM dispersion decreases the effective mass of the charge carriers, leading to enhanced electron mobility within the channel.

## B. LFN Characteristics I: $O_2$ Annealing

The LFN characteristics of IGZO TFTs are evaluated by measuring the normalized drain-current power spectral density ($S_{ID}/I_D^2$), which removes the influence of absolute current values. This normalization allows for a more direct comparison of the intrinsic noise behavior across devices. Fig. 5(a) displays the frequency dependence (0.03 Hz–20 kHz) of $S_{ID}/I_D^2$ for IGZO TFTs with different In ratios, measured without post-thermal annealing. For all ratios, the overdrive voltage ($V_{OV,LFN} = V_{GS} - V_T$) was fixed at 1 V within the linear operating region of the device ($V_{DS} = 0.1$ V). The LFN spectra follow a $1/f^{\Gamma}$ behavior, where Γ is approximately 1 for each composition (specifically, 1.089, 1.076, and 1.038 for 2:1:1, 5:1:1, and 7:1:1, respectively), though it slightly deviates to ~1.2 at frequencies below 1 Hz. Increasing the In ratio in the channel effectively lowers the overall LFN, yielding an average improvement of up to 54% (from 2:1:1 to 5:1:1) and up to 86% (from 2:1:1 to 7:1:1) throughout the measured

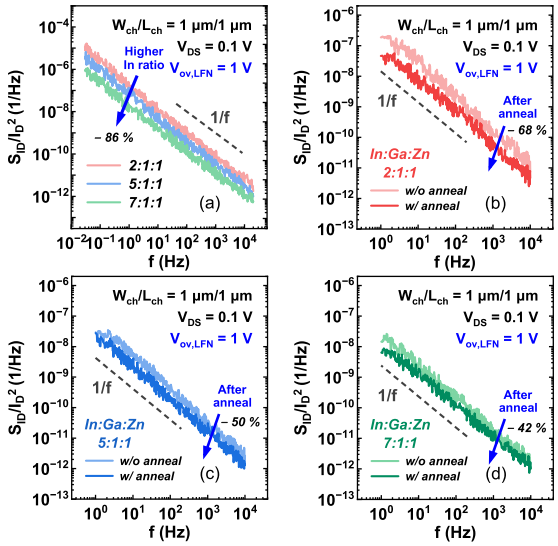


Fig. 5. (a) Summary of normalized drain-current power spectral density ($S_{ID}/I_D^2$) as a function of frequency (0.03 Hz–20 kHz) for IGZO TFTs with different In:Ga:Zn compositions without oxygen annealing at a fixed overdrive voltage ($V_{OV,LFN} = V_{GS} - V_T$) of 1 V. Comparison of $S_{ID}/I_D^2$ versus frequency (1 Hz–10 kHz) with and without oxygen annealing for each In:Ga:Zn composition (b) 2:1:1, (c) 5:1:1, and (d) 7:1:1.

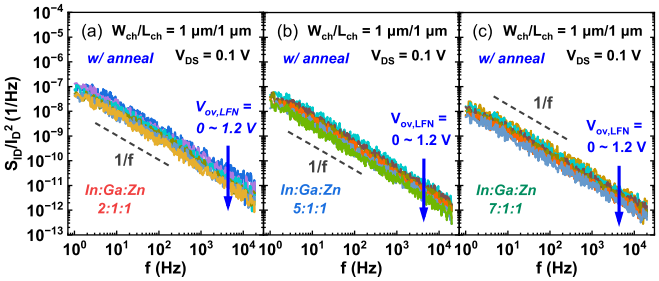


Fig. 6. (a) $S_{ID}/I_D^2$ versus frequency (1 Hz–20 kHz) for IGZO TFTs with different In:Ga:Zn compositions after oxygen annealing (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1. The drain voltage ($V_{DS}$) is fixed at 0.1 V, while $V_{OV,LFN}$ is varied from 0 to 1.2 V.

frequency range. To further investigate the impact of oxygen annealing on the LFN characteristics of IGZO TFTs, $S_{ID}/I_D^2$ for devices with and without short oxygen annealing are compared for different compositions, as shown in Fig. 5(b)–(d). The results show that oxygen annealing improves LFN levels by an average of 68% in 2:1:1, 50% in 5:1:1%, and 42% in 7:1:1.

To understand the origin of the LFN in a-IGZO TFTs, it is essential to examine the $S_{ID}/I_D^2$ values as a function of the $V_{OV}$ since two widely used models to explain LFN exhibit distinct dependencies on $V_{OV}$. Thus, we measured the $S_{ID}/I_D^2$ values at varying $V_{OV}$ (ranging from 0 to 1.2 V) across three different compositions, as illustrated in Fig. 6. Previous studies have demonstrated that contact noise tends to dominate at high $V_{OV}$, where LFN becomes nearly independent of or increases with $V_{OV}$, often exhibiting a saturation-like behavior in $S_{ID}/I_D^2$ versus $V_{OV}$ plots [23], [24], [25]. Since our scope of study focuses on channel noise, our LFN measurements were conducted in a relatively low $V_{OV}$ range (<3 V), where channel noise is expected to be the dominant mechanism.

The $S_{ID}/I_D^2$ values at a fixed frequency ($f = 1$ Hz) were extracted for each $V_{OV}$ and plotted in Fig. 7 to allow a quantitative comparison of their dependence on $V_{OV}$. A clear

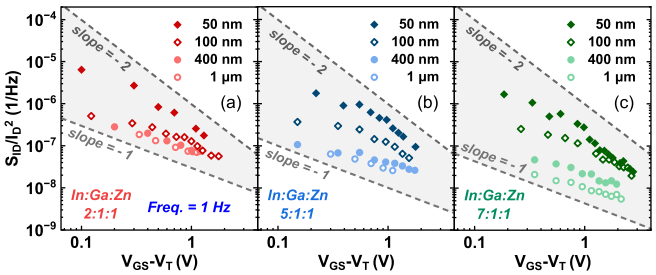


Fig. 7. $S_{ID}/I_D^2$ as a function of $V_{OV,LFN}$ for IGZO TFTs with different In:Ga:Zn compositions (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1. Data are sampled at 1 Hz across different channel lengths from 1 $\mu$m to 50 nm. A transition in the slope of $S_{ID}/I_D^2$ versus $V_{OV,LFN}$ from $-1$ to $-2$ is observed as $L_{ch}$ scales down within each composition.

linear dependence of $S_{ID}/I_D^2$ on $V_{OV}$ across all measured conditions further suggests that the influence of contact noise is negligible in our analyzed regime. For all compositions with $L_{ch}$ of 1 $\mu$m, the $V_{OV}$ dependence approaches a slope of $-1$, which aligns with the $\Delta\mu$ model. This behavior is observed consistently in Fig. 8(a) for both annealed and unannealed samples, indicating that mobility fluctuations in the bulk channel serve as the dominant source of LFN in 1-$\mu$m IGZO TFTs, irrespective of the annealing process. According to the model, LFN arises from variations in carrier mobility, which, in crystalline, silicon-based devices, are mainly driven by lattice and impurity scattering. In amorphous IGZO, however, traps play a more significant role in carrier transport, especially at low carrier densities when $V_{GS}$ is low [26], [27]. Shallow traps introduce localized states within the bandgap that hinder carrier conduction. It has been reported that thermal annealing reduces these localized traps in IGZO [22], [28], [29]. This reduction likely mitigates trap-related scattering in the channel, explaining the improved LFN across different compositions after annealing, as shown in Fig. 5(b)–(d).

### C. LFN Characteristics II: $L_{ch}$

In the previous section, we discussed the effect of oxygen annealing on LFN, focusing on identifying the dominant mechanism in long-channel IGZO TFTs by examining $S_{ID}/I_D^2$ versus $V_{OV}$ dependence. In Fig. 7, however, the $V_{OV}$ dependence shifts from a slope of $-1$ to $-2$ as $L_{ch}$ scales down from 1 $\mu$m to 50 nm, indicating a transition from mobility fluctuations to carrier number fluctuations as the prevailing LFN mechanism across all IGZO TFT compositions. This shift suggests that as the device dimensions shrink, LFN becomes increasingly dominated by carrier trap and detrap effects at the gate dielectric defects near the channel—the primary sources of LFN in the number of carrier fluctuation ($\Delta n$) model. It is worth noting that the majority of previously reported IGZO TFTs follow the $\Delta\mu$ model to explain LFN behavior [15], [16], [30], [31]. These devices often have relatively large dimensions, ranging from tens to hundreds of micrometers, or utilize high-quality ALD-grown gate dielectrics, which reduce the impact of interface traps and lead to LFN characteristics dominated by mobility fluctuations. However, our findings indicate that even in IGZO TFTs utilizing both ALD-grown channel and gate dielectric—known for their superior interface quality—the influence of interface traps on LFN becomes increasingly dominant as $L_{ch}$ scales below 100 nm. Consequently, in scaled devices, effective suppression of LFN necessitates a stronger emphasis on enhancing the gate dielectric and the interface quality.

Given this transition in the dominant LFN mechanism as $L_{ch}$ scaling, it becomes crucial to analyze the results using the appropriate models for each case. In this section, we compare the effects of compositional differences on LFN characteristics by separately analyzing: 1) long-channel and 2) short-channel devices, each described by a distinct LFN model.

*1) Long Channel:* Assuming that LFN characteristics in long-channel IGZO TFTs are dominated by mobility fluctuations, the observed reduction is quantified by extracting Hooge's parameter ($\alpha_H$), an empirical dimensionless constant, from Fig. 6. This parameter is derived by rearranging the noise spectral density equation as described in the $\Delta\mu$ model using the linear region expression

$$\alpha_H = \left(\frac{S_{ID}}{I_{D.}^2}\right)\left(\frac{fC_{ox}WL}{q}\right)V_{OV} \tag{1}$$

where $C_{ox}$ represents the gate insulator capacitance per unit area and $W$ and $L$ denote the channel width and length of the TFTs, respectively. In Fig. 8(b)–(d), $\alpha_H$ is plotted against $V_{OV}$ for each IGZO composition, showing a constant behavior across $V_{OV}$. The average $\alpha_H$ values are presented in each figure, revealing a clear decreasing trend as the enhanced In ratio, dropping from $4.89 \times 10^{-3}$ for the 2:1:1 IGZO to $6.89 \times 10^{-4}$ for the 7:1:1 IGZO after annealing. Given that LFN characteristics in long-channel are governed by mobility fluctuations in the bulk channel, the observed LFN reduction with increasing In concentration may result from a suppression of localized shallow trap states near the CBM, which play an important role in trap-limited conduction by hindering carrier transport in the low gate voltage regime [32], [33]. Compared to previously reported IGZO TFTs, which exhibit $\alpha_H$ values in the range of $10^{-3} < \alpha_H < 10^{-2}$, our devices demonstrate relatively lower LFN, even with ultrathin $T_{ch}$ (<5 nm) and small channel dimensions ($W_{ch}/L_{ch} = 1/1$ $\mu$m). This reduction can be attributed to the precise control afforded by ALD in depositing both the channel and gate dielectric layers, resulting in a more uniform film with fewer interface traps. Considering these observations, an increased In ratio in IGZO, combined with optimized thermal annealing, helps achieve a noticeable enhancement in LFN performance.

To investigate the impact of temperature-dependent LFN characteristics, $S_{ID}/I_D^2$ versus $V_{OV}$ for long-channel IGZO TFTs is measured at three temperatures (i.e., 25 °C–125 °C) across different ratios, as shown in Fig. 9. A consistent slope of $-1$ observed at all temperatures and ratios indicating that mobility fluctuations remain as the primary source. As the temperature rises from 25 °C to 125 °C, the noise level increases—by an average of 82% up to 85 °C and by approximately 65% further at 125 °C. At elevated temperatures, phonon scattering becomes more prominent, introducing additional mobility fluctuations as carriers experience more frequent scattering within the channel, contributing to larger LFN.

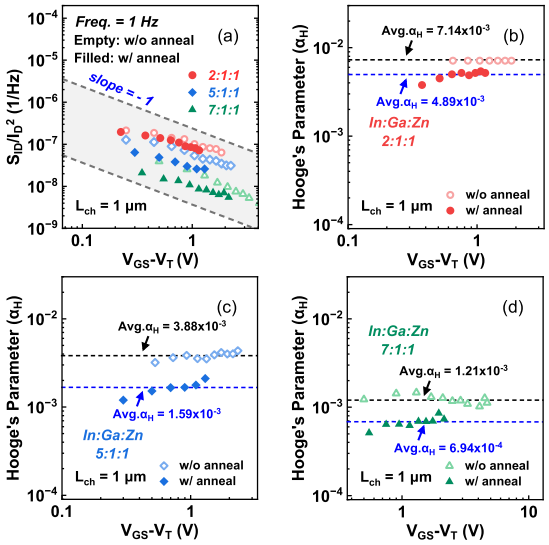


Fig. 8. (a) $S_{ID}/I_D^2$ versus $V_{OV,LFN}$ for IGZO TFTs with a long channel length ($L_{ch} = 1\ \mu$m), comparing the LFN level with and without oxygen annealing. The slope remains near $-1$ in both cases. (b) Extracted Hooge's parameters ($\alpha_H$) versus $V_{OV,LFN}$ for each In:Ga:Zn ratio (b) 2:1:1, (c) 5:1:1, and (d) 7:1:1, with and without oxygen annealing.

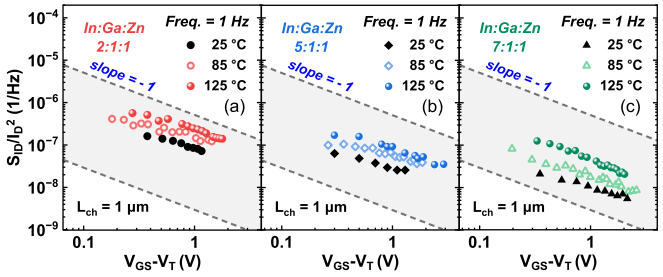


Fig. 9. Comparison of $S_{ID}/I_D^2$ versus $V_{OV,LFN}$ for long-channel IGZO TFTs (LFN sampled at 1 Hz) measured at three temperatures (25 °C to 125 °C) for each composition (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1. The slope of $-1$ is maintained across all compositions and temperatures.

*2) Short Channel:* In Fig. 10, $S_{ID}/I_D^2$ versus $V_{OV}$ for short-channel IGZO TFTs is measured at 25 °C and 85 °C. Unlike the long-channel devices where $S_{ID}/I_D^2$ consistently increases with temperature, the LFN levels in short-channel devices remain largely unaffected by changes in temperature. This distinct behavior, in alignment with the contrasting $S_{ID}/I_D^2$ versus $V_{OV}$ slopes observed in Fig. 7, supports that the dominant LFN mechanism in short-channel devices may differ from that in long-channel devices, shifting from mobility fluctuations to carrier number fluctuations. In this model, noise arises from carrier trapping and detrapping at traps within the gate dielectric near the channel interface rather than from mobility variations in the bulk channel. These interface traps, often referred to as border traps, generally exhibit limited thermal activation within the examined temperature range, which leads to their lower sensitivity to the increased temperature and a minimal impact on LFN in short-channel devices.

To verify that the carrier number fluctuations serve as the dominant LFN mechanism, we analyze the relationship defined by the $\Delta$n model

$$\frac{S_{ID}}{I_D^2} \cong \left(\frac{g_m}{I_D}\right)^2 \times S_{vfb} \tag{2}$$

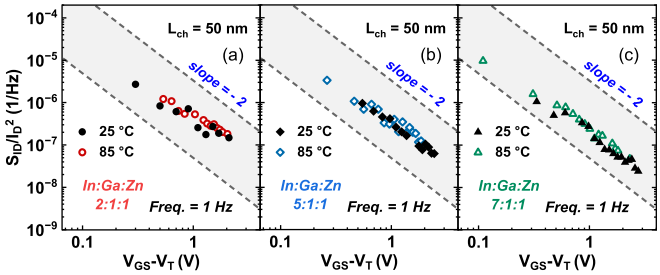


Fig. 10. Comparison of $S_{ID}/I_D^2$ versus $V_{OV,LFN}$ (sampled at 1 Hz) for short-channel IGZO TFTs measured at two different temperatures (25 °C and 85 °C) for each composition (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1. The slope of $-2$ is maintained across all compositions and temperatures.

where $g_m$ is the transconductance and $S_{vfb}$ represents the flat-band voltage noise power spectral density associated with fluctuations in interface charge states [34]. This spectral density distribution can be further expressed as

$$S_{vfb} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f} \tag{3}$$

where $f$ is the frequency, $\lambda$ is the tunnel attenuation distance ($\approx$0.1 nm), $kT$ is the thermal energy, and $N_t$ is the volumetric oxide trap density ($eV^{-1}cm^{-3}$) [35]. Fig. 11(a)–(c) displays the dependence of $(g_m/I_D)^2$ (in black) and $S_{ID}/I_D^2$ (in red) on $I_D$ for IGZO TFTs with varying In compositions. The observed linear correlation confirms the presence of carrier number fluctuations as a key source of LFN. To further examine the influence of interfacial oxide trap density within the gate oxide on LFN across different In ratios, we extract $S_{vfb}$ through a linear fit of the data, as shown in Fig. 11(d), based on the relationship in (2). Subsequently, the gate oxide trap density $N_t$ is determined based on the measured LFN levels. The spatial distribution of these border trap densities in the gate oxide layer can be evaluated by calculating trap depth distribution ($x_t$) with the formula $x_t = \lambda \ln(1/2\pi f \tau_0)$, where $\tau_0$ is the Shockley–Read–Hall recombination time, has a typical value of around $10^{-10}$ s [36]. Fig. 12(a) presents the extracted $N_t$ as a function of trap depth for different IGZO compositions, using data from 1 Hz to 10 kHz. Notably, there was a corresponding decrease in near-channel gate oxide trap density as the In ratio increased. This trend may be linked to the chemical interaction between the IGZO channel and the gate oxide interface. With higher In concentrations in IGZO, the proportion of relatively weak In–O bonds increases relative to strong Ga–O bonds. These weaker In–O bonds are likely to release oxygen atoms, which can subsequently migrate toward the interface during the fabrication process and potentially reduce the formation of oxygen vacancies—one of the primary sources of border traps at the gate dielectric near the interface [37], [38]. Consequently, this reduction in oxygen vacancies near the interface may lead to a lower density of oxide traps in the gate dielectric.

The observed reduction in trap density is consistent with BTI measurements in Fig. 12(b), which show significantly suppressed $\Delta V_T$ degradation in 7:1:1 IGZO compared to 2:1:1 IGZO under positive bias stress (PBS) ($V_{OV} = 4$ V at T = 85 °C). This aligns with the understanding that $\Delta V_T$ under

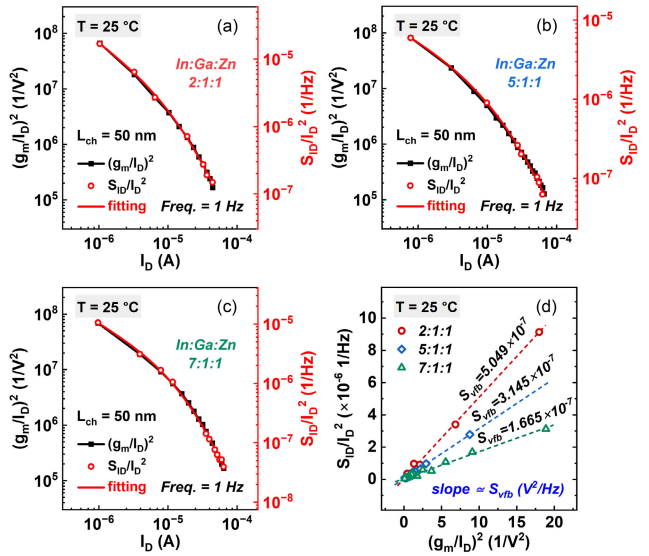


Fig. 11. $(g_m/I_D)^2$ versus $I_D$ (black) and $S_{ID}/I_D^2$ versus $I_D$ (red) for IGZO TFTs with different In:Ga:Zn composition (a) 2:1:1, (b) 5:1:1, and (c) 7:1:1. (d) Relationship between $(g_m/I_D)^2$ and $S_{ID}/I_D^2$, where $S_{vfb}$ is extracted by linear fitting of the slope.

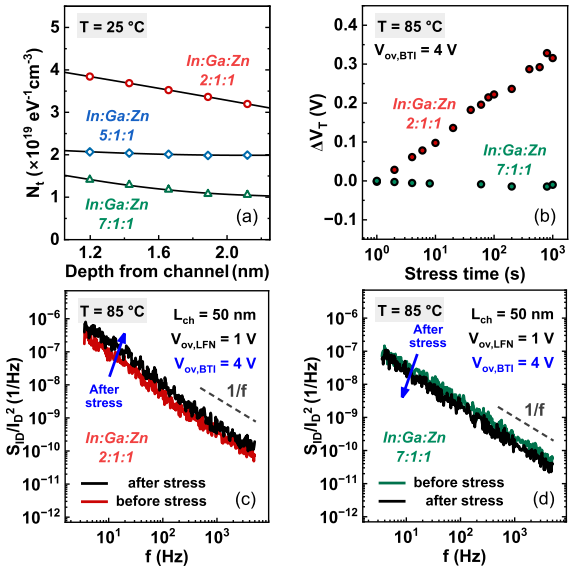


Fig. 12. (a) Extracted gate oxide trap density ($N_t$) versus trap depth for IGZO TFTs with different In:Ga:Zn composition, using data from 1 Hz to 10 kHz. (b) $V_T$ shift ($\Delta V_T$) under PBS at the gate ($V_{OV,BTI} = V_{GS} - V_T = 4$ V and T = 85 °C) for 2:1:1 and 7:1:1 IGZO TFTs. Comparison of $S_{ID}/I_D^2$ versus frequency (5 Hz–5 kHz) before and after gate bias stress of 1000 s for (c) 2:1:1 and (d) 7:1:1 IGZO TFTs.

PBS is primarily attributed to electron trapping at the gate oxide and interface, leading to a positive shift in threshold voltage [39]. Additionally, Fig. 12(c)–(d) compares the LFN characteristics, $S_{ID}/I_D^2$ versus frequency from 5 Hz to 5 kHz, for 2:1:1 and 7:1:1 IGZO TFTs before and after 1000 s of PBS. While both compositions maintain a 1/f slope, the 2:1:1 IGZO shows a noticeable increase in noise after stress, whereas the 7:1:1 IGZO exhibits relatively stable noise levels. This change in LFN after PBS further supports interface traps as the dominant source of LFN in short-channel devices while reinforcing the correlation between higher In ratios, reduced interface trap density, and improved noise resilience.

The increase in LFN in the 2:1:1 device is consistent with enhanced electron trapping effects shown in Fig. 12(b), which may lead to greater fluctuations in the number of carriers due to newly generated trap sites [40]. In contrast, the relatively stable LFN in the 7:1:1 IGZO suggests that additional factors, such as the hydrogen-induced passivation of preexisting or newly generated trap sites, may contribute to suppressing post-stress noise, as observed in a previous study [41]. However, further investigations are necessary to conclusively determine the underlying mechanisms.

## IV. Conclusion

This study provides an in-depth analysis of LFN origins in scaled ALD IGZO TFTs, focusing on the effects of composition, thermal annealing, and channel scaling. Post-oxygen annealing effectively reduces LFN across all compositions, achieving an average improvement of up to 53%. Analysis of $S_{ID}/I_D^2$ versus $V_{OV}$ reveals a gradual transition in the dominant LFN mechanism as channel dimensions decrease. In long-channel devices, LFN is governed by the $\Delta\mu$ model, with higher In ratios reducing shallow traps in the bulk channel, leading to noise reductions of up to 85%. This trend is quantified by a decrease in $\alpha_H$, from $4.89 \times 10^{-3}$ for 2:1:1 IGZO to $6.89 \times 10^{-4}$ and 7:1:1 IGZO TFTs. In contrast, short-channel devices show a shift toward the $\Delta n$ model as the dominant LFN mechanism, driven by trap/detrap processes at the near-channel gate oxide. The observed reduction in gate oxide trap density with increasing In ratios, as corroborated by BTI measurements, underscores the role of In concentration in stabilizing the gate dielectric/channel interface. By systematically examining the interplay between composition, thermal treatment, and scaling effects on LFN, this study highlights strategies for improving both the performance and reliability of IGZO TFTs while emphasizing the need for appropriate LFN models to analyze noise behavior in scaled applications.

## References

[1] N. Loubet et al., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, Jun. 2017, pp. 230–231, doi: 10.23919/VLSIT.2017.7998183.

[2] X. Duan et al., "Novel vertical channel-all-around (CAA) In-Ga-Zn-O FET for 2T0C-DRAM with high density beyond $4F^2$ by monolithic stacking," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2196–2202, Apr. 2022, doi: 10.1109/TED.2022.3154693.

[3] S. Liao et al., "Complementary field-effect transistor (CFET) demonstration at 48 nm gate pitch for future logic technology scaling," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413672.

[4] H. Hosono, "How we made the IGZO transistor," *Nature Electron.*, vol. 1, no. 7, p. 428, Jul. 2018, doi: 10.1038/s41928-018-0106-0.

[5] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment andab initiocalculations," *Phys. Rev. B, Condens. Matter*, vol. 75, no. 3, Jan. 2007, Art. no. 035212, doi: 10.1103/physrevb.75.035212.

[6] J. Zhang et al., "Back-end-of-line-compatible scaled InGaZnO transistors by atomic layer deposition," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6651–6657, Dec. 2023, doi: 10.1109/TED.2023.3312357.

[7] S. Lee, C. Niu, Y. Zhang, H. Wang, and P. D. Ye, "Positive to negative Schottky barrier transition in metal/oxide semiconductor contacts by tuning indium concentration in IGZO," in *Proc. Symp. VLSI Technol. Circuits*, Honolulu, HI, USA, 2024, pp. 1–3, doi: 10.1109/VLSITechnologyandCir46783.2024.10631411.

[8] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," *Nature Electron.*, vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: 10.1038/s41928-022-00718-w.

[9] J.-Y. Lin et al., "First demonstration of top-gate enhancement-mode ALD $In_2O_3$ FETs with high thermal budget of 600 °C for DRAM applications," *IEEE Electron Device Lett.*, vol. 45, no. 10, pp. 1851–1854, Oct. 2024, doi: 10.1109/LED.2024.3442729.

[10] D. Ha et al., "Highly manufacturable, cost-effective, and monolithically stackable $4F^2$ single-gated IGZO vertical channel transistor (VCT) for sub-10nm DRAM," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413772.

[11] W.-T. Chen et al., "Oxygen-dependent instability and annealing/passivation effects in amorphous In-Ga-Zn-O thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1552–1554, Nov. 2011, doi: 10.1109/LED.2011.2165694.

[12] J. Zhang et al., "First demonstration of BEOL-compatible atomic-layer-deposited InGaZnO TFTs with 1.5 nm channel thickness and 60 nm channel length achieving ON/OFF ratio exceeding $10^{11}$, SS of 68 mV/dec, normal-off operation and high positive gate bias stability," in *Proc. Symp. VLSI Technol. Circuits*, Kyoto, Japan, 2023, pp. 1–2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185312.

[13] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994, doi: 10.1109/16.333808.

[14] P. Kushwaha et al., "Characterization and modeling of flicker noise in FinFETs at advanced technology node," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 985–988, Jun. 2019, doi: 10.1109/LED.2019.2911614.

[15] R. Kolarova, T. Skotnicki, and J. A. Chroboczek, "Low frequency noise in thin gate oxide MOSFETs," *Microelectron. Rel.*, vol. 41, no. 4, pp. 579–585, Apr. 2001, doi: 10.1016/s0026-2714(00)00248-1.

[16] T.-C. Fung, G. Baek, and J. Kanicki, "Low frequency noise in long channel amorphous In–Ga–Zn–O thin film transistors," *J. Appl. Phys.*, vol. 108, no. 7, Oct. 2010, Art. no. 074518, doi: 10.1063/1.3490193.

[17] J.-M. Lee, W.-S. Cheong, C.-S. Hwang, I.-T. Cho, H.-I. Kwon, and J.-H. Lee, "Low-frequency noise in amorphous indium-gallium-zinc-oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 505–507, May 2009, doi: 10.1109/LED.2009.2015783.

[18] C. G. Theodorou et al., "Origin of low-frequency noise in the low drain current range of bottom-gate amorphous IGZO thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 898–900, Jul. 2011, doi: 10.1109/LED.2011.2143386.

[19] M. Si, A. Charnas, Z. Lin, and P. D. Ye, "Enhancement-mode atomic-layer-deposited $In_2O_3$ transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1075–1080, Mar. 2021, doi: 10.1109/TED.2021.3053229.

[20] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[21] T. Hong, Y. Kim, S. Choi, J. H. Lim, and J. Park, "Exploration of chemical composition of In–Ga–Zn–O system via PEALD technique for optimal physical and electrical properties," *Adv. Electron. Mater.*, vol. 9, no. 4, Apr. 2023, Art. no. 2201208, doi: 10.1002/aelm.202201208.

[22] K. Nomura et al., "Subgap states in transparent amorphous oxide semiconductor, In–Ga–Zn–O, observed by bulk sensitive X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 92, no. 20, May 2008, Art. no. 202117, doi: 10.1063/1.2927306.

[23] J. Rhayem, M. Valenza, D. Rigaud, N. Szydlo, and H. Lebrun, "1/f noise investigations in small channel length amorphous silicon thin film transistors," *J. Appl. Phys.*, vol. 83, no. 7, pp. 3660–3667, Apr. 1998, doi: 10.1063/1.366586.

[24] J. Renteria et al., "Low-frequency 1/f noise in $MoS_2$ transistors: Relative contributions of the channel and contacts," *Appl. Phys. Lett.*, vol. 104, no. 15, Apr. 2014, Art. no. 153104, doi: 10.1063/1.4871374.

[25] Y. Chen et al., "Source–drain contact impacts on electrical performances and low frequency noise of InZnO thin-film transistors down to 7 K," *Appl. Phys. Lett.*, vol. 124, no. 17, Apr. 2024, Art. no. 173507, doi: 10.1063/5.0204316.

[26] S. Lee et al., "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 20, May 2011, Art. no. 203508, doi: 10.1063/1.3589371.

[27] C.-G. Lee, B. Cobb, and A. Dodabalapur, "Band transport and mobility edge in amorphous solution-processed zinc tin oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 97, no. 20, Nov. 2010, Art. no. 203505, doi: 10.1063/1.3517502.

[28] K. Nomura, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Defect passivation and homogenization of amorphous oxide thin-film transistor by wet $O_2$ annealing," *Appl. Phys. Lett.*, vol. 93, no. 19, Nov. 2008, Art. no. 192107, doi: 10.1063/1.3020714.

[29] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, "Trap densities in amorphous-$InGaZnO_4$ thin-film transistors," *Appl. Phys. Lett.*, vol. 92, no. 13, Mar. 2008, Art. no. 133512, doi: 10.1063/1.2904704.

[30] I.-T. Cho, W.-S. Cheong, C.-S. Hwang, J.-M. Lee, H.-I. Kwon, and J.-H. Lee, "Comparative study of the low-frequency-noise behaviors in a-IGZO thin-film transistors with $Al_2O_3$ and $Al_2O_3$/SiNx gate dielectrics," *IEEE Electron Device Lett.*, vol. 30, no. 8, pp. 828–830, Aug. 2009, doi: 10.1109/LED.2009.2023543.

[31] H.-S. Choi, S. Jeon, H. Kim, J. Shin, C. Kim, and U.-I. Chung, "Verification of interface state properties of a-InGaZnO thin-film transistors with $SiN_x$ and $SiO_2$ gate dielectrics by low-frequency noise measurements," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1083–1085, Aug. 2011, doi: 10.1109/LED.2011.2158057.

[32] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, Jul. 2009, doi: 10.1109/jdt.2009.2021582.

[33] W. Chakraborty, H. Ye, B. Grisafe, I. Lightcap, and S. Datta, "Low thermal budget (<250 °C) dual-gate amorphous indium tungsten oxide (IWO) thin-film transistor for monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5336–5342, Dec. 2020, doi: 10.1109/TED.2020.3034063.

[34] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: 10.1002/pssa.2211240225.

[35] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 573–582, Apr. 2002.

[36] J. W. Lee, W. S. Yun, and G. Ghibaudo, "Impact of trap localization on low-frequency noise in nanoscale device," *J. Appl. Phys.*, vol. 115, no. 19, May 2014, Art. no. 194501, doi: 10.1063/1.4878456.

[37] S. Guha and V. Narayanan, "Oxygen vacancies in high dielectric constant oxide-semiconductor films," *Phys. Rev. Lett.*, vol. 98, no. 19, May 2007, Art. no. 196101, doi: 10.1103/physrevlett.98.196101.

[38] E. Cartier, B. P. Linder, V. Narayanan, and V. K. Paruchuri, "Fundamental understanding and optimization of PBTI in nFETs with $SiO_2$/$HfO_2$ gate stack," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2006, pp. 1–4, doi: 10.1109/IEDM.2006.346773.

[39] Y.-P. Chen, M. Si, B. K. Mahajan, Z. Lin, P. D. Ye, and M. A. Alam, "Positive bias temperature instability and hot carrier degradation of back-end-of-line, nm-thick, $In_2O_3$ thin-film transistors," *IEEE Electron Device Lett.*, vol. 43, no. 2, pp. 232–235, Feb. 2022, doi: 10.1109/LED.2021.3134902.

[40] C. Gu, Q. Hu, Q. Li, S. Zhu, J. Kang, and Y. Wu, "1/f noise of short-channel indium tin oxide transistors under stress," *Appl. Phys. Lett.*, vol. 122, no. 25, Jun. 2023, Art. no. 252104, doi: 10.1063/5.0147577.

[41] G. Liu et al., "Unveiling the influence of channel thickness on PBTI and LFN in sub-10 nm-thick IGZO FETs: A holistic perspective for advancing oxide semiconductor devices," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413735.