Effects of Gallium on Electron Transport and Bias Stability in Ultrascaled Amorphous InGaO Transistors

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***Abstract*— In this work, we systematically investigated the effects of gallium (Ga) incorporation on electron transport and bias stability in ultrascaled InGaO transistors with channel thickness (T_{ch}) of 3 nm and scaled channel length (L_{ch}) down to 60 nm. It is found that Ga atoms act as carrier suppressors in the In_2O_3 host, resulting in a positively shifted threshold voltage (V_{th}) and a concurrent reduction in field-effect mobility (μ_{FE}) as Ga concentration increases. Notably, the shift in V_{th} (ΔV_{th}) of InGaO transistors during positive gate bias stability (PBS) tests transitions from negative to positive with increasing Ga concentration. This behavior is explained by the trap neutrality level (TNL) model, which defines the energy level at which positively charged donor-like traps are balanced by negatively charged acceptor-like traps. The relative position of the Fermi level (E_F) in In_XGaO with respect to the TNL determines whether donor-like or acceptor-like traps dominate the charge trapping behavior. Ga incorporation modifies the electronic nature of interface traps by reducing donor-like oxygen vacancies and introducing acceptor-like excessive oxygen states due to its strong oxygen-gettering effect. This study elucidates the crucial role of Ga in electron transport and bias stability in ultrascaled amorphous InGaO transistors, providing valuable guidance for designing In_2O_3-based transistors with high ON-state and stability performance while also shedding light on the interfacial trap dynamics in the ultrascaled regime.**

***Index Terms*— Amorphous oxide semiconductor, atomic layer deposition (ALD), back-end-of-line (BEOL) compatibility, electron percolation transport, gate bias stability.**

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I. Introduction

As SILICON CMOS transistors approach the physical limits of further scaling, monolithic 3-D integration—where layers of logic and memory are vertically stacked to increase chip density and reduce signal transmission delays—has emerged as a key enabler for the continuation of Moore's Law [1], [2]. Oxide semiconductors have shown great promise for back-end-of-line (BEOL)-compatible logic and memory applications in monolithic 3-D integration due to their advantageous properties, including high electron mobility, excellent uniformity, low leakage current, and low-temperature fabrication capabilities [1], [2], [3]. Ultrascaled In_2O_3-based transistors with sub-10 nm channel thickness (T_{ch}) and sub-100 nm channel length (L_{ch}) have recently been demonstrated, enabled by either sputtering or atomic layer deposition (ALD) within a BEOL-compatible fabrication process [4], [5], [6], [7]. These ultrascaled In_2O_3-based transistors exhibit excellent ON-state performance, achieving extremely high ON-current values, thereby confirming their potential as strong candidates for BEOL transistors. Such extraordinary ON-state performance can be attributed to the ultrahigh electron density occupying high-energy states in the conduction band of In_2O_3, resulting in high band velocity [1], [2], [3], [4], [5], [6], [7]. However, this excessive electron density leads to a negative threshold voltage (V_{th}), and reliability issues arise for transistors with high drain currents, which must be adequately addressed for practical applications [8], [9].

Recent investigations into ultrascaled In_2O_3 and doped-In_2O_3 transistors have provided initial evaluations of stability performance [5], [6], [7], [8], [9], [10], [11]. These studies indicate that doping In_2O_3 with metal cations that possess stronger oxygen-bonding capabilities, such as W [5], Sn [6], [10], Zn [11], [12], Ga [13], [14], effectively reduces excessive electrons and achieves a positive V_{th}. Notably, these ultrascaled In_2O_3-based transistors can exhibit anomalously negative shifts in V_{th} (ΔV_{th}) during positive gate bias stability (PBS) tests, a phenomenon not explicable by classical trapping/detrapping mechanisms [10], [11], [12], [13], [14]. Furthermore, cation doping has been shown to alleviate the negative ΔV_{th} [10], [11]. Several studies suggest that the anomalously negative ΔV_{th} may stem from hydrogen diffusion from the high-k dielectric into the channel under gate stress [15], [16], [17], [18]. However, hydrogen diffusion alone cannot fully account for the reduction in negative ΔV_{th}

observed with cation doping in the In_2O_3 channel while maintaining the same dielectric [10], [11]. This implies that the electronic signature of traps is closely related to the channel characteristics, underscoring the necessity for more in-depth studies on the atomistic effects of cation doping on electron transport and trapping in these ultrascaled oxide transistors. Among all doped In_2O_3 systems, ternary InGaO serves as an ideal platform for studying the effects of cation doping. Ga has the same number of valence electrons as In but features a smaller radius, higher ionic potential, and stronger bonding energy with oxygen [13], [19]. This leads to minimal modifications of the In_2O_3 host, providing valuable insights into the behavior of other metal cations.

In this work, we systematically investigated the effects of Ga doping on the electrical performance of ultrascaled InGaO transistors with a T_{ch} of 3 nm and an L_{ch} down to 60 nm achieved through ALD, with Ga concentration adjusted via ALD subcycle ratios. The results indicate that Ga atoms act as effective carrier suppressors and potential trap sites within the In_2O_3 host, resulting in a positive shift in V_{th} and a concurrent reduction in μ_{FE} as Ga concentration increases. Gate bias stability tests reveal that the anomalously negative ΔV_{th} observed under PBS occurs exclusively in In-rich InGaO transistors. We propose that the electronic signature of interface traps, where the E_F of InGaO resides, shifts from donor-like to acceptor-like upon Ga incorporation. This can be attributed to the strong oxygen-gettering effects of Ga, which reduces oxygen vacancies that function as donor-like traps while introducing excessive oxygen states that act as acceptor-like traps. This is corroborated by X-ray photoelectron spectroscopy (XPS) and supported by density function theory (DFT) calculations. This study not only demonstrates ultrascaled amorphous InGaO transistors with state-of-the-art electrical performance for BEOL applications but also elucidates the crucial role of cation dopants with stronger oxygen-bonding capabilities in electron transport and bias stability in ultrascaled In_2O_3-based transistors.

II. Experiment

Fig. 1(a) illustrates the schematic of an ultrathin In_XGaO transistor with varying Ga concentrations, where X denotes the ratio of In_2O_3 to Ga_2O_3 in the ALD growth cycles, thereby controlling the incorporated Ga concentration. These In_XGaO transistors feature a back-gate and top-contact architecture, with 40 nm Ni, 6 nm HfO_2, and 3 nm In_XGaO serving as the electrodes, dielectric, and channel, respectively. The fabrication process of In_XGaO transistors is similar to our previous work [4], [13]. Briefly, the process started with the growth of 8 nm Al_2O_3 by ALD at 175 °C on the p^+ Si substrate with thermally grown 90 nm SiO_2 to obtain a smooth surface, where $(CH_3)_3Al$ and H_2O function as the Al and O precursors, respectively. Then, 40 nm Ni bottom gates were formed by a bilayer photoresist lithography process and e-beam evaporation. Next, 6 nm HfO_2 was deposited by ALD at 200 °C as gate dielectric using $[(CH_3)_2N]_4Hf$ and H_2O as the Hf and O precursors, respectively. This is followed by 3 nm In_XGaO channel deposition using ALD at 225 °C with $In(CH_3)_3$, $Ga_2(NMe_2)_6$, and H_2O as the In, Ga, and O precursors, respectively. The supercycle of the In_XGaO consists of one cycle of Ga_2O_3 followed by X (X = 1, 3, 5, 10) cycles of In_2O_3, and the thickness of the In_XGaO channel was controlled by the number of supercycles. Then, BCl_3/Ar ICP etching was performed for device isolation.

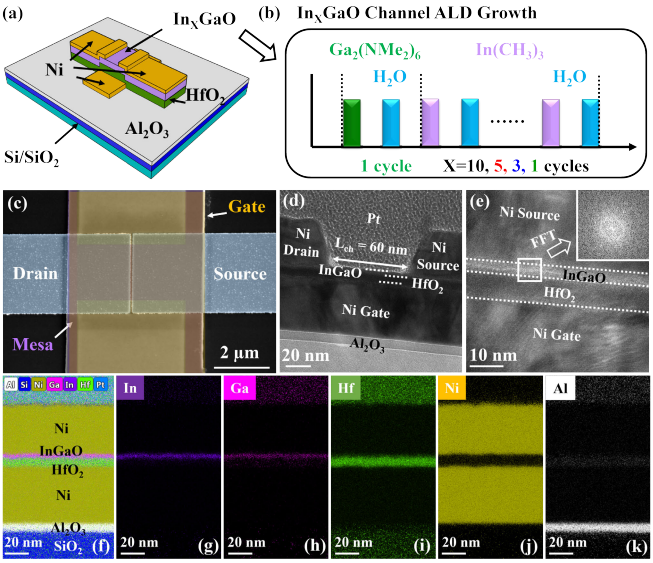

Fig. 1. (a) Schematic of ALD-derived ultrathin InGaO transistors. (b) In_XGaO ALD growth. (c) Top-down SEM image. (d) Cross-sectional TEM image of the InGaO transistor with an L_{ch} of 60 nm and a T_{ch} of 3 nm. (e) Magnified TEM image; Inset: FFT image of the selected region of the InGaO channel. (f)–(k) HAADF STEM images with EDX elemental mapping.

Finally, 40 nm Ni as source/drain contacts were formed by e-beam evaporation and patterned by e-beam lithography. The devices were annealed in O_2 at 250 °C for 1 min to improve the interface quality before measurement.

Leveraging the high-resolution patterning capabilities of electron beam lithography, we successfully scaled down the L_{ch} of our In_XGaO transistors to sub-100 nm dimensions. Fig. 1(c) and (d) present the top-down scanning electron microscope (SEM) image and the cross-sectional high-resolution transmission electron microscope (TEM) image of the ultrascaled $In_{10}GaO$ transistors, respectively, revealing an L_{ch} of 60 nm and a T_{ch} of 3 nm. Furthermore, Fig. 1(e) provides a magnified view of the channel region, showing no observable crystallinity in the ultrathin $In_{10}GaO$ channel, as evidenced by the diffusion ring feature in the fast Fourier transform (FFT) image of the selected region, depicted in the inset of Fig. 1(e). The amorphous nature of the InGaO channel is supported by the incorporation of Ga as a crystallization retarder [19], [20], the ultrathin thickness, and the low-temperature fabrication process, all of which contribute to excellent short-range uniformity. Fig. 1(f)–(k) further illustrates the high-angle annular dark-field (HAADF) scanning TEM (STEM) images, along with energy dispersive X-ray spectroscopy (EDX) elemental mapping of the Ni/$In_{10}GaO$/HfO_2/Ni/Al_2O_3/SiO_2 stack, highlighting the excellent interface quality between the HfO_2 dielectric and the $In_{10}GaO$ channel without observable interdiffusion. This superior interface quality can be attributed to the smooth and uniform oxide films enabled by ALD, which exhibits a low surface roughness of approximately 0.06 nm, as examined by atomic force microscopy (Not shown). Achieving such atomically thin films with other deposition techniques would be challenging.

It is noted that the back-gate structure provides a platform for investigating the effects of Ga doping on electron transport and trapping properties. This design choice is crucial because

the deposition of a top dielectric may introduce unintentional defects into the oxide channel [21], potentially degrading electron transport and masking the effects of Ga doping. On the other hand, these transistors may be susceptible to oxygen and water adsorption/desorption from the air due to the lack of a passivation layer [22]. Therefore, all electrical measurements were conducted in dark and nitrogen (N_2) ambient conditions, with a constant N_2 flow of approximately 5 standard cubic feet per minute (SCFM) to mitigate environmental effects.

III. Results and Discussion

A. Effects of Ga Concentration on Electron Transport

Fig. 2(a) presents the transfer characteristics of In_XGaO transistors with an L_{ch} of 60 nm and a T_{ch} of 3 nm under V_{DS} of 0.5 V. Five In_XGaO transistors with the same Ga concentration exhibit consistent switching behavior. As the Ga concentration increases (lower X values), the transfer curves shift positively, accompanied by an enlarged hysteresis window and reduced current drivability. Notably, the subthreshold swing (SS) increases with higher Ga concentration, with values of 95 ± 6, 83 ± 5, 94 ± 12, and 147 ± 5 mV/dec as the X value decreases from 10 to 5, 3, and 1. The decreased current drivability with Ga incorporation suggests that Ga atoms function as effective carrier suppressors and potential trap sites within the In_2O_3 host, impeding the generation and transport of free electrons. Fig. 2(b) shows the extracted V_{th} as a function of L_{ch} for In_XGaO transistors by linear extrapolation, showing that enhancement-mode (E-mode) operation can be achieved with a higher Ga concentration. The error bars represent the standard deviations calculated from the average of five transistors. Moreover, our In_XGaO transistors also exhibit excellent short-channel immunity, as indicated by consistent V_{th} values across varying L_{ch}. This is attributed to the ultrathin channel/dielectric stack.

Fig. 2(c) illustrates the extracted transconductance (g_m) as a function of L_{ch} under a V_{DS} of 0.5 V for In_XGaO transistors, where a $1/L_{ch}$ trend is generally observed, except for In_1GaO transistors with sub-100-nm L_{ch}. This deviation indicates that contact resistance (R_C) becomes significant in these short-channel In_1GaO transistors. Transfer length method (TLM) measurements were conducted on these In_XGaO transistors. The extracted R_C and sheet resistance (R_{sheet}) as functions of gate overdrive voltage ($V_{GS}-V_{th}$) are plotted in Fig. 2(d). Both R_c and R_{sheet} increases significantly with increasing Ga concentration. Specifically, Rc increases from 0.2 to 0.8 Ω · mm, 2.6 and 267 Ω · mm as X reduces from 10 to 5, 3, and 1, respectively, under $V_{GS}-V_{th}$ of 1.2 V. Similarly, R_{sheet} also increases from 2.2, 4.4, and 16.6, to 2534 Ω/□. The increase in both R_C and R_{sheet} can be attributed to the significant reduction in electron concentration upon Ga incorporation. The marked rise in R_C for In_1GaO transistors also explains the deviation of g_m from the $1/L_{ch}$ trend in Fig. 2(c).

Fig. 3(a)–(d) shows the output characteristics of the In_XGaO transistors with an L_{ch} of 60 nm and X values ranging from 10 to 1. The maximum ON-current density (I_{on}) is recorded as 1328, 504, 232, and 0.46 $\mu A/\mu m$ for $X = 10$, 5, 3, and 1, respectively, under a V_{GS} of 4 V. It is important to note that the maximum applied V_{DS} is limited for In_XGaO transistors with high In concentration due to the severe self-heating under high electric fields and current stress [23], resulting in a lack of observable current saturation under the $V_{DS} < V_{GS}-V_{th}$ bias condition. Conversely, current saturation can be achieved in long-channel transistors (Not shown), although this occurs at the cost of reduced current.

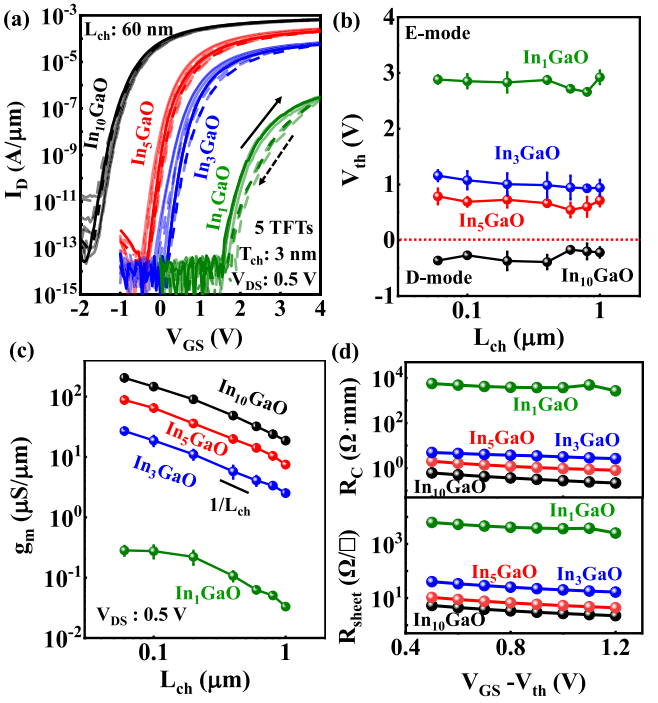

Fig. 2. (a) Transfer curves of In_XGaO transistors with an L_{ch} of 60 nm and a T_{ch} of 3 nm under V_{DS} of 0.5 V, showing consistent switching characteristics across five transistors. (b) Extracted V_{th} as a function of L_{ch} for In_XGaO transistors. (c) Extracted g_m as a function of L_{ch} under V_{DS} of 0.5 V for In_XGaO transistors, where the trend follows $1/L_{ch}$. (d) Extracted R_C and R_{sheet} as a function of gate overdrive voltage for In_XGaO transistors by TLM method.

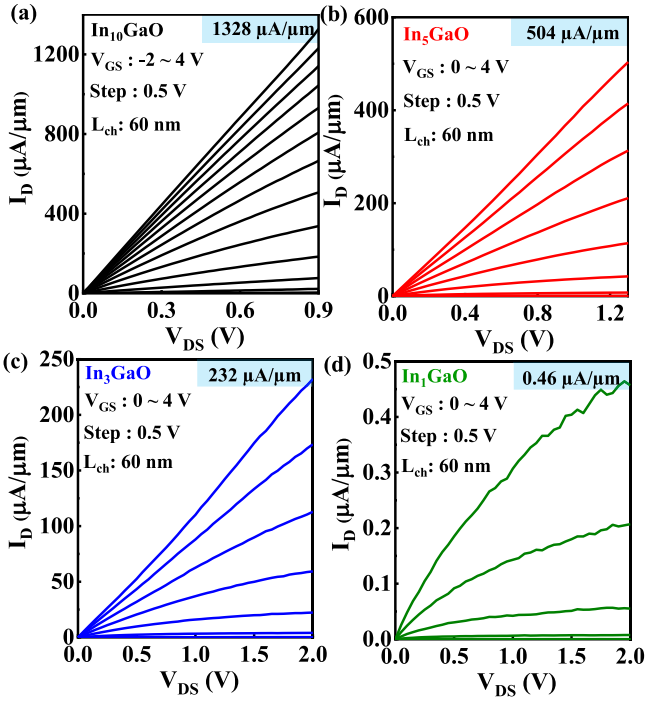

Fig. 3. Output characteristics for (a) $In_{10}GaO$, (b) In_5GaO, (c) In_3GaO, and (d) In_1GaO transistors, all with L_{ch} of 60 nm.

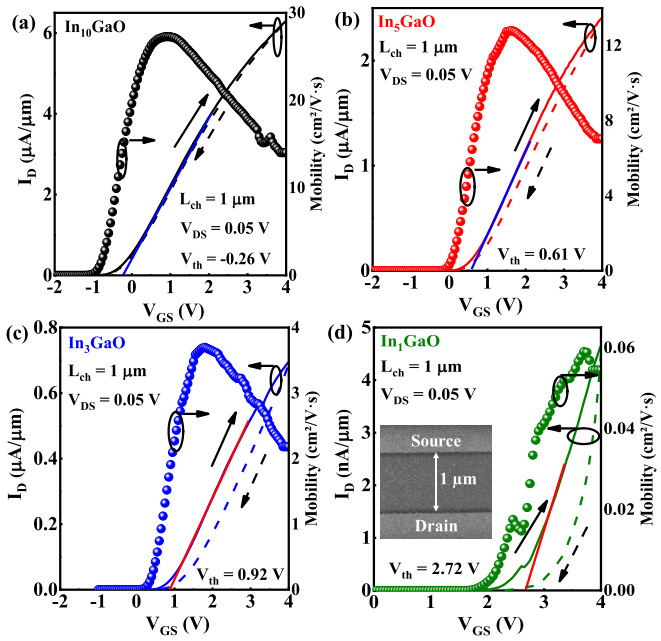

Fig. 4. Extracted V_{th} and μ_{FE} for (a) $In_{10}GaO$, (b) In_5GaO, (c) In_3GaO, and (d) In_1GaO transistors with L_{ch} of 1 μm under V_{DS} of 0.05 V. Inset of (d): Top-down SEM image of transistors with L_{ch} of 1 μm.

The field-effect mobility (μ_{FE}) of In_XGaO can be extracted from the g_m of transistors with a large L_{ch} of 1 μm under V_{DS} of 0.05 V in Fig. 4, assuming that the R_C is negligible compared to the R_{sheet}. The μ_{FE} decreases monotonically from 28.6 ± 1.05 $cm^2 \cdot V^{-1} \cdot s^{-1}$ ($X = 10$) to 11.4 ± 1.4 $cm^2 \cdot V^{-1} \cdot s^{-1}$ ($X = 5$), 3.9 ± 0.09 $cm^2 \cdot V^{-1} \cdot s^{-1}$ ($X = 3$), and 0.06 ± 0.008 $cm^2 \cdot V^{-1} \cdot s^{-1}$ ($X = 1$). The mobility peak arises from strong surface scattering under high vertical electric fields in the ultrathin channel/dielectric stack. On the other hand, the V_{th} during forward sweep is determined through linear extrapolation. Correspondingly, V_{th} increases from -0.22 ± 0.09 V ($X = 10$) to 0.69 ± 0.08 V ($X = 5$), 0.93 ± 0.03 V ($X = 3$), and 2.66 ± 0.04 V ($X = 1$). Fig. 5(a) illustrates the extracted μ_{FE} as a function of V_{th} for In_XGaO transistors with varying Ga concentration, revealing a reciprocal relationship that suggests an electron percolation transport mechanism in the amorphous oxide semiconductors [24], [25]. According to this theory, potential barriers arising from structural randomness near the conduction band hinder electron transport. Electrons can become trapped at localized states between these barriers, with only a fraction gaining enough energy to contribute to charge transport. When these electrons reach the delocalized states in the conduction band, they behave as free electrons with a band mobility (μ_{Band}). Thus, μ_{FE} is proportional to μ_{Band} and the ratio of the free carriers to those trapped in the trap states [24], [25]. As carrier concentration increases, more electrons can overcome energy barriers, improving μ_{FE}. Fig. 5(b) schematically illustrates the percolation mechanism, elucidating the observed reciprocal relationship between V_{th} and μ_{FE}.

B. Effects of Ga Concentration on Gate Bias Stability

Systematic gate bias stress stability tests were conducted on In_XGaO transistors with an L_{ch} of 80 nm at room temperature in an N_2 ambient. As shown in the inset of

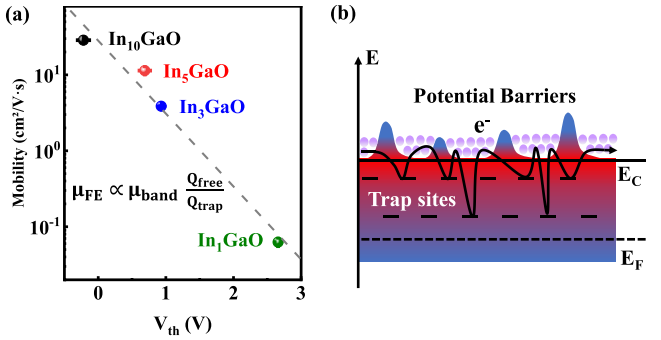

Fig. 5. (a) Extracted μ_{FE} as a function of V_{th}, indicating a percolation transport mechanism. (b) Illustration of the percolation mechanism.

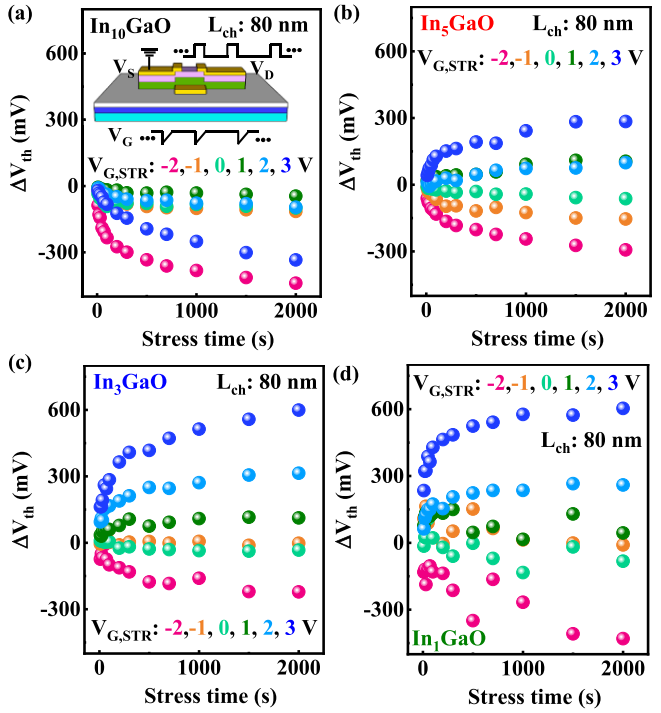

Fig. 6. Time evolution of ΔV_{th} for (a) $In_{10}GaO$, (b) In_5GaO, (c) In_3GaO, and (d) In_1GaO transistors with an L_{ch} of 80 nm during gate bias stability tests conducted for up to 2 ks. Inset of (a): schematic of the gate bias stability test.

Fig. 6(a), the measurement-stress-measurement scheme was employed for the stability tests, where the gate was biased at a fixed voltage ($V_{G,STR}$), while the source and drain were grounded during the stress phase. After each stress segment, full transfer curves under a V_{DS} of 50 mV were measured using a moderate integration time to minimize recovery effects. Fig. 6(a)–(d) summarizes the time evolution of ΔV_{th} for In_XGaO transistors with an L_{ch} of 80 nm under various $V_{G,STR}$ conditions with stress durations of up to 2 ks. Notably, $In_{10}GaO$ transistors exhibit an anomalous negative ΔV_{th} under positive $V_{G,STR}$ while transistors with higher Ga concentrations show a typical positive ΔV_{th}. Additionally, the magnitude of the positive ΔV_{th} increases with higher Ga concentration.

It is widely accepted that electron trapping at interface states under positive $V_{G,STR}$ results in a positive ΔV_{th}, while electron release from these traps under negative $V_{G,STR}$ leads to a negative ΔV_{th} [26]. However, this model assumes that the

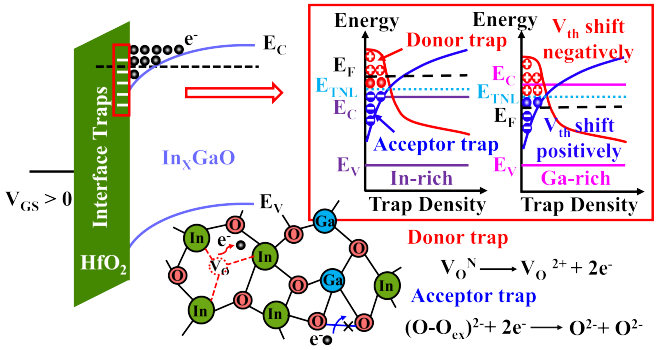

Fig. 7. Proposed trap model to explain the distinct ΔV_{th} behavior observed in In_XGaO transistors with varying Ga concentrations during PBS tests.

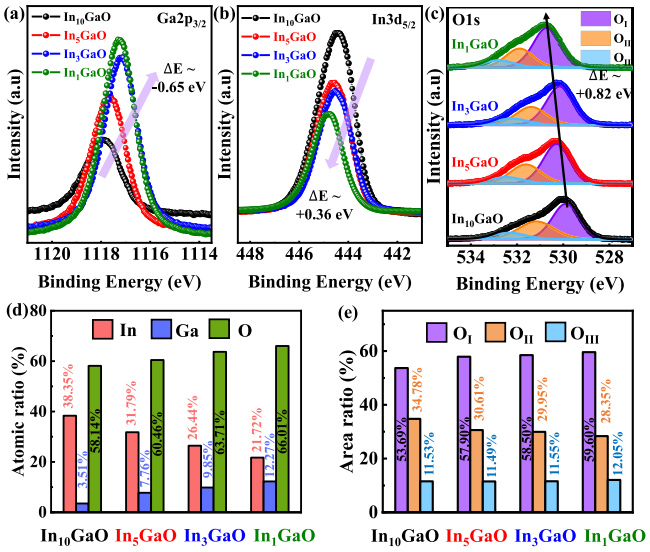

Fig. 8. XPS spectra for (a) Ga $2p_{3/2}$, (b) In $3d_{5/2}$, and (c) O 1s core levels of InGaO films with T_{ch} of 3 nm. (d) Composition analysis. (e) Area ratios of the deconvoluted subpeaks in the O 1s spectra.

electronic characteristics of the interface traps are acceptor-like, which may not be applicable to In-rich oxides. We propose that the differing ΔV_{th} behaviors can be qualitatively explained by the trap neutrality level (TNL) model depicted in Fig. 7 [9]. The TNL is defined as the energy level (E_{TNL}) at which the positively charged donor-like traps are balanced by the negatively charged acceptor-like traps. Donor-like traps are positively charged when their energy level lies above E_F and are neutral when below it. In contrast, acceptor-like traps are neutral when above E_F and become negatively charged when below it. Therefore, the distinct ΔV_{th} responses observed in In_XGaO transistors likely originate from variations in the nature and energy distribution of interface traps, depending on where the E_F stabilizes during gate bias stress. For In-rich InGaO transistors, abundant oxygen vacancies arise from weak In-O bonds, and these vacancies can function as donor-like traps through ionization under high electric fields [27], leading to the observed anomalous negative ΔV_{th}. Because of the strong oxygen-gettering effects of Ga, these oxygen vacancies can be significantly reduced. Furthermore, increased Ga concentration may introduce excess oxygen. These peroxide states have been reported to act as acceptor-like traps, contributing to positive ΔV_{th} [28]. Consequently, it is believed that the electronic signature of interface traps determines the polarity of ΔV_{th}, and Ga incorporation effectively shifts this signature from donor-like to acceptor-like due to its strong oxygen-gettering capacity. Because of the ultrathin channel/dielectric structure and identical HfO_2 grown in the same ALD run, charge trapping in the gate dielectric was not further considered, as interface traps are likely the dominant factor influencing ΔV_{th} differences. The trap energy levels are positioned near the conduction band in our In_XGaO films due to their high indium content, which pins the defect states near the conduction band, similar to pure In_2O_3 [31].

C. XPS Analysis

To provide material evidence supporting our proposed TNL model, the chemical composition of the ALD In_XGaO films was analyzed using XPS, as illustrated in Fig. 8. Approximately 10% atomic percentage of carbon and nitrogen contamination was observed in all In_XGaO films, originating from precursor materials or surface adsorbates. Given the comparable contamination levels across all samples, these impurities are unlikely to be responsible for the observed ΔV_{th} transitions under PBS conditions in the In_XGaO transistors. As expected, the intensity of the In $3d_{5/2}$ spectrum decreases, while the intensity of the Ga $2p_{3/2}$ spectra increases with higher Ga concentrations. Both the In $3d_{5/2}$ and O 1s spectra exhibit positive shifts, with respective ΔE values of +0.36 and +0.82 eV as the X value decreases from 10 to 1. In contrast, a negative shift with ΔE of −0.65 eV is observed in the Ga $2p_{3/2}$ spectrum. This behavior can be attributed to the higher bond energy of Ga-O bonds (374 kJ/mol) compared to In-O bonds (346 kJ/mol) [19], [20]. Consequently, incorporating more Ga enhances oxygen binding in the InGaO system, resulting in the observed positive shifts in the O and In spectra. Additionally, the high ionic potential of Ga attracts more electrons around the Ga atoms, explaining the negative shift in the Ga spectrum [29].

Fig. 8(d) presents the composition analysis of these In_XGaO films, showing that the atomic ratio of In decreases from 38.35% to 31.79%, 26.44%, and 21.72% as the X value reduces from 10 to 5, 3, and 1, respectively. In contrast, the atomic ratio of Ga increases from 3.51% to 7.76%, 9.85%, and 12.27%, indicating the substitution of Ga atoms for In atoms in the In_2O_3 host. Notably, the atomic ratio of O also increases from 58.14% to 60.46%, 63.71%, and 66.01% as the X value decreases from 10 to 5, 3, and 1, suggesting strong oxygen gettering effects of Ga. Quantification of composition by XPS was performed by integrating the peak areas of the core-level spectra (In 3d, Ga 2p, and O 1s), corrected using Scofield sensitivity factors. This is further supported by the deconvolution analysis of the O 1s spectrum in Fig. 8(c), where the spectrum can be deconvoluted into three subpeaks: O_I (oxygen atoms bound to metal), O_{II} (oxygen deficiency), and O_{III} (surface hydroxyl). As the X value decreases from 10 to 5, 3, and 1, the area percentage of O_I increases from 53.69% to 57.90%, 58.50%, and 59.60% with increasing Ga concentration. Conversely, the area percentage of O_{II} decreases from 34.78% to 30.61%, 29.95%, and 28.35%, while the area percentage of O_{III} remains relatively stable at values of 11.53%, 11.49%, 11.55%, and 12.05%. Thus, the incorporation of Ga leads to an increase in oxygen content within the InGaO systems, resulting

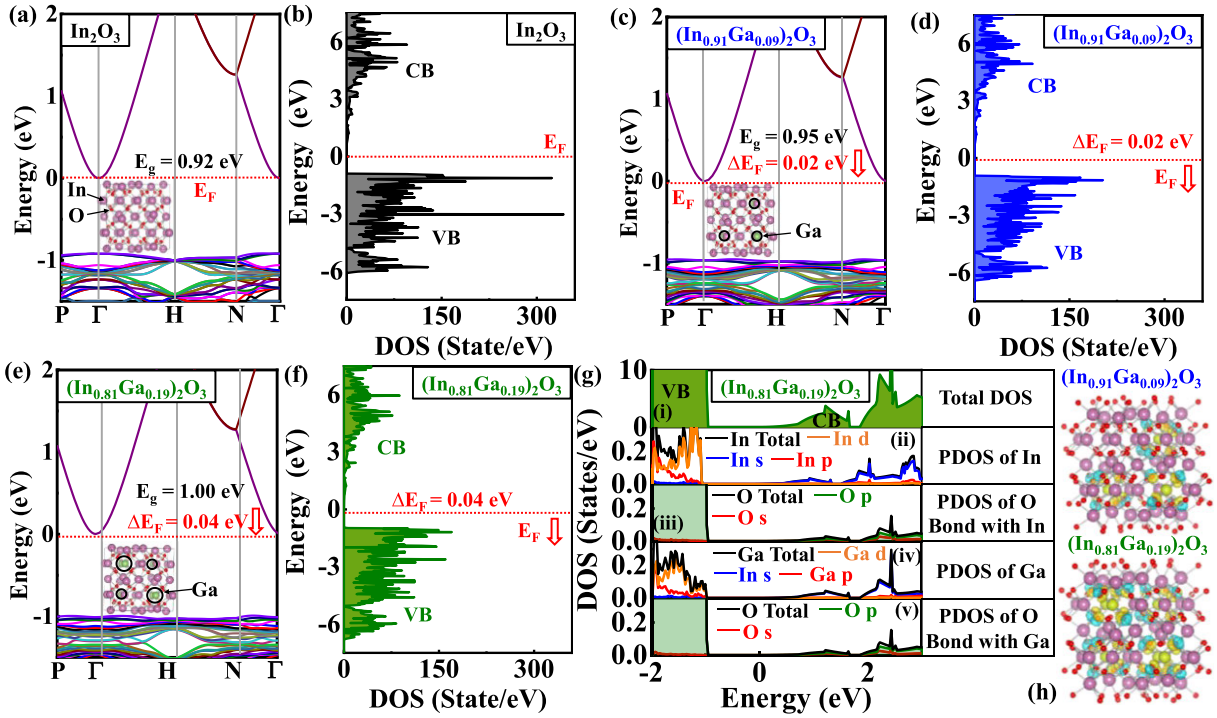

Fig. 9. DFT calculations for In_XGaO. (a) and (b) Band structure and DOS for In_2O_3; (c) and (d) $(In_{0.91}Ga_{0.09})_2O_3$; (e) and (f) $(In_{0.81}Ga_{0.19})_2O_3$. Insets: corresponding atomic structures. (g) Partial DOS of $(In_{0.81}Ga_{0.19})_2O_3$. (h) Spatial charge distribution of $(In_{0.91}Ga_{0.09})_2O_3$ $(In_{0.81}Ga_{0.19})_2O_3$ relative to In_2O_3.

in a greater proportion of oxygen bound to metal atoms and a reduction in oxygen vacancies or weakly bonded oxygen species. This provides direct material evidence supporting our proposed TNL model, which can be attributed to the stronger oxygen-bonding capability of Ga atoms.

D. DFT Calculation

To elucidate the atomistic effects of Ga doping, DFT calculations were performed on stoichiometric In_2O_3 using a supercell comprising 32 In atoms and 48 O atoms, as well as on $(In_{0.91}Ga_{0.09})_2O_3$ and $(In_{0.81}Ga_{0.19})_2O_3$, where 3 and 6 Ga atoms replace In atoms in In_2O_3 host, respectively. The crystalline In_XGaO model serves as a reasonable approximation of amorphous In_XGaO because In-based oxides are known to be largely insensitive to crystallinity and local structural randomness [30], primarily due to the conduction bands formed by the spherical In orbitals. Fig. 9(a)–(f) present the calculated band structure and total density of states (DOSs) for In_2O_3, $(In_{0.91}Ga_{0.09})_2O_3$, and $(In_{0.81}Ga_{0.19})_2O_3$. Pure In_2O_3 exhibits a direct bandgap structure with a bandgap (E_g) value of 0.92 eV, with both the conduction band minimum (CBM) and valence band maximum (VBM) located at the Γ point. This calculated E_g value is significantly smaller than the experimental value, which typically exceeds 3 eV, due to unoptimized atomic pseudopotentials, a known issue in the DFT community [31]. Consequently, the relative changes in E_g values upon Ga incorporation, rather than the absolute E_g values, are of primary importance.

Interestingly, the E_F, defined as the zero-energy position of pure In_2O_3, is located at the CBM, indicating n-type conduction with semi-metallic properties [31]. Upon Ga incorporation, the E_g value increases to 0.95 eV for $(In_{0.91}Ga_{0.09})_2O_3$ and 1 eV for $(In_{0.81}Ga_{0.19})_2O_3$. Additionally, a downward shift of E_F from CBM toward the bandgap is observed with increased Ga incorporation, with shifts of 0.02 eV for $(In_{0.91}Ga_{0.09})_2O_3$ and 0.04 eV for $(In_{0.81}Ga_{0.19})_2O_3$. Fig. 9(g) illustrates the partial DOS for $(In_{0.81}Ga_{0.19})_2O_3$. The VBM is predominantly influenced by O 2p orbitals, with contributions from In 4d and Ga 3d orbitals, while the CBM is primarily composed of In 5s and Ga 4s orbitals, alongside contributions from O 2s and 2p orbitals. These partial DOS results indicate that the band structure arises from cation-anion hybridization [29], [30], and the smaller radius and shorter bond lengths of Ga lead to stronger orbital hybridization with O than that of In. The enhanced p–d repulsion between Ga and O results in a downshift of the VBM and a slight upshift of the CBM, explaining the observed increase in E_g and the downward shift of E_F upon Ga incorporation.

Fig. 9(h) further illustrates the spatial charge distribution of $(In_{0.91}Ga_{0.09})_2O_3$ and $(In_{0.81}Ga_{0.19})_2O_3$ compared to In_2O_3, showing that more electrons localize at the Ga-O bonds, while fewer electrons are found around the surrounding In-O bonds. This behavior can be attributed to the higher ionic potential and greater bonding energy of Ga with oxygen compared to In [19], [20], suggesting a reduced tendency for oxygen vacancy formation upon Ga incorporation. Therefore, Ga incorporation not only alters the band structure of the InGaO system but also reduces oxygen vacancies, which could modify the electronic signature of interface traps from donor-like to acceptor-like.

IV. Conclusion

In summary, we systematically investigated the effects of Ga incorporation on electron transport and bias stability in

ultrascaled InGaO transistors, featuring a T_{ch} of 3 nm and an L_{ch} down to 60 nm, using ALD techniques. Our findings reveal that Ga atoms act as effective carrier suppressors and potential trap sites within the In_2O_3 host, leading to reduced current drivability, a positively shifted V_{th}, decreased μ_{FE}, and an enlarged hysteresis window. Moreover, a transition of ΔV_{th} from negative to positive during PBS tests can be observed with increasing Ga concentration. This is attributed to a change in the electronic signature of interface traps, where the E_F of InGaO resides, shifting from donor-like to acceptor-like characteristics upon Ga incorporation. The strong oxygen-gettering capacity of Ga is believed to reduce oxygen vacancies, which function as donor-like traps, while introducing excess oxygen states that serve as acceptor-like traps. This study offers crucial guidance for achieving ultrascaled In_2O_3-based transistors with positive V_{th}, high ON-current, and excellent bias stability simultaneously.

REFERENCES

[1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, "Back-end-of-line compatible transistors for monolithic 3-D integration," *IEEE Micro*, vol. 39, no. 6, pp. 8–15, Nov. 2019, doi: 10.1109/MM.2019.2942978.

[2] A. Charnas et al., "Review—Extremely thin amorphous indium oxide transistors," *Adv. Mater.*, vol. 36, no. 9, Mar. 2024, Art. no. 2304044, doi: 10.1002/adma.202304044.

[3] T. Kim et al., "Progress, challenges, and opportunities in oxide semiconductor devices: A key building block for applications ranging from display backplanes to 3D integrated semiconductor chips," *Adv. Mater.*, vol. 35, no. 43, Oct. 2023, Art. no. 2204663, doi: 10.1002/adma.202204663.

[4] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," *Nature Electron.*, vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: 10.1038/s41928-022-00718-w.

[5] W. Chakraborty, H. Ye, B. Grisafe, I. Lightcap, and S. Datta, "Low thermal budget (<250 °C) dual-gate amorphous indium tungsten oxide (IWO) thin-film transistor for monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5336–5342, Dec. 2020, doi: 10.1109/TED.2020.3034063.

[6] S. Li et al., "Nanometre-thin indium tin oxide for advanced high-performance electronics," *Nature Mater.*, vol. 18, no. 10, pp. 1091–1097, Oct. 2019, doi: 10.1038/s41563-019-0455-8.

[7] S. Samanta, K. Han, C. Sun, C. Wang, A. V.-Y. Thean, and X. Gong, "Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high $G_{m,max}$ of 125 μS/μm at VDS of 1 V and I_{ON} of 350 μA/μm," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITECHNOLOGY18217.2020.9265052.

[8] J. Zhang et al., "Fluorine-passivated In_2O_3 thin film transistors with improved electrical performance via low-temperature CF_4/N_2O plasma," *Appl. Phys. Lett.*, vol. 121, no. 17, Oct. 2022, Art. no. 172101, doi: 10.1063/5.0113015.

[9] Z. Zhang et al., "Reliability of atomic-layer-deposited gate-all-around In_2O_3 nano-ribbon transistors with ultra-high drain currents," in *IEDM Tech. Dig.*, Dec. 2022, pp. 30.3.1–30.3.4, doi: 10.1109/IEDM45625.2022.10019494.

[10] Z. Zhang et al., "Atomically thin indium-tin-oxide transistors enabled by atomic layer deposition," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 231–236, Jan. 2022, doi: 10.1109/TED.2021.3129707.

[11] D. Zheng et al., "First demonstration of BEOL-compatible ultrathin AtomicLayer-deposited InZnO transistors with GHz operation and record high bias-stress stability," in *IEDM Tech. Dig.*, Dec. 2022, pp. 4.3.1–4.3.4, doi: 10.1109/IEDM45625.2022.10019452.

[12] Y.-K. Liang et al., "Aggressively scaled atomic layer deposited amorphous $InZnO_x$ thin film transistor exhibiting prominent short channel characteristics (SS = 69 mV/dec.; DIBL = 27.8 mV/V) and high Gm(802 μS/μm at VDS = 2 V)," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2023, pp. 1–2, doi: 10.23919/VLSITECHNOLOGYANDCIR57934.2023.10185343.

[13] J. Zhang, D. Zheng, Z. Zhang, A. Charnas, Z. Lin, and P. D. Ye, "Ultrathin InGaO thin film transistors by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 273–276, Feb. 2023, doi: 10.1109/LED.2022.3233080.

[14] J. Zhang et al., "Back-end-of-line-compatible scaled InGaZnO transistors by atomic layer deposition," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6651–6657, Dec. 2023, doi: 10.1109/TED.2023.3312357.

[15] A. Chasin et al., "Understanding and modelling the PBTI reliability of thin-film IGZO transistors," in *IEDM Tech. Dig.*, Dec. 2021, pp. 31.1.1–31.1.4, doi: 10.1109/IEDM19574.2021.9720666.

[16] Z. Wu et al., "Characterizing and modelling of the BTI reliability in IGZO-TFT using light-assisted I–V spectroscopy," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2022, p. 30, doi: 10.1109/IEDM45625.2022.10019454.

[17] Q. Kong et al., "New insights into the impact of hydrogen evolution on the reliability of IGZO FETs: Experiment and modeling," in *IEDM Tech. Dig.*, Dec. 2022, p. 30, doi: 10.1109/IEDM45625.2022.10019394.

[18] Z. Lin et al., "Universal PBTI relaxation on the negative V_{TH} shift in oxide semiconductor transistors and new insights," *IEEE Electron Device Lett.*, vol. 44, no. 7, pp. 1136–1139, Jul. 2023, doi: 10.1109/LED.2023.3274771.

[19] J. S. Hur et al., "High-performance thin-film transistor with atomic layer deposition (ALD)-derived indium-gallium oxide channel for back-end-of-line compatible transistor applications: Cation combinatorial approach," *ACS Appl. Mater. Interfaces*, vol. 14, no. 43, pp. 48857–48867, Oct. 2022, doi: 10.1021/acsami.2c13489.

[20] M. H. Rabbi, S. Lee, D. Sasaki, E. Kawashima, Y. Tsuruma, and J. Jang, "Polycrystalline InGaO thin-film transistors with coplanar structure exhibiting average mobility of ≈78 $cm^2\ V^{-1}\ s^{-1}$ and excellent stability for replacing current poly-Si thin-film transistors for organic light-emitting diode displays," *Small Methods*, vol. 6, no. 9, Sep. 2022, Art. no. 2200668, doi: 10.1002/smtd.202200668.

[21] A. Charnas, M. Si, Z. Lin, and P. D. Ye, "Improved stability with atomic-layer-deposited encapsulation on atomic-layer In_2O_3 transistors by reliability characterization," *IEEE Trans. Electron Devices*, vol. 69, no. 10, pp. 5549–5555, Oct. 2022, doi: 10.1109/TED.2022.3198926.

[22] J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 12, Sep. 2008, Art. no. 123508, doi: 10.1063/1.2990657.

[23] P.-Y. Liao et al., "Transient thermal and electrical co-optimization of BEOL top-gated ALD In_2O_3 FETs toward monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 2052–2058, Apr. 2023, doi: 10.1109/TED.2023.3235313.

[24] S. Lee et al., "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 20, May 2011, Art. no. 203508, doi: 10.1063/1.3589371.

[25] A. V. Nenashev, J. O. Oelerich, S. H. M. Greiner, A. V. Dvurechenskii, F. Gebhard, and S. D. Baranovskii, "Percolation description of charge transport in amorphous oxide semiconductors," *Phys. Rev. B, Condens. Matter*, vol. 100, no. 12, Sep. 2019, Art. no. 125202, doi: 10.1103/physrevb.100.125202.

[26] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," *Appl. Phys. Lett.*, vol. 92, no. 3, Jan. 2008, Art. no. 033502, doi: 10.1063/1.2824758.

[27] B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," *Appl. Phys. Lett.*, vol. 97, no. 2, Jul. 2010, Art. no. 022108, doi: 10.1063/1.3464964.

[28] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, "Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 9, Aug. 2011, doi: 10.1063/1.3633100.

[29] J. E. N. Swallow et al., "Indium gallium oxide alloys: Electronic structure, optical gap, surface space charge, and chemical trends within common-cation semiconductors," *ACS Appl. Mater. Interface*, vol. 13, no. 2, pp. 2807–2819, Jan. 2021, doi: 10.1021/acsami.0c16021.

[30] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, Jul. 2009, doi: 10.1109/jdt.2009.2021582.

[31] M. Si et al., "Why In_2O_3 can make 0.7 nm atomic layer thin transistors," *Nano Lett.*, vol. 21, no. 1, pp. 500–506, Jan. 2021, doi: 10.1021/acs.nanolett.0c03967.