Alleviation of Self-Heating Effect in Top-Gated Ultrathin In_2O_3 FETs Using a Thermal Adhesion Layer

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***Abstract*— In this work, a thin layer of hexagonal boron nitride (h-BN) or HfO_2 serves as an adhesion layer between the ultrathin atomic-layer-deposited (ALD) indium oxide (In_2O_3) channel and a sapphire substrate to enhance the thermal interfacial conductance. A thermo-reflectance (TR) measurement system with high spatial resolution is introduced to experimentally demonstrates the improvement. With the thin h-BN or HfO_2 interlayer, the temperature elevation (ΔT) induced by self-heating effect (SHE) is decreased by roughly 9% or 27%, respectively. To quantify the improvement of the interfacial heat transfer, a steady-state thermal diffusion model with a finite-element method is combined with the experimental TR observation to extract the effective thermal boundary conductance (TBC) values in each case. It is shown that the effective TBC is ameliorated by a factor of 2 or 7 with the h-BN or HfO_2 interlayer, which is responsible for the ΔT reduction. Furthermore, phonon density of states (PDOS) distribution mismatch implies that the intersection over union (IOU) ratio in the acoustic phonon region of In_2O_3 with h-BN or HfO_2 is roughly 3 or 11 times higher than that directly with sapphire, which is responsible for the profound TBC enhancement. Based on this, ultra-high maximum drain current of 2.4 mA/μm is achieved with 2.1-nm-thick In_2O_3 channel on a sapphire substrate with an HfO_2 interlayer in between due to the alleviated SHE.**

***Index Terms*— Back-end-of-line (BEOL), indium oxide (In_2O_3), oxide semiconductors, self-heating effect (SHE).**

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I. Introduction

IN THE past few decades, oxide semiconductors have received continuous attention and been broadly explored in thin-film transistor (TFT) applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. Owing to their remarkable properties including low fabrication thermal budget, high carrier mobility, atomically smooth surface roughness, and wafer-level scalability, indium oxide (In_2O_3) [1], [2], [3], [4], [5], [6], [7] and doped indium oxides [8], [9], [10], [11], [12], [13] are especially considered as promising channel materials for next-generation back-end-of-line (BEOL) compatible transistors for monolithic three-dimensional (3-D) integration [14], [15], [16], [17], [18] in recent years.

In_2O_3 has a wide bandgap of roughly 2.9 eV [19]. Due to its exceptional conformality and thickness control enabled by atomic layer deposition (ALD), scaled In_2O_3 transistors have been investigated extensively [1], [2], [3], [4], [5], [6], [7]. It has been reported that the channel thickness (T_{ch}) of In_2O_3 transistors can be down to 0.5 nm, which is as thin as a couple of atoms [1], [2]. On the other hand, the drain current (I_D) of enhancement-mode (E-mode) In_2O_3 transistors with T_{ch} of 1.5 nm, channel length (L_{ch}) of 40 nm, and a back-gate (BG) structure can be up to 2.2 mA/μm at drain voltage (V_{DS}) of 0.7 V [4], [5].

Nevertheless, In_2O_3 devices with top-gate (TG) structures are rarely explored in literature since most of the studies concentrate on BG devices, even though transistors with TG structures are especially needed in practical applications [1], [2], [3], [4], [5]. There are two major difficulties for TG In_2O_3 device investigations, the oxygen vacancy induction during the formation of high-k oxide gate dielectric [18] and the performance deterioration caused by the serious self-heating effect (SHE) [6], [7]. For the former, it is proposed that the pulse of Hf precursor may fetch oxygen atoms from the In_2O_3 channel during the ALD growth of HfO_2 stack, leading to the generation of oxygen defects at the In_2O_3/HfO_2 interface and therefore the degradation of the device transfer characteristics. Fortunately, this issue can be partly overcome by depositing the HfO_2 dielectric layer at relatively low temperature of 120 °C followed by a rapid-thermal-annealing (RTA) treatment

at 250 °C–350 °C [18]. For the latter, SHE happens when the power density (PD) of the device is too high. PD is defined as

$$\mathrm{PD} = \frac{P}{A} = \frac{I_D \times V_{\mathrm{DS}}}{L_{\mathrm{ch}} \times W_{\mathrm{ch}}}$$

where P denotes the power, A denotes the channel area, I_D denotes the drain current, V_{DS} denotes the drain-to-source bias, L_{ch} denotes the channel length, and W_{ch} denotes the channel width. As the applied V_{DS} is large and the I_D becomes high, huge amount of thermal energy will be generated at the atomically thin channel. If the heat cannot be dissipated efficiently, the temperature at the channel region will elevate dramatically. Consequently, the local high temperature may degrade not only the channel material and the dielectric layer but also the interface between them, resulting in the unstability of the device and the non-ideal transport characteristics. This phenomenon is therefore called SHE, and it also significantly damages the long-term reliability of the devices [20], [21].

Because of the extensive commercial availability and favorable affordability, silicon dioxide on silicon (SiO_2/Si) is often employed as the substrate for TG In_2O_3 transistor fabrication in the previous investigations [1], [2], [3], [4], [5]. However, a substrate with better heat-transfer capability is desired to alleviate the self-heating issue. Sapphire, which has been utilized as the substrate material in other power devices [22], [23], [24], is more thermally advantageous considering its high thermal conductivity (κ) of 40 $\mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$ [25] compared with that of SiO_2 (1.5 $\mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$ [26]). The higher κ of sapphire implies preferable heat dissipation potential. Nonetheless, it is found that the thermal boundary conductance (TBC) at the In_2O_3/sapphire interface is far from ideal, limiting the benefits of SHE reduction that sapphire can conduct. Moreover, TBC between wide bandgap semiconductors and high thermal conductivity substrates has been a concern for FET applications in other materials [27], [28], [29], [30]. Therefore, even though thermal management has been applied to In_2O_3 and other material systems where substrates with higher κ such as sapphire are utilized to assist transferring thermal energy to deal with SHE, additional explorations to thermally improve the interface between the In_2O_3 channel and the substrate are still desired [6], [7], [24]. We can call these efforts as interface thermal engineering.

It is reported that a thermal adhesion layer as thin as 1 nm is sufficient to increase the TBC by more than a factor of 4 at the Au/sapphire interface [31]. Herein, a thin layer of h-BN or ALD HfO_2 is similarly introduced as a thermal adhesion layer between the In_2O_3 channel and the sapphire substrate. To experimentally demonstrate the difference between devices with and without the presence of an interlayer, a thermoreflectance (TR) measurement system with high spatial resolution is employed to observe the temperature increase (ΔT) caused by SHE. The ΔT of TG In_2O_3 transistors with the h-BN or HfO_2 adhesion layer induced by SHE is shown to drop by 9% or 27%, compared to that without the interlayer. Through heat-transfer simulation and phonon density of state (PDOS) calculation, it is revealed that the TBC at the interface is improved by a factor of 2 or 7, and this is due to the higher value of the intersection over union (IOU) ratio in the PDOS acoustic region of In_2O_3 with h-BN or HfO_2 than that with sapphire by a factor of 3 or 11. Consequently, TG In_2O_3 transistors achieving extremely high I_D of 2.4 mA/μm are realized with T_{ch} of 2.1 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm on a sapphire substrate with a thin HfO_2 thermal adhesion layer. Even with such high PD, there is no observable performance degradation due to the reduced SHE.

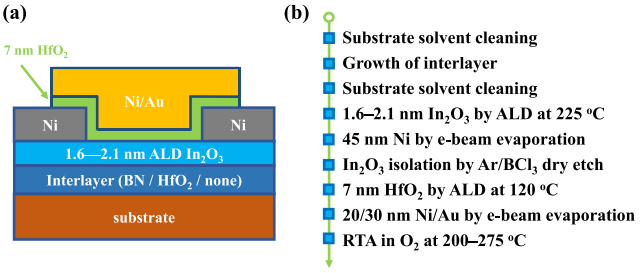

Fig. 1. (a) Cross-sectional illustration of device structure and (b) fabrication flow of TG In_2O_3 transistors with a thermal adhesion interlayer.

II. Experiments

Fig. 1(a) and (b) illustrates the schematic and fabrication flow of TG In_2O_3 transistors. The substrate was either p+ silicon with 90-nm thermally grown silicon dioxide (SiO_2/Si) or sapphire. At first, standard solvent cleaning process was applied to the substrates to ensure the surface cleanness. There was no interlayer as SiO_2/Si served as the substrate while bi-layer (2L) of hexagonal boron nitride (h-BN) or 4 nm of HfO_2 on sapphire served as the substrate. The 2L h-BN was formed by chemical vapor deposition (CVD) while the 4-nm HfO_2 was grown by ALD at 200 °C with $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as the Hf and O precursors, respectively. Being limited by CVD process of h-BN on sapphire, only 2L h-BN can be formed instead of thicker h-BN film. Standard solvent cleaning steps were followed again at this point before the deposition of the channel layer.

An 1.6–2.1 nm of In_2O_3 ultrathin film was conformally grown by ALD at 225 °C with trimethylindium (TMIn) and H_2O as the In and O precursors, respectively, on the well-cleaned substrates with or without an interlayer, followed by an Ar/BCl_3 plasma dry-etch step for channel region isolation. Next, 45 nm of Ni as source and drain (S/D) contacts with variant L_{ch} was formed by e-beam lithography (EBL), e-beam deposition, and a lift-off process. At the step of EBL patterning, diluted ZEP 520A served as the e-beam resist. With a sapphire substrate, DisCharge H_2O was applied as an anti-charging agent on top of the e-beam resist because of the electrical insulation property of sapphire. The anti-charging agent was removed by 2-propanol (isopropyl alcohol, IPA) before development. Then, 7-nm HfO_2 as TG dielectric layer was deposited by ALD at 120 °C where the relatively low temperature was for the minimization of the interaction between the HfO_2 and In_2O_3 layers as mentioned. On the top, a Ni/Au of 20-/30-nm metal stack as the gate contact was defined by the identical process as the S/D contacts.

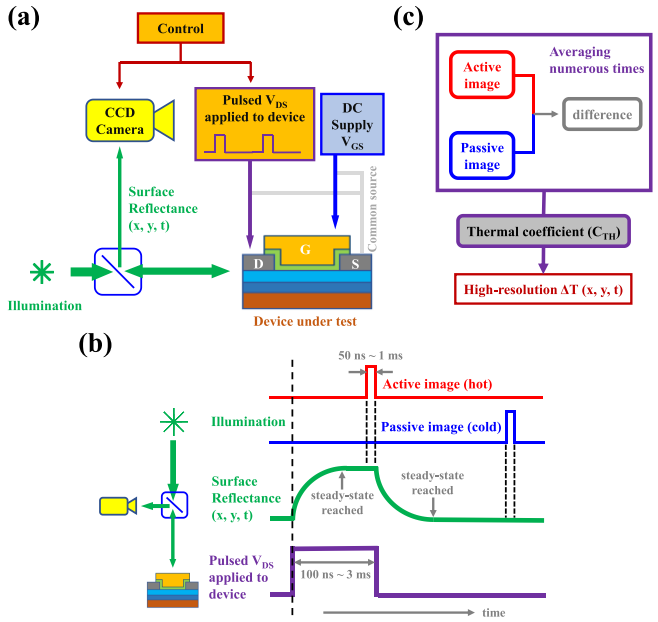

Fig. 2. (a) Schematic of the high spatial resolution TR imaging equipment setup. (b) Working mechanism of the TR measurement system in time domain. (c) Transformation process from TR signal to a temperature scale.

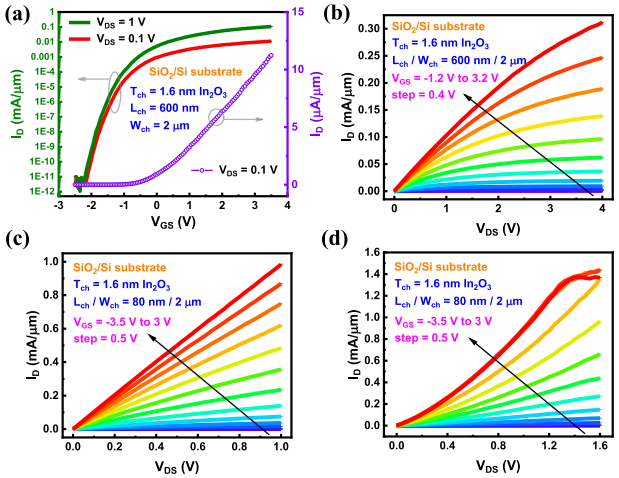

Fig. 3. (a) Transfer and (b) output characteristics of a TG In_2O_3 transistor with a long L_{ch} of 600 nm on a SiO_2/Si substrate, exhibiting large ON–OFF ratio of more than 11 orders. Output characteristics of a TG In_2O_3 transistor with a short L_{ch} of 80 nm and V_{DS} of (c) 1.0 and (d) 1.6 V on a SiO_2/Si substrate. Severe SHE degrades the device performance in (d).

The whole fabrication flow ended with an RTA treatment at 200 °C–275 °C for 2 min in an O_2 environment to annihilate the oxygen vacancies. Dedicated ALD chambers for HfO_2 and In_2O_3 growth were utilized to circumvent cross-contamination throughout the steps, and the thickness of HfO_2 and In_2O_3 films were measured by Gaertner L116A ellipsometer calibrated by transmission electron microscopy (TEM) and atomic force microscopy (AFM) as presented in our previous reports [1], [2], [3], [17], [18].

Fig. 2(a) exhibits the setup of the high-resolution TR measurement system employed to quantitatively explore and address the SHE in this work. Periodic V_{DS} pulses and a direct-current (dc) gate-to-source (V_{GS}) bias are applied to the device under test by dedicated suppliers to generate heat. Besides, high-speed green LED pulses (wavelength of 530 nm) are adopted to illuminate the device, and a synchronized charge-coupled device (CCD) camera is used to capture the surface reflectance.

Fig. 2(b) reveals the working mechanism of the system in time domain. As a V_{DS} pulse starts, the device is turned on and therefore heated up. After the steady state is reached, TR signal is captured by the synchronized CCD camera as an active image. On the other hand, at the end of the V_{DS} pulse, the device is turned off and consequently cooled down. After the steady state is reached, TR signal is captured as a passive image. This process is repeated numerous times, and the difference between the active and passive images is averaged accordingly to maximize the signal-to-noise ratio as illustrated in Fig. 2(c). The TR signal is transformed into a temperature scale through diving the values by the calibrated TR coefficient of the surface material ($C_{TH,Au} = -2.5 \times 10^{-4}$ K^{-1}) to obtain the final thermal image [23], [32], [33].

III. Results and Discussion

Fig. 3(a) and (b) shows the transfer and output characteristics of a representative TG In_2O_3 transistor with T_{ch} of 1.6 nm, long L_{ch} of 600 nm, and W_{ch} of 2 μm on a SiO_2/Si substrate, respectively. The device operates at E-mode with threshold voltage of 0.08 V, and the subthreshold swing (SS) is as low as 150 mV/dec. The ON–OFF ratio is larger than 11 orders of magnitude, specifying decent switching behaviors. Fig. 3(c) and (d) exhibits the output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.6 nm, short L_{ch} of 80 nm, and W_{ch} of 2 μm on a SiO_2/Si substrate, and V_{DS} applied are 1.0 and 1.6 V, respectively. The V_{GS} sweeps from –3.5 to 3 V with a 0.5-V step, and the maximum I_D achieves 1 mA/μm at V_{GS} of 3 V and V_{DS} of 1 V. Nevertheless, as V_{DS} is enlarged to 1.6 V, the I_D–V_{DS} curves appear in Schottky-like shapes and gradually start dropping with the increased V_{GS}. This implies the unstability of the device due to the severe SHE.

Sapphire, given much higher thermal conductivity compared to SiO_2, is utilized to replace SiO_2/Si as the substrate to assist alleviating the acute SHE. However, because of its inferior TBC with the In_2O_3 stack, the heat-transfer capability of sapphire is restricted to some degree. Therefore, a thermal adhesion layer of h-BN or HfO_2 is inserted in between to enhance the effective TBC. Fig. 4(a) and (b) exhibits the ΔT distribution around the channel region of a TG In_2O_3 transistor on a sapphire substrate with L_{ch} of 400 nm, W_{ch} of 2 μm, and no interlayer at PD of approximately 5 kW/mm^2 in a 3-D plot and a heat map, respectively. Likewise, Fig. 4(c)–(f) presents the devices with identical structure and dimensions but an inserted layer of h-BN or HfO_2 at similar PD. In all the three cases, the ΔT distributes in bell-like shapes with high plateaus in the middle of the device, descending to their proximity. It is noticeable that the device without a thermal adhesion layer shows the highest ΔT while the one with an HfO_2 interlayer exhibits the lowest.

For a clearer comparison, the cross sections of Fig. 4(b), (d), and (f) along the direction of channel width are plotted into

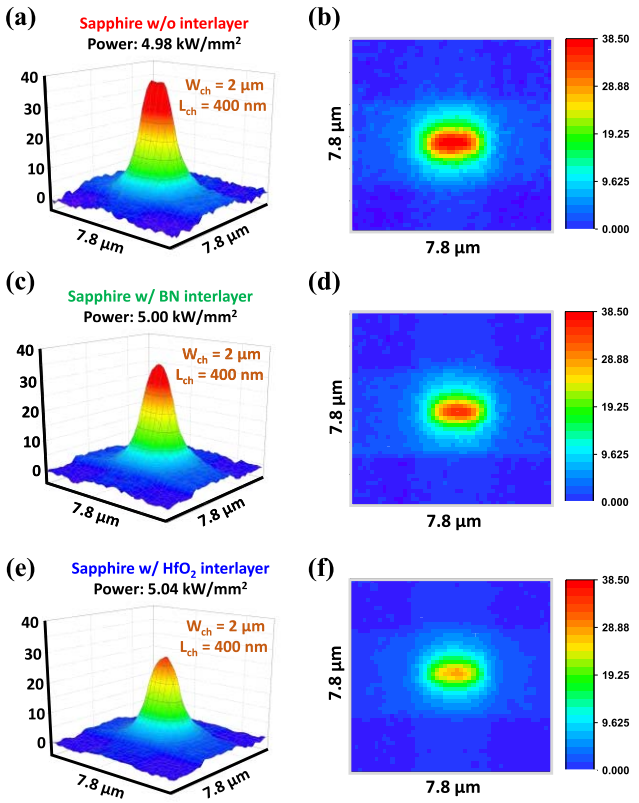

Fig. 4. ΔT (a) 3-D plot and (b) heat map of a TG In_2O_3 transistor with W_{ch} of 2 μm, L_{ch} of 400 nm, and no interlayer on a sapphire substrate at PD of roughly 5 kW/mm^2 imaged by the TR measurement system. The corresponding plots of the devices with the same structure, dimensions, but a thermal adhesion layer of (c) and (d) 2L h-BN, and (e) and (f) 4-nm HfO_2 at similar PD.

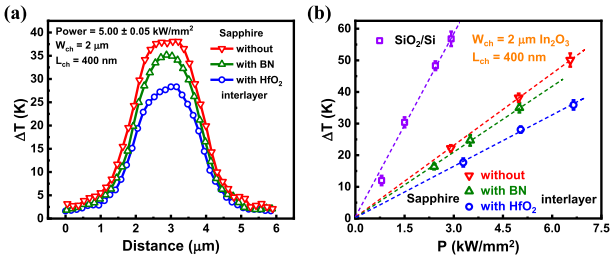

Fig. 5. (a) Cross sections of the three ΔT plots along the direction of channel width, showing 9% or 27% alleviation of the SHE by inserting a thermal adhesion layer of h-BN or HfO_2, respectively. (b) Comparison between devices with different substrates and interlayers and variant PD. Great linearity is agreed in all cases.

Fig. 5(a). With identical dimensions and similar PD, the TG In_2O_3 devices without a thermal adhesion layer, with 2L h-BN, and with 4-nm HfO_2 demonstrate maximum ΔT of 38.2, 35.0, and 28.1 K, respectively. This suggests that a 9% or 27% of ΔT reduction is obtained by inserting a thin thermal adhesion layer of h-BN or HfO_2 between the In_2O_3 channel and the sapphire substrate. Besides, the maximum ΔT with cases of different substrates and interlayers at variant PD is arranged into Fig. 5(b) where the error bars indicate 95% confidence intervals. Observably, the maximum ΔT of a certain device

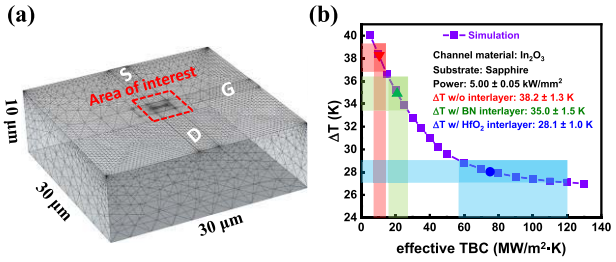

Fig. 6. (a) Mesh build-up of the thermal diffusion model for heat transfer simulation with a finite-element method. The area of interest is indicated by the red-dashed square. (b) Maximum ΔT at the steady state extracted by setting variant effective TBC. Considering the experimental ΔT error ranges, ranges of effective TBCs are corresponded accordingly.

is roughly proportional to the PD in all cases. Moreover, at the same PD, the ΔT decreases by a factor of 2.5 through replacing the SiO_2/Si substrate with sapphire and by a factor of 2.8 or 3.7 through replacing that with BN/sapphire or HfO_2/sapphire, respectively. This specifies the alleviation of SHE in TG In_2O_3 transistors by interface thermal engineering.

Although h-BN has much higher thermal conductivity (390 W·m^{-1}·K^{-1} [34]) than HfO_2 (1.2 W·m^{-1}·K^{-1} [35]), devices with HfO_2 interlayer performs 3× larger ΔT reduction. This suggests that the thermal interfacial conductance is significant here. The insertion of the thermal adhesion layer eliminates the interface of In_2O_3/sapphire but brings in another two interfaces of In_2O_3/interlayer and interlayer/sapphire. By the TR imaging and maximum ΔT comparison discussed, it is observable that the effective TBC of the devices with a h-BN or HfO_2 interlayer is larger than the TBC of the devices without one. To quantify the improvement, a steady-state thermal diffusion model with a finite-element method is combined with the TR imaging results to extract the effective TBC values. It is verified in literature that this method of TBC extraction is consistent with experimentally measured TBC values [36], [37].

The steady-state thermal simulation is carried out through COMSOL Multiphysics which adopts a finite-element method. Fig. 6(a) demonstrates the mesh build-up of the model which is designed to have identical structures and dimensions (L_{ch} of 400 nm and W_{ch} of 2 μm) with the devices used in Fig. 3. The PD is set to be around 5 kW/mm^2 which is the same as the scenarios in Fig. 3 as well, and the square indicated by the red dashed lines denotes the area of interest which includes the channel region and its proximity. By giving variant effective TBC values of the introduced interfaces, different values of maximum ΔT are obtained as shown in Fig. 6(b). Considering the experimental ΔT values with the error ranges, the corresponding TBC implied by the steady-state simulation for the devices without an interlayer is extracted to be 11 +4/−4 MW/(m^2·K). Similarly, the effective TBC of the devices with a thermal adhesion layer of h-BN or HfO_2 is extracted to be 21 +6/−5 MW/(m^2·K) or 75 +45/−19 MW/(m^2·K), which is 2 or 7 times larger than the original value, respectively. The huge improvement of effective TBC suggests that the interlayer of h-BN or HfO_2 enhances the heat dissipation that sapphire is capable of, benefiting the SHE alleviation in TG In_2O_3 transistors.

The obtained effective TBC, including contributions from both the introduced interfaces and the interlayer itself, equals to the inverse of the sum of the inversed thermal conductance of the three contributions. The thermal conductance of the interlayer itself is defined as the thermal conductivity divided by the thickness. It is revealed that thermal conductivity of a thin film is more dependent on its thickness as the thickness is down to the same order of magnitude of the energy carriers' mean free path [38], [39]. Considering the thin-film thermal conductivity of the 4-nm HfO_2 (0.5–1.0 $W{\cdot}m^{-1}{\cdot}K^{-1}$ [40]) or 2L h-BN (out-of-plane thermal conductivity 2.3–3.5 $W{\cdot}m^{-1}{\cdot}K^{-1}$ [41]) thermal adhesion layer, the TBC contribution from the interlayer itself is roughly 125–250 $MW/(m^2{\cdot}K)$ or 1900–3500 $MW/(m^2{\cdot}K)$, respectively. The TBC contributions are larger than their individual effective TBC values, indicating that the interlayer itself may not be a critical thermal bottleneck for the effective TBC in either case.

Beside the interlayer itself, there are two introduced interfaces by the insertion of the interlayer, namely, interlayer/sapphire and In_2O_3/interlayer. For the former, the experimentally demonstrated TBC of HfO_2/sapphire interface by time-domain TR (TDTR) is around 227–327 $MW/(m^2{\cdot}K)$ [36], which is much larger than the effective TBC of 75 $MW/(m^2{\cdot}K)$. Besides, the TBC of h-BN/sapphire is reported to be 980 $MW/(m^2{\cdot}K)$ [42] which is also even higher than the effective TBC of 21 $MW/(m^2{\cdot}K)$. Consequently, the TBC contribution from the interlayer/sapphire interface is not a main concern in each case, either.

Therefore, the bottleneck of the effective TBC could be the In_2O_3/interlayer interface. Here, phonons as the energy carriers play a significant role. Especially, phonons at lower frequency, called acoustic phonons, are attributed to most of the heat transport behaviors [43]. To investigate the behaviors, the PDOS distributions of HfO_2 and sapphire were obtained from [36] and [44], and the PDOS distribution calculations of h-BN and In_2O_3 were performed by density functional theory (DFT) as implemented in Vienna Ab initio Simulation Package (VASP) [45], [46]. The two calculations on h-BN and In_2O_3 followed different pathways due to the differences in their material properties. A bilayer h-BN with vacuum above and below was constructed to replicate the 2L interlayers in the device. The projector augmented wave (PAW) [47] method was adopted along with optB86-vdW [48] functional due to the presence of van der Waals forces based on previous work [49]. An energy cut-off of 600 eV was involved together with a $9 \times 9 \times 3$ Monkhorst-Pack k-point mesh for structure optimization of the four-atom bilayer unit cell. Density functional perturbation theory (DFPT) was applied for calculating the second-order force constants on a $6 \times 6 \times 1$ supercell with a $3 \times 3 \times 2$ k-point grid. The required PDOS were acquired using an open-source package Phonopy [50]. The calculated phonon dispersion of 2L h-BN is revealed in Fig. 7(a), and its resultant PDOS distribution is demonstrated in Fig. 7(b). For In_2O_3, the PAW method was used alongside LDA functional with a cut-off of 520 eV. The 40-atom cubic unit cell was optimized utilizing a $4 \times 4 \times 4$ Monkhorst-Pack k-point mesh. A supercell of $2 \times 2 \times 2$ was constructed with a $2 \times 2 \times 2$ k-point mesh for the second-order force constants calculations. However, DFPT is not applicable for In_2O_3 due to the large computational expense of the method for this complicated structure. Hence, the finite differences method for force constants calculation was adopted instead. Similar to h-BN, Phonopy was employed for post-processing and obtaining the PDOS of In_2O_3. The calculated phonon dispersion of In_2O_3 is shown in Fig. 7(c), and its resultant PDOS distribution is demonstrated in Fig. 7(d).

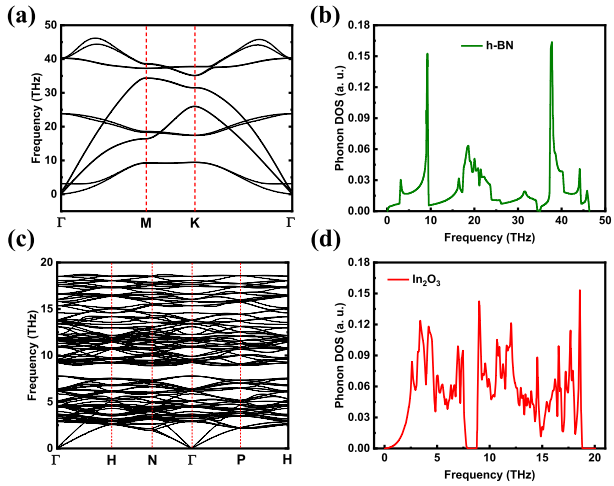

Fig. 7. Phonon dispersion of (a) h-BN and (c) In_2O_3 performed by DFT calculation and (b) and (d) resultant PDOS distributions of them.

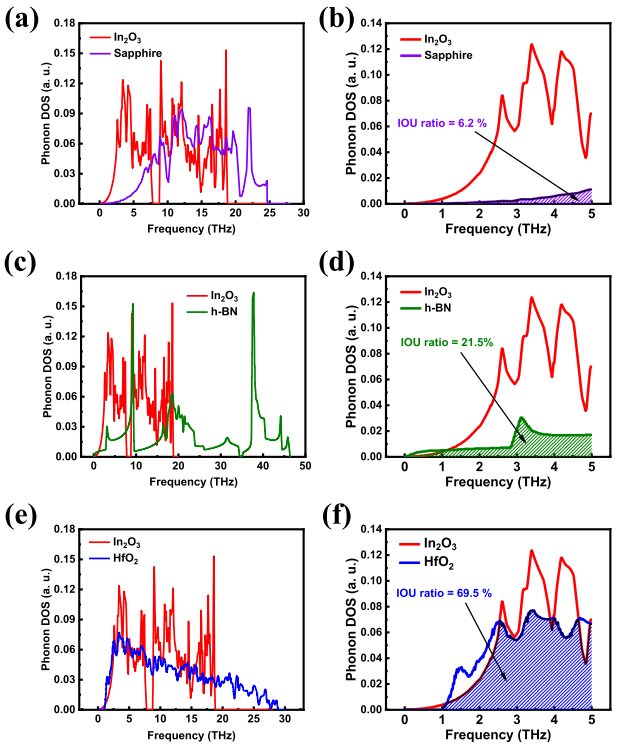

Fig. 8. PDOS distribution comparison between In_2O_3 and (a) sapphire, (c) h-BN, and (e) HfO2 and (b), (d), and (f) their acoustic phonon region magnification (frequency lower than 5 THz). The IOU ratio between PDOS distributions of sapphire, h-BN, and HfO_2 and that of In_2O_3 in the acoustic phonon region are 6.2%, 21.5%, and 69.5%, respectively.

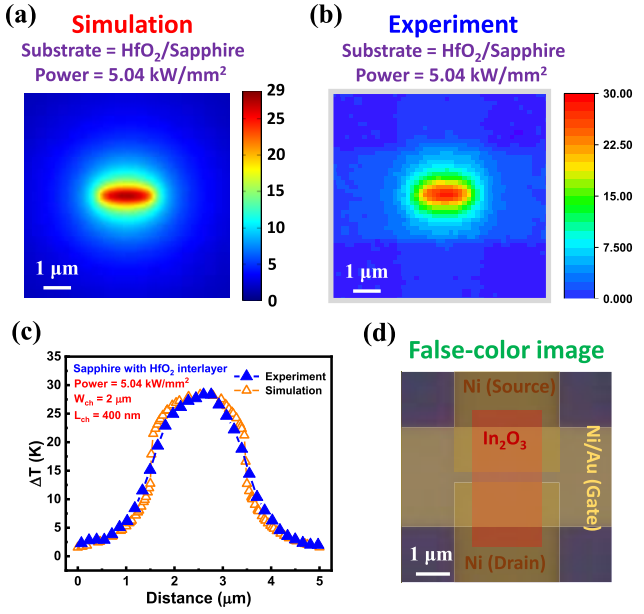

Fig. 9. (a) Simulated ΔT distribution around the channel region of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm on a sapphire substrate with HfO_2 interlayer at PD of 5 kW/mm$_2$. (b) Experimental ΔT distribution of the same region of a transistor with identical structure and dimensions at the same PD imaged by the high-resolution TR equipment. (c) Cross-sectional comparison along the channel width direction of the experimental and simulation results. (d) False-color image of a TG In_2O_3 transistor with the same structure and dimensions for better visualization of the SHE.

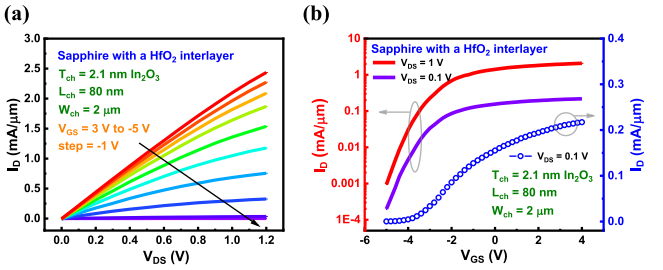

Fig. 10. (a) Output and (b) transfer characteristics of a 2.1-nm-thick TG In_2O_3 transistor with L_{ch} of 80 nm and W_{ch} of 2 μm on a sapphire substrate with a HfO_2 thermal adhesion layer. Due to the great heat-transfer properties of the substrate, SHE is negligible, and maximum I_D of 2.4 mA/μm is achieved at V_{DS} of 1.2 V. The ON–OFF ratio is larger than 3 orders of magnitude.

Fig. 8 exhibits the PDOS distributions of sapphire, h-BN, and HfO_2 with that of In_2O_3 where Fig. 8(a), (c), and (e) shows the comparisons of the whole distributions while Fig. 8(b), (d), and (f) illustrates the acoustic region magnification (frequency lower than 5 THz). All the distributions are normalized by setting the integration area to be one (1). IOU ratio is here used to evaluate how well two distributions match with each other and defined as the ratio of their intersection area and their union area. As demonstrated in Fig. 8(b), the IOU ratio between PDOS of sapphire and In_2O_3 in the acoustic phonon region is only 6.2%, explaining the low TBC of 11 +4/−4 MW/(m^2·K). On the other hand, Fig. 8(d) and (f) indicates that the IOU ratios in the acoustic phonon region with h-BN and HfO_2 employed are improved to 21.5% and 69.5%, which are 3 and 11 times larger than 6.2%, respectively. Due to the much larger IOU ratios in the acoustic phonon region of the PDOS distributions, heat transfer is much more efficient with the presence of the h-BN or HfO_2 interlayer in TG In_2O_3 devices with a sapphire substrate, especially HfO_2. Accordingly, the effective TBC of: 1) In_2O_3/interlayer interface; 2) thin h-BN or HfO_2 stack; and 2) interlayer/sapphire interface as a whole is considered satisfactory and improved from the structure without the thermal adhesion layer, which is responsible for the 9% or 27% of the SHE alleviation observed by the TR imaging, respectively.

With the extracted effective TBC, the steady-state ΔT distribution is demonstrated in Fig. 9(a) where the case with HfO_2 interlayer at PD of around 5.04 kW/mm^2 is simulated. For clearer comparison, the TR image of Fig. 4(f) is re-plotted with a modified rainbow-color scale into Fig. 9(b) where the device with HfO_2 interlayer at PD of 5.04 kW/mm^2 is measured. Fig. 9(a) and (b) shows in excellent agreement, specifying that the experiments and simulation lead to extremely consistent results and support each other. The cross sections of Fig. 9(a) and (b) along the direction of channel width are revealed in Fig. 9(c). The two curves are alike and only off a little near the edge of the channel where the experimental curve is smoother while the simulation curve is sharper. On the other hand, Fig. 9(d) exhibits a false-color image of a TG In_2O_3 transistor with the same structure and dimensions. By comparing Fig. 9(a), (b), and (d), it is clear that the heat comes from the channel region of the device and transfers to its proximity in all directions, and the SHE is better visualized.

Therefore, by growing an HfO_2 interfacial layer on a sapphire substrate for thermal adhesion or thermal interface engineering, the SHE of TG In_2O_3 devices is reduced. Fig. 10(a) exhibits the output characteristics of a TG In_2O_3 transistor with T_{ch} of 2.1 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm on an HfO_2/sapphire substrate where very high I_D of 2.4 mA/μm is demonstrated at V_{DS} of 1.2 V. The I_D–V_{DS} curves are well-performed with some saturation behaviors at low V_{GS}, and the SHE is not severe under these bias conditions. Fig. 10(b) reveals the corresponding transfer characteristics where an ON–OFF ratio larger than 3 orders of magnitude is behaved even though the device is in depletion-mode. The solid curves are in logarithmic scale, and the empty symbols represent the identical curve in linear scale. Some key parameters are extracted as follows: threshold voltage (V_T) being −3.7 V, transconductance (g_m) being 495 μS/μm at V_{DS} = 1 V, and field-effect mobility (μ_{FE}) being 20.9 cm^2·V^{-1}·s^{-1}. Note that the degradations of the transfer characteristics and the negative shift of V_T in Fig. 10(b) compared with Fig. 3(a) are not due to the change of substrate but the thicker T_{ch} and shorter L_{ch}, as the device performance parameters such as V_T, μ_{FE}, ON–OFF ratio, and SS value of ALD In_2O_3 transistors sensitively depend on their T_{ch} and L_{ch} [1], [2], [3], [4], [6], [18].

Although substrate materials with even higher thermal conductivity such as silicon carbide (SiC, 387 W·m^{-1}·K^{-1}) [51] and diamond (2200 W·m^{-1}·K^{-1}) [52] normally have less

affordability and relatively limited commercial availability, they are generally advantageous against others for power device applications. Nevertheless, thermal interfacial issues at the channel/substrate interface may also restrict the benefit they can conduct to some degree. This work provides a route to potentially resolve this challenge and maximize the profits that those higher thermal conductivity substrates can bring to relieve SHE.

IV. Conclusion

In summary, heat dissipation of TG ultrathin In_2O_3 transistors on a sapphire substrate with 2L h-BN, 4-nm HfO_2, or no interlayer is explored to assist alleviating SHE. A high spatial resolution TR measurement system is introduced to visualize the ΔT distribution as the devices are at ON-state with SHE. With the thermal adhesion layer of h-BN or HfO_2 to improve the interfacial heat transfer between the In_2O_3 channel and the sapphire substrate, the observed maximum ΔT of the devices is reduced by 9% or 27%, respectively. A steady-state thermal diffusion model with a finite-element method is integrated with the TR imaging results to extract the effective TBC values in each case to quantify the improvement of the interfacial heat transfer. The effective TBC is enhanced by a factor of 2 or 7 with the insertion of the h-BN or HfO_2 interlayer. The huge amelioration of the effective TBC is likely due to the better match of the PDOS distribution in the acoustic region where the IOU ratio of In_2O_3 with h-BN or HfO_2 is 3 or 11 times larger than that with sapphire. Because of the cured SHE, high I_D of 2.4 mA/μm at V_{DS} of 1.2 V is realized in a TG In_2O_3 transistor with ultrathin T_{ch} of 2.1 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm on an HfO_2/sapphire substrate. This thermal engineering method can be potentially applied to other BEOL devices with other thermal engineered adhesion and isolation layers above the standard front-end-of-line Si CMOS circuits.

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