Abstract—In this work, we report the experimental demonstration of In$_2$O$_3$ 3-D transistors coated on fin structures and integrated circuits by a back-end-of-line (BEOL) compatible atomic layer deposition (ALD) process. High-performance planar back-gate In$_2$O$_3$ transistors with high mobility of 113 cm$^2$/V·s and high maximum drain current ($I_D$) of 2.5 mA/μm are achieved by channel thickness engineering and postdeposition annealing. The high-performance ALD In$_2$O$_3$-based zero-$V_{GS}$-load inverter is demonstrated with a maximum voltage gain of 38 V/V and a minimum supply voltage ($V_{DD}$) down to 0.5 V. Top-gate indium oxide (In$_2$O$_3$) transistors by low-temperature ALD of both gate insulator and channel semiconductor are also demonstrated with $I_D$ of 570 μA/μm and low subthreshold slope (SS) down to 84.6 mV/decade. ALD In$_2$O$_3$ 3-D Fin transistors with the top-gate structure are then demonstrated, benefiting from the conformal deposition capability of ALD. These results suggest that ALD oxide semiconductors and devices have unique advantages and are promising toward BEOL-compatible monolithic 3-D integration for 3-D integrated circuits.

Index Terms—3-D structure, atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, indium oxide, oxide semiconductor, thin-film transistor.

I. INTRODUCTION

Oxide semiconductors are the leading semiconductor channel materials for flat-panel display applications [1], [2]. Recently, indium oxide (In$_2$O$_3$) or doped-In$_2$O$_3$, such as (indium gallium zinc oxide, IGZO), are being investigated as promising channel materials for back-end-of-line (BEOL) compatible transistors for monolithic 3-D integration [3], by both sputtering [4]–[13] and atomic layer deposition (ALD) [14]–[18], due to their high mobility, wide bandgap, low variability, and high stability. ALD-based oxide semiconductors [19]–[23] are of special interest due to the atomically smooth surface, ultrathin thickness, and the capability of conformal deposition on 3-D structures. Recently, high-performance back-gate ALD In$_2$O$_3$ transistors have been demonstrated with a high drain current over 2 mA/μm in both depletion-mode (D-mode) and enhancement-mode (E-mode) operations [15], [16]. The devices have ultrascaled channel thickness ($T_{ch}$) down to 0.7 nm, channel length down ($L_{ch}$) to 40 nm, low thermal budget below 400 °C, and stability in the H$_2$ environment, which are highly compatible with the BEOL process. Meanwhile, for many practical applications, a top-gate device structure is required for integrated circuits and other applications. However, how to form high-quality gate dielectric on top of ALD In$_2$O$_3$ and how to realize high-performance top-gate ALD In$_2$O$_3$ transistors remain unclear.

In this work, the performance of back-gate ALD In$_2$O$_3$ transistors is further enhanced by $T_{ch}$ engineering and post-deposition annealing. An optimized $T_{ch}$ is determined to be 2.2–2.5 nm, achieving record high mobility of 113 cm$^2$/V·s and record-high maximum drain current of 2.5 mA/μm at $L_{ch}$ of 40 nm and $V_{DD} = 0.7$ V. The high-performance back-gate ALD In$_2$O$_3$ transistors-based zero-$V_{GS}$-load inverter is demonstrated with a maximum voltage gain of 38 V/V and a minimum supply voltage ($V_{DD}$) down to 0.5 V. Top-gate In$_2$O$_3$ transistors are also demonstrated by low-temperature ALD of both gate insulator and channel semiconductor. High-performance top-gate In$_2$O$_3$ transistors are realized with a maximum drain current ($I_D$) of 570 μA/μm and a low subthreshold slope (SS) down to 84.6 mV/decade. It is found that the deposition of hafnium oxide (HfO$_2$) as gate insulator at low temperature and postdeposition annealing in O$_2$ at low temperature are critical to annihilate defects that are generated during the formation of top dielectrics and top-gate electrodes. ALD In$_2$O$_3$ 3-D Fin transistors with top-gate structures coated on SiO$_2$ fin structures are also demonstrated for the first time, taking advantage of conformal deposition of ALD on 3-D structures.
II. EXPERIMENTS

Fig. 1 presents the schematic of planar (a) back-gate and (b) top-gate In2O3 transistors. The back-gate device structure is similar to previously reported in [15] and [16], which is used for circuit demonstration. The gate-stack consists of 40-nm Ni as gate metal, 5-nm HfO2 as gate dielectric, 0.5–3.5-nm In2O3 as semiconducting channels, and 80-nm Ni as source/drain electrodes. The device fabrication process is similar to [15] and [16]. The fabricated devices were annealed in O2, N2, or forming gas (FG, 96% N2/4% H2) for 30 s at different temperatures from 250 °C to 350 °C according to the optimized annealing conditions achieved in [15]. Fig. 1(c) shows the photograph of a fabricated In2O3 zero-\(V_{GS}\)-load inverter in a five-stage ring oscillator. The circuit diagram of the In2O3 zero-\(V_{GS}\)-load inverter is shown in Fig. 1(d). D-mode and E-mode transistors could be achieved by threshold voltage \(V_T\) engineering, such as plasma treatment described in [17]. The E-mode device has a channel length \(L_{ch}\) of 2 \(\mu\)m, while \(L_{ch}\) of D-mode devices \(L_{D}\) varies from 0.1 to 0.3 \(\mu\)m to engineer the load resistance.

The gate-stack of planar top-gate In2O3 transistors, as shown in Fig. 1(b), includes 40-nm Ni as gate metal, 7-nm HfO2 as gate dielectric, 1.5-nm In2O3 as the semiconducting channel, and 40-nm Ni as source/drain electrodes. The device fabrication starts with a standard cleaning of 90-nm SiO2/p+ Si substrates. The 1.5-nm-thick In2O3 films were then deposited by ALD at 225 °C, using (CH3)3In (TMIn) and \(\text{H}_2\text{O}\) as In and O precursors. Channel isolation was done by wet etching using concentrated HCl. The 40-nm Ni was then deposited by e-beam evaporation as S/D contacts. Then, HfO2 was deposited by ALD at various temperatures of 120 °C/150 °C/200 °C, using \([\text{CH}_3\text{C}_2\text{N}_2]_\text{H}_2\)HF (TDMAHf) and \(\text{H}_2\text{O}\) as Hf and O precursors. The impact of ALD deposition temperature is discussed in great detail in the following section. The fabricated devices were annealed by rapid thermal annealing (RTA) in \(\text{O}_2\) at different temperatures. 3-D Fin transistors with top-gate structures were fabricated on a SiO2/Si substrate with SiO2 fin structures. The top-gate dielectric of 7-nm HfO2 was formed by low-temperature ALD at 120 °C, which is critical to form top-gate devices.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the \(I_D-V_{GS}\) characteristics of a planar In2O3 transistor with \(L_{ch}\) of 1 \(\mu\)m and \(T_{ch}\) of 2.2 nm with \(O_2\) annealing at 350 °C for 30 s. Fig. 2(b) shows the corresponding \(I_D-V_{DS}\) characteristics of the same device, exhibiting high maximum \(I_D\) of 850 \(\mu\)A/\(\mu\)m even with \(L_{ch}\) of 1 \(\mu\)m and well-behaved drain current saturation at high \(V_{DS}\). Such high \(I_D\) is the result of high field-effect mobility \((\mu_{FE})\) of 113 cm2/V·s, as shown in Fig. 2(c), extracted from the maximum transconductance \((g_m)\) at \(V_{DS}\) of 0.05 V. Effective mobility \((\mu_{eff})\) versus \(V_{DS}\) extracted from drain conductance \((g_D)\) are presented in Fig. 2(d), which is consistent with \(\mu_{FE}\). Fig. 3(a) and (b) presents the \(I_D-V_{GS}\) and \(I_D-V_{DS}\) characteristics of an In2O3 transistor with \(L_{ch}\) of 40 nm and \(T_{ch}\) of 2.2 nm, exhibiting a high maximum \(I_D\) of 2.5 mA/\(\mu\)m under \(V_{DS}=0.7\) V and \(V_{GS}-V_T=4\) V with optimized \(T_{ch}\) and annealing conditions. Further dielectric scaling is needed to realize \(V_{GS}-V_T\) approaching \(V_{DS}\).

The mobility of In2O3 in this work is significantly improved compared to other ALD-based oxide
semiconductors [19]–[23]. Such high mobility is achieved by \( T_{ch} \) engineering and postdeposition annealing, as shown in Fig. 4(a). Average \( \mu_{FE} > 100 \text{ cm}^2/\text{V} \cdot \text{s} \) is achieved with \( T_{ch} \) of 2.2–2.5 nm at optimized annealing conditions. \( \mu_{FE} \) decreases rapidly with \( T_{ch} \) below 1 nm, most likely due to the enhanced surface scattering and quantum confinement effect on the band structure [14]. \( \mu_{FE} \) decreases at \( T_{ch} \) above 3 nm due to the higher carrier concentration and weaker gate electrostatic control, as also shown in \( V_T \) versus \( T_{ch} \) in Fig. 4(b).

Postdeposition annealing for the reduction of oxygen vacancies in as-deposited films is needed to tune \( V_T \) of devices with \( T_{ch} \) above 2 nm to obtain a sufficiently high on/off ratio. \( V_T \) of devices with certain \( T_{ch} \) can be controlled by annealing conditions, as shown in Fig. 4(b). Fig. 4(c) shows \( T_{ch} \)-dependent SS extracted from as-deposited devices and devices with optimized annealing conditions, exhibiting SS close to the thermal limit of 60 mV/decade at room temperature at \( T_{ch} \sim 1 \text{ nm} \). The thickness-dependent SS indicates that the interface trap density \( D_{it} \) in the subthreshold region may be related to \( T_{ch} \). However, the atomic configuration at the oxide-semiconductor interface does not have a \( T_{ch} \) dependence. Thus, the defect energy levels should not change with respect to the vacuum level. Therefore, the only possible reason is that the band structure of In\(_2\)O\(_3\) is changing with \( T_{ch} \) (such as \( T_{ch} \)-dependent conduction band minimum, \( E_C \)) so that the Fermi level (\( E_F \)) alignment at the subthreshold region is changing. This result is consistent with previous theoretical analysis and density function theory (DFT) simulations [14].

Fig. 5(a) presents \( V_{out} \) versus \( V_{in} \) curve of an In\(_2\)O\(_3\) zero-\( V_{GS} \)-load inverter with \( L_{ch} \) of 0.3 \( \mu \text{m} \) at different \( V_{DD} \)'s from 2 down to 0.5 V, showing well-behaved voltage transfer characteristics. The voltage gains are given in Fig. 5(b), achieving a maximum voltage gain of 38 V/V at \( V_{DD} \) of 2 V. The midpoint voltage of the In\(_2\)O\(_3\) zero-\( V_{GS} \)-load inverter can be engineered by tuning the load resistance and varying the channel length of the D-mode transistor, as illustrated in Fig. 5(c), providing the essential approach for \( V_{DD} \) and midpoint voltage engineering accordingly. Therefore, a sufficiently large noise margin (NM) can be achieved at a low \( V_{DD} \) of 0.7 V, as shown in Fig. 5(d).
for 3 min. This device has a maximum $I_D$ of 397 $\mu$A/\mu m and SS of 84.6 mV/decade. The small SS at the subthreshold region indicates a high-quality oxide/semiconductor interface. The interface trap density $D_t$ at the sub-threshold region is estimated to be $\sim 5.6 \times 10^{12}$/cm$^2$ ev. $D_t$ at the HfO$_2$/In$_2$O$_3$ interface in a top-gate device is much larger than that in a back-gate device. The main difficulty for the integration of top-gate on the ALD In$_2$O$_3$ channel is from the ALD HfO$_2$ process. Hf-O bond with dissociation energy of 801 kJ/mol is much more stable compared to the In-O bond of 346 kJ/mol. ALD of HfO$_2$ on In$_2$O$_3$ generates more O vacancies in In$_2$O$_3$ and induces much more charge density. Meanwhile, it also degrades In$_2$O$_3$ film and HfO$_2$/In$_2$O$_3$ interface quality. Appropriate O$_2$ annealing can fill these O vacancies and heal most of the defects from the process so that SS of top-gate devices can be improved. To further improve the oxide/semiconductor interface quality, a high trap oxide or interfacial layer with low dissociation energy is preferred, and a lower interface trap density may be achieved. For example, Al-O has dissociation energy of 512 kJ/mol, and Mg-O has dissociation energy of 394 kJ/mol.

Fig. 7(a) shows the transfer characteristics at $V_{DS}$ of 1 V of top-gate In$_2$O$_3$ transistors with different annealing conditions. $I_{DS}$ at $V_{DS}$ of 1 V of top-gate In$_2$O$_3$ transistors with different annealing conditions with HfO$_2$ gate oxide deposited by ALD at 120 $^\circ$C, 150 $^\circ$C, and 200 $^\circ$C.

Therefore, from the above experimental observation, it is speculated that the deposition of HfO$_2$ by ALD generates defects at the HfO$_2$/In$_2$O$_3$ interface, most likely because the pulse of Hf precursor (TDMAHf) takes oxygen atoms away from In$_2$O$_3$, leading to the formation of oxygen vacancies at HfO$_2$/In$_2$O$_3$ interface. Such defects can only be healed in an O$_2$ environment by O$_2$ annealing. Such a process also depends on the annealing time, as shown in Fig. 7(a). It is also found that devices with O$_2$ annealing at 250 $^\circ$C have higher $I_D$ than devices with O$_2$ annealing at 300 $^\circ$C with a similar threshold voltage ($V_t$). Therefore, low-temperature O$_2$ annealing is preferred to maintain high mobility.

Fig. 7 presents the $I_D$–$V_{GS}$ characteristics at $V_{DS}$ of 1 V of top-gate In$_2$O$_3$ transistors with O$_2$ annealing and with HfO$_2$ gate oxide deposited by ALD at (a) 120 $^\circ$C, (b) 150 $^\circ$C, and (c) 200 $^\circ$C. As we can see, the on/off ratio of the devices degrades significantly with higher temperature HfO$_2$ ALD process and indicates that much more defects are generated at higher ALD temperature most likely due to the stronger reaction between TDMAHf and In$_2$O$_3$. All these detailed experiments offer a consistent picture of the challenge of integration of ALD HfO$_2$ on top of In$_2$O$_3$.

Fig. 8(a) shows the scanning electron microscopic (SEM) image of an In$_2$O$_3$ 3-D Fin transistor with top-gate structure, capturing the gate metal, source/drain contacts, and the fin structures. Fig. 8(b)–(d) presents the transmission electron microscope (TEM) image and energy-dispersive X-ray spectroscopic (EDX) mapping under high-angle annular dark-field imaging (HAADF) scanning transmission electron microscope (STEM) of an In$_2$O$_3$ 3-D fin transistor. ALD In$_2$O$_3$ channel with $T_{ch}$ of 1.5 nm is conformally coated on top of SiO$_2$ fin structures with a fin height of 180 nm and a fin pitch of 130 nm, as shown in the EDX element mapping of Hf and In. Fig. 8(e) shows $I_D$–$V_{GS}$ characteristics of an In$_2$O$_3$ 3-D Fin transistor with $L_{ch}$ of 2 $\mu$m and $T_{ch}$ of 1.5 nm, exhibiting well-behaved transfer characteristics. Fig. 8(f) shows the
corresponding $I_D-V_{DS}$ characteristics with a maximum $I_D$ of 180 $\mu$A/$\mu$m, normalized by device width, which is about two times larger than that from its top-gate planar counterpart. The 3-D fin structure provides an effective approach to increase the drive current without increasing the device area. The ultrathin channel thickness and the top-gate non-self-align structure with a large link resistance make $I_D$ smaller than those from back-gate planar devices.

IV. CONCLUSION

In summary, high-performance 3-D Fin transistors and integrated circuits based on BEOL compatible oxide semiconductors by ALD are demonstrated. High mobility of 113 cm$^2$/V·s and high maximum drain current of 2.5 mA/$\mu$m are achieved. The demonstration of 3-D devices and integrated circuits suggests that ALD oxide semiconductors and devices have their unique advantages over sputtering films and are promising toward BEOL-compatible monolithic 3-D integration for 3-D integrated circuits.

REFERENCES


