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Back-End-of-Line-Compatible Scaled InGaZnO Transistors by Atomic Layer Deposition

Jie Zhang, *Member, IEEE*, Zehao Lin, Zhuocheng Zhang, Ke Xu, Hongyi Dou, Bo Yang, Adam Charnas, Dongqi Zheng, Xinghang Zhang, Haiyan Wang, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— In this work, we report on back-end-of-line (BEOL)-compatible InGaZnO indium gallium zinc oxide (IGZO) thin film transistors (TFTs) with extreme scaled device dimension including channel thickness (T_{ch}) down to 1.5 nm and channel length (L_{ch}) down to 60 nm. These IGZO channels with a high In atomic ratio of 92% were derived by atomic-layer-deposition (ALD), where the IGZO thickness could be precisely controlled by ALD cycles. These TFTs were subjected to a mild O_2 annealing at 250 °C, the effect of which is also systematically investigated. It is found that both T_{ch} and O_2 annealing have significant effects on TFT performance. By using optimized O_2 annealing conditions, the ALD IGZO TFTs with scaled T_{ch} of 1.5 nm and L_{ch} of 60 nm exhibit desirable electrical performance including a high ON/OFF ratio (I_{ON}/I_{OFF}) $\sim 10^{11}$, a decent high Ion of 354 μA/μm under V_{DS} of 1.2 V, a steep subthreshold swing (SS) of 68 mV/dec, a small drain-induced-barrier-lowering (DIBL) of 30 mV/V, and a normal-off operation, which is comparable to the state-of-art sputtered IGZO TFTs. Furthermore, the optimized TFTs also exhibit significantly resolved threshold voltage (V_T) roll-off and a remarkably high degree of stability to the positive gate bias stress (PBS). A trap model with its possible microscopic origin is proposed, which explains well the dependence of electrical performance on both T_{ch} and O_2 annealing, thus providing a new insight into the reliability of IGZO TFTs.**

***Index Terms*— Atomic layer deposition (ALD), back-end-of-line (BEOL), indium gallium zinc oxide (IGZO), O_2 annealing, reliability, thin film transistor (TFT), trap model.**

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I. Introduction

INDIUM-GALLIUM-ZINC-OXIDE (IGZO) thin film transistors (TFTs) have made a commercial success in back-plane display applications as the replacement for a-Si and poly-Si TFTs due to their excellent properties such as decent mobility, low off-current (I_{OFF}), high transparency, and good uniformity [1], [2]. Recent work on scaled IGZO TFTs has extended their application domain from the traditional back-plane display to back-end-of-line (BEOL)-compatible logic and memory applications toward monolithic 3-D integration [3], [4], [5], [6], [7], [8], [9]. These scaled IGZO TFTs were derived by sputtering method and fabricated under a low thermal budget (<400 °C), exhibiting excellent electrical performance with high on-current (I_{ON}) and thus revitalizing the prospects of IGZO as a TFT channel material. Compared to sputtering, atomic layer deposition (ALD) growth method provides more precise thickness control, excellent conformity, composition flexibility, and large-area uniformity, benefiting to the realization of the ultrascaled TFTs [10], [11], [12]. However, to the best of our knowledge, scaled ALD IGZO TFTs are still missing, with only reports demonstrating long-channel TFTs with $L_{ch} > 10$ μm [13], [14]. On the other hand, although sputtered IGZO TFTs with sub-100 nm L_{ch} have been reported, these scaled TFTs could suffer from some unsatisfied properties such as large drain-induced barrier-lowering (DIBL), normal-on operation, significant threshold voltage (V_T) roll-off at scaled length, and severe positive bias stability issues [3], [4], [5], [6], [7], [8], [9], which needs to be addressed properly for practical applications. Additionally, the underlying reasons for these undesirable performances have not been disclosed yet, which requires more in-depth studies.

In this work, we report for the first time ALD IGZO TFTs with extreme scaled T_{ch} down to 1.5 nm and L_{ch} down to 60 nm using optimized O_2 annealing, exhibiting outstanding electrical performance including a high ON/OFF ratio (I_{ON}/I_{OFF}) $\sim 10^{11}$, a steep subthreshold swing (SS) of 68 mV/dec, a high I_{ON} of 354 μA/μm at V_{DS} of 1.2 V, a small DIBL of 30 mV/V, a normal-off operation, a negligible V_T roll-off, and a remarkably high degree of stability to positive gate bias stress (PBS). The excellent electrical performances could be attributed to the combinatorial effects of ultrathin channel and optimized O_2 annealing. It is found that T_{ch} has a significant effect on TFT performance, where V_T is shifted positively and field-effect-mobility (μ_{FE}) is reduced with the decreased T_{ch}, explained well by the trap neutral level (TNL) model.

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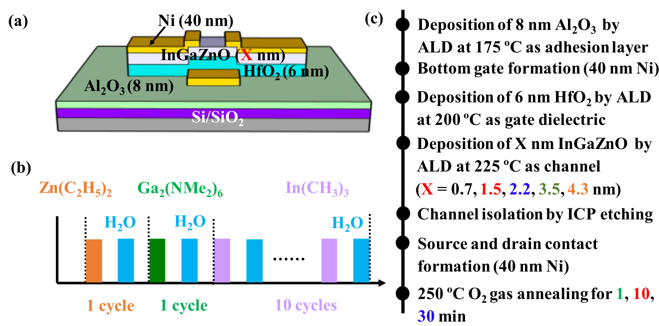

Fig. 1. (a) Device schematic. (b) Illustration of IGZO ALD growth. (c) Fabrication flow of scaled IGZO TFTs, where the maximum temperature during fabrication is 250 °C, qualifying the BEOL applications.

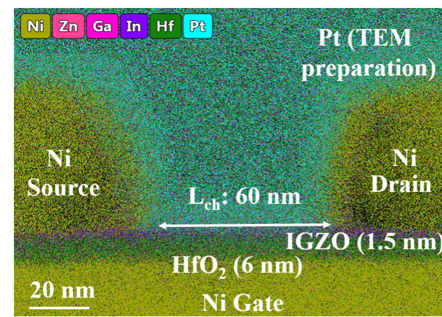

Fig. 2. Cross-sectional STEM with EDX elemental mapping of ultra-scaled IGZO TFTs after 10 min O_2 annealing, capturing T_{ch} of 1.5 nm and L_{ch} of 60 nm.

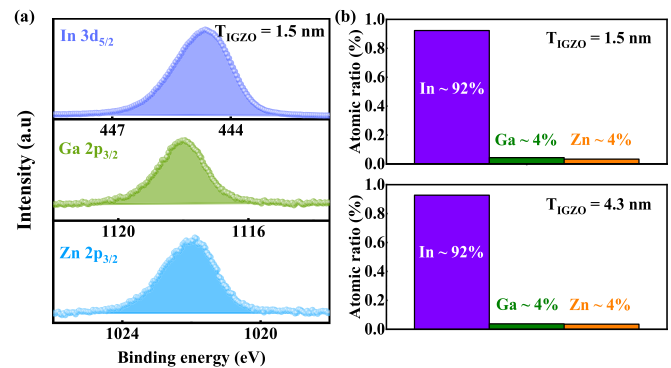

Fig. 3. (a) XPS of In $3d_{5/2}$, Ga $2p_{3/2}$, and Zn $2p_{3/2}$ spectrum of 1.5 nm IGZO films. (b) Elemental analysis from XPS spectrum based on IGZO films with T_{ch} of 1.5 and 4.3 nm, showing consistent film composition with high In atomic ratio of 92%.

The DIBL is also found to be improved with the reduced T_{ch}, which is attributed to the alleviated self-heating effect (SHE) with thinner channels, suppressing the formation of donor-like traps. On the other hand, optimizing O_2 annealing could significantly alleviate V_T roll-off at scaled L_{ch} and achieve a high degree of stability to PBS, which could be attributed to reduced donor traps without introducing many acceptor traps. Based on these observations, it is believed that the donor-like traps such as oxygen vacancy and hydrogen states are the underlying reason for large DIBL, significant V_T roll-off, and anomaly-negative V_T shift during PBS. A TNL trap model with its possible microscopic origin is proposed, explaining well the dependence of electrical performance on both T_{ch} and O_2 annealing, offering guidance for future device optimization.

II. Experiment

Fig. 1(a) illustrates the schematic of an ultrathin IGZO TFT with the T_{ch} ranging from 0.7 to 4.3 nm, where 40 nm Ni, 6 nm HfO_2 function as electrode and dielectric, respectively. The IGZO channel was deposited by ALD at 225 °C, with one cycle of ZnO and Ga_2O_3 followed by ten cycles of In_2O_3 forming one super-cycle of the IGZO growth, as shown in Fig. 1(b). The IGZO channel thickness was controlled by the number of super-cycles with a growth rate of ∼1.25 Å/super-cycle, which was examined by an ellipsometer and high-resolution transmission electron microscope (HRTEM). The detailed TFT fabrication process is depicted in Fig. 1(c). Briefly, the fabrication process started with the deposition of 8 nm Al_2O_3 by ALD at 175 °C on the Si/SiO_2 substrates to obtain a smooth surface. Then, 40 nm Ni was deposited by *e*-beam evaporation as bottom gate, defined by photolithography. Next, 6 nm HfO_2 was deposited by ALD at 200 °C, followed by the deposition of IGZO by ALD at 225 °C. The thickness of IGZO channel were varied from 0.7 to 4.3 nm to investigate the effects of channel thickness on TFT performance. After channel deposition, the IGZO mesa isolations were formed by Cl-based inductively coupled plasma (ICP) etching. Finally, 40 nm Ni was deposited as source/drain contacts by *e*-beam evaporation, defined by electron beam lithography. The fabricated TFTs have a L_{ch} ranging from 1 μm to 60 nm. After fabrication, TFTs were subjected to a mild O_2 annealing at 250 °C with respective duration of 1, 10, and 30 min to investigate the effects of oxygen annealing on TFT performance.

Fig. 2 shows the cross-sectional scanning transmission electron microscopy (STEM) image of the ultrascaled IGZO TFTs with a T_{ch} of 1.5 nm and a L_{ch} of 60 nm after 10 min O_2 annealing. The energy dispersive X-ray (EDX) spectroscopy elemental mapping suggests the appearance of In, Ga and Zn elements in the channel with the dominance of the In element. This is further confirmed by the X-ray photoelectron spectroscopy (XPS) in Fig. 3, where the chemical composition of ALD IGZO films with thickness of 1.5 and 4.3 nm were analyzed. Both films exhibit a consistently high In ratio of ∼92%/4%/4% for In/Ga/Zn, respectively. The high In ratio could be attributed to the high In_2O_3 cycle ratio during IGZO super-cycle ALD growth, which is beneficial for achieving high I_{ON} for IGZO TFTs with scaled T_{ch}.

III. Results and Discussion

A. Effects of Channel Thickness on TFT Performance

Fig. 4(a) illustrates bi-directional transfer characteristics of IGZO TFTs with a L_{ch} of 60 nm and various T_{ch} of 0.7 to 4.3 nm under V_{DS} of 0.5 V using optimized 10 min O_2 annealing. It is found that the T_{ch} has a significant effect on the electron transport in the IGZO channel. The IGZO TFTs with T_{ch} of 0.7 nm show no observable current while that of 1.5 to 4.3 nm exhibit a well-behaved performance. This is in contrast to that pure In_2O_3 TFTs with T_{ch} of 0.7 nm could still be operational [11], suggesting that Zn and Ga could function as carrier suppressors and transport hinders in the In_2O_3 host. The V_T, which is defined at V_{GS} where I_D reaches 1 nA/μm, is also

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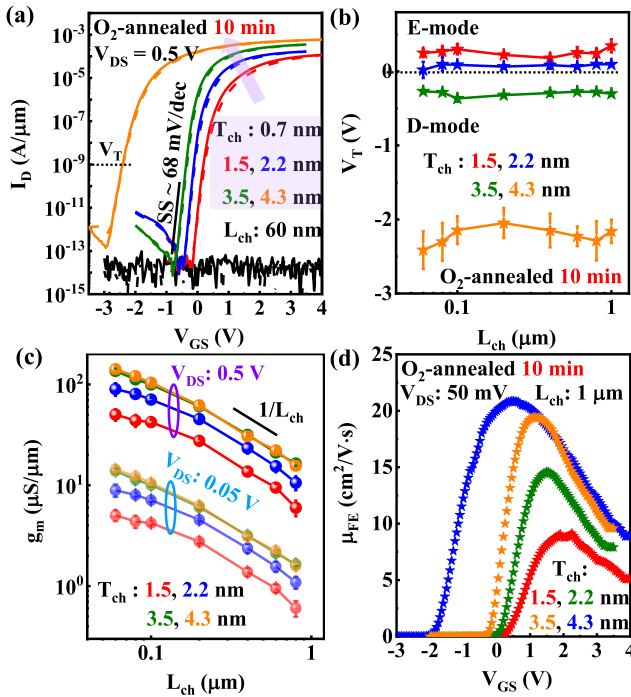

Fig. 4. (a) Transfer characteristics of IGZO TFTs with L_{ch} of 60 nm and varying T_{ch} of 0.7 to 4.3 nm under V_{DS} of 0.5 V, which have undergone optimized 10 min O_2 annealing at 250 °C. (b) Statistical results of extracted V_T as a function of L_{ch}. (c) Extracted transconductance (g_m) as a function of L_{ch} under V_{DS} of 0.05 and 0.5 V for IGZO TFTs with varying T_{ch}. (d) Extracted μ_{FE} from g_m of long-channel IGZO TFTs with L_{ch} of 1 μm and varying T_{ch} of 1.5 to 4.3 nm.

found to be negatively shifted with the increased T_{ch}. Fig. 4(b) exhibits the extracted V_T as a function of L_{ch} for IGZO TFTs of different T_{ch}. The IGZO TFTs with T_{ch} of 1.5 and 2.2 nm show enhancement-mode (E-mode) operation with positive V_T whereas that of 3.5 and 4.3 nm exhibit depletion-mode (D-mode) with negative V_T. It is also noted that TFTs with different L_{ch} show consistent V_T, which could be attributed to the optimized O_2 annealing and will be discussed in later session. All TFTs show a negligible hysteresis in Fig. 4(a), suggesting a high-quality channel/dielectric interface. This is also evidenced by the low SS values of the IGZO TFTs, where a nearly ideal SS of ~68 mV/dec can be achieved for TFTs with T_{ch} of 1.5 nm.

Fig. 4(c) exhibits the extracted transconductance (g_m) as a function of L_{ch} under V_{DS} of 0.05 and 0.5 V for IGZO TFTs with varying T_{ch}, where $1/L_{ch}$ trend is followed well for TFTs with large L_{ch}. Some deviation from $1/L_{ch}$ trend can be observed for sub-100 nm L_{ch}, suggesting that contact resistance (R_C) starts to play a role and could be related to the increased R_C due to O_2 annealing. The field-effect-mobility (μ_{FE}) can be extracted from g_m of long-channel IGZO TFTs without considering R_C. Fig. 4(d) shows the extracted μ_{FE} for IGZO TFTs of different T_{ch}, where μ_{FE} is reduced from 20.2 $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 19.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, 14.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and 8.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ as the T_{ch} is reduced from 4.3 nm to 3.5 nm, 2.2 nm, and 1.5 nm, respectively. Fig. 5(a) and (b) summarize the extracted V_T and μ_{FE} as a function of T_{ch}, where V_T is shifted positively and μ_{FE} is reduced with the decreased T_{ch}. This T_{ch} dependence could be explained

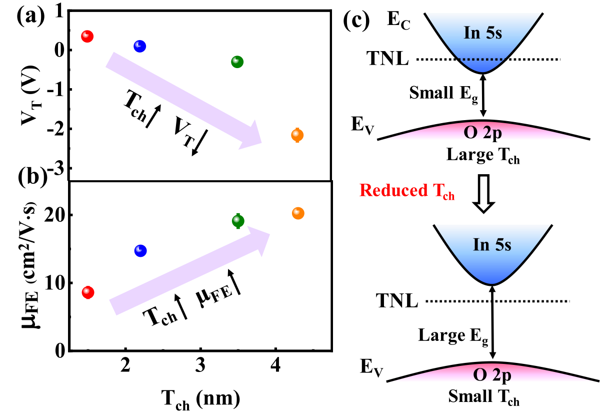

Fig. 5. (a) Extracted V_T. (b) μ_{FE} as a function of T_{ch}, where V_T is negatively shifted and μ_{FE} is increased with the increased T_{ch}. (c) Proposed TNL model, explaining the T_{ch} dependence.

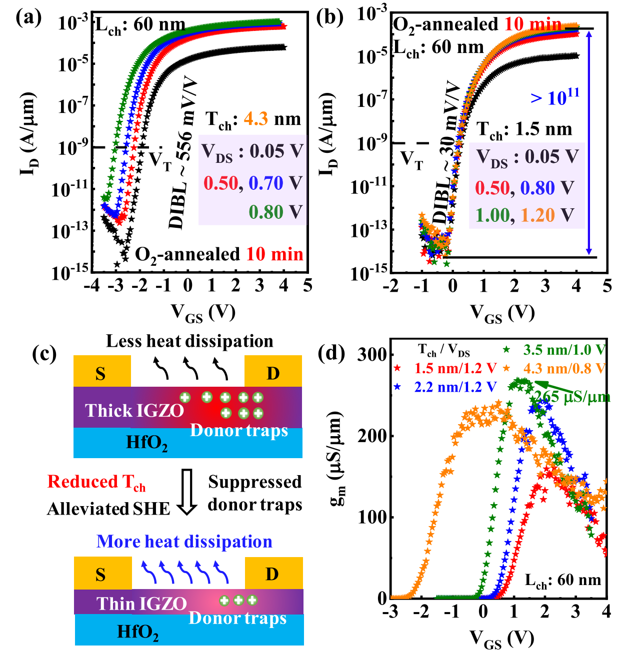

Fig. 6. Transfer curves of IGZO TFTs under varying V_{DS} with L_{ch} of 60 nm and T_{ch} of (a) 4.3 nm and (b) 1.5 nm, where the DIBL is significantly reduced from 556 to 30 mV/V as T_{ch} is reduced from 4.3 to 1.5 nm. (c) Illustration of alleviated SHE due to reduced T_{ch}, suppressing the formation of donor traps and leading to improved DIBL. (d) Maximum g_m for TFTs with L_{ch} of 60 nm and varying T_{ch} and V_{DS}.

by the TNL model [11], [12], [13], [14], [15], where TNL moves from the conduction band into the bandgap (E_g) of IGZO with the decreased T_{ch}. This is also companied by the enlarged E_g with the reduced T_{ch} due to quantum confinement, all leading to the reduced electron concentration and positively shifted V_T. The reduced μ_{FE} with positively shifted V_T can be explained by the percolation conduction theory [16], [17], where electron transport is hindered by more in-gap states due to the movement of TNL into E_g arising from the reduced T_{ch}.

Fig. 6(a) and (b) exhibit transfer curves of TFTs under varying V_{DS} with L_{ch} of 60 nm and T_{ch} of 4.3 and 1.5 nm, respectively. It can be observed that TFTs with T_{ch} of 4.3 nm show a significant negative V_T shift (ΔV_T) under higher V_{DS} with large DIBL of ~556 mV/V. The I_{OFF} is also increased under higher V_{DS} and further increase in V_{DS} beyond 0.8 V

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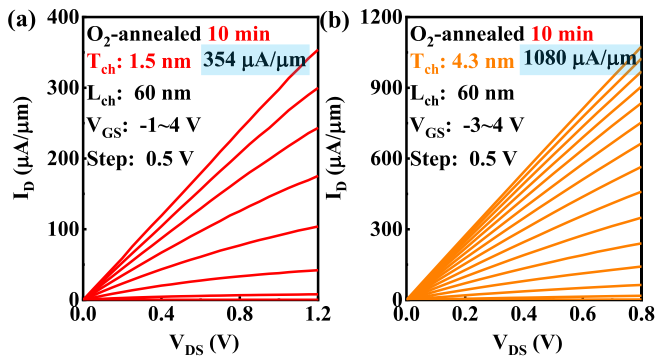

Fig. 7. Output characteristics of IGZO TFTs with L_{ch} of 60 nm and T_{ch} of (a) 1.5 nm and (b) 4.3 nm, featuring a high I_{ON} of 354 and 1080 μA/μm, respectively.

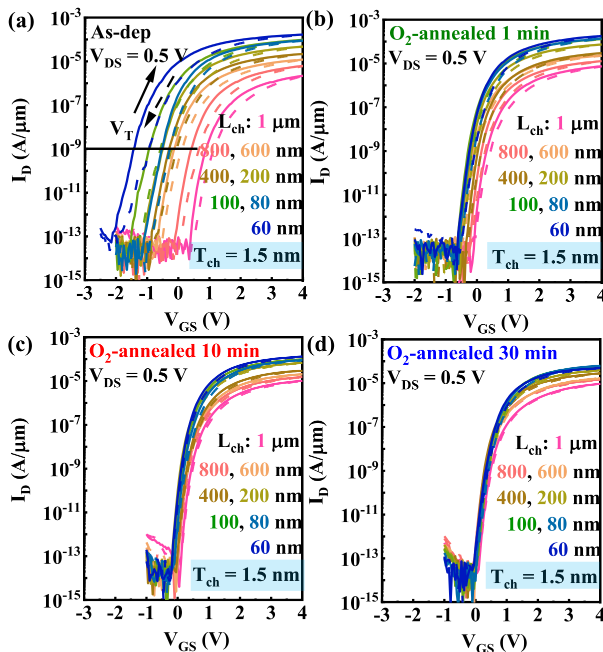

Fig. 8. Transfer characteristics of IGZO TFTs with T_{ch} of 1.5 nm and L_{ch} ranging from 1 μm to 60 nm under V_{DS} of 0.5 V (a) as-deposited, (b) 1 min, (c) 10 min, and (d) 30 min O_2-annealed IGZO TFTs, suggesting a solution to the V_T roll-off issue with a reduced I_{ON}.

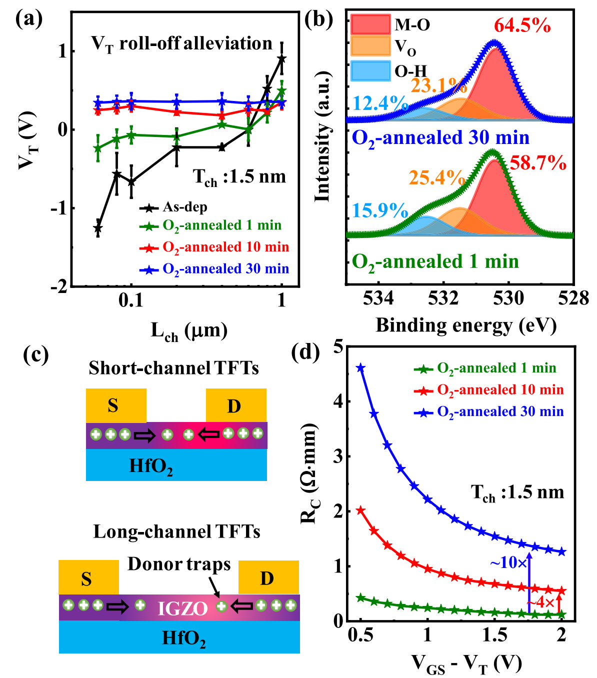

Fig. 9. (a) Extracted V_T as a function of L_{ch} for 1, 10, and 30 min O_2-annealed IGZO TFTs with T_{ch} of 1.5 nm. (b) O 1 s spectrum of 1 and 30 min O_2-annealed IGZO, showing a reduced V_O and OH contamination. (c) Illustration of possible origin of V_T roll-off, where donor traps migrate under high electric field. (d) Contact resistance (R_C) as a function of gate overdrive voltage ($V_{GS} - V_{th}$) for 1, 10, and 30 min O_2-annealed IGZO TFTs with T_{ch} of 1.5 nm, where the reduced I_{ON} could be attributed to the increased R_C.

result in the loss of switching behavior. This is in contrast to that TFTs with T_{ch} of 1.5 nm exhibit a high I_{ON}/I_{OFF} of $> 10^{11}$ and a small DIBL of ~30 mV/V with V_{DS} up to 1.2 V. The reduced DIBL could be attributed to less generated heat due to less I_{ON} and more heat dissipation due to the increased surface area to volume ratio with thinner channel [Fig. 6(c)], thus suppressing the formation of donor-like traps such as ionized oxygen vacancy and hydrogen states and resulting in the alleviated SHE [18], [19]. The maximum g_m for TFTs with L_{ch} of 60 nm and varying T_{ch} can be found in Fig. 6(d). Our ALD IGZO TFTs show a high g_m value of ~151 to 265 μS/μm, which are among the best values for the IGZO TFTs [3], [4], [5], [6], [7], [8], [9]. Fig. 7(a) shows the output characteristics of IGZO TFTs with L_{ch} of 60 nm and T_{ch} of 1.5 nm, where a relatively high I_{ON} of 354 μA/μm can be observed under V_{DS} of 1.2 V. An extreme high I_{ON} of 1080 μA/μm can be achieved in Fig. 7(b) for TFTs with T_{ch} of 4.3 nm under V_{DS} of 0.8 V. The enhanced current drivability is attributed to the increased electron concentration and mobility with the increased T_{ch}.

B. Effects of Oxygen Annealing on TFT Performance

Fig. 8(a)–(d) illustrates bi-directional transfer characteristics of IGZO TFTs with T_{ch} of 1.5 nm and L_{ch} ranging from 1 μm to 60 nm under V_{DS} of 0.5 V, which have the as-deposited or O_2-annealed channel with respective annealing time of 1, 10, and 30 min. It is interesting to note that the as-deposited IGZO TFTs exhibit a large hysteresis window and negative ΔV_T with the decreased L_{ch}. With the increased O_2 annealing time, a shrinking hysteresis window and a reduced V_T variation among different L_{ch} can be observed accompanied by a decreased I_{ON}. The extracted V_T as a function of L_{ch} for as-deposited TFTs and O_2-annealed TFTs of different duration is depicted in Fig. 9(a). At least five devices of the same L_{ch} were measured for the average extraction with error bars standing for the standard deviation. It is found that an overall positively shifted V_T, an alleviated V_T roll-off and a smaller error bar can be achieved with the increased O_2 annealing time. This suggests that O_2 annealing could effectively reduce the trap states in IGZO TFTs, leading to the shrinking hysteresis window, more positive V_T and smaller device-to-device variation. These trap states are also the underlying reasons for the V_T roll-off at scaled L_{ch}.

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TABLE I
BENCHMARKING TABLE FOR ALD IGZO TFTS WITH OTHER RECENTLY REPORTED SPUTTERED IGZO TFTS

References	Structure	T_{ch} (nm)	L_{ch} (nm)	I_{on}/I_{off}	SS (mV/dec)	I_{on} @ V_{DS}=1V, V_{GS}-V_T=2 V	DIBL (mV/V)	V_T>0?
[3]	Back-gate	3.6	38	2×10^8	87	160	187	No
[4]	Top-gate	30	100	5×10^8	80	620	45	No
[5]	Back-gate	8	45	10^8	105	55	120	No
[6]	Top-gate	10	40	10^8	174	NA	NA	No
[7]	Back-gate	8	12.8	2×10^8	NA	635	NA	No
[8]	Double-gate	3	30	5×10^8	63	615	10	Yes
[9]	Back-gate	8	60	10^{11}	NA	800	NA	Yes
This work	Back-gate	**1.5**	**60**	**10^{11}**	**68**	**208**	**30**	**Yes**

NA: Not applied. It is noted that the reliability performance is not evaluated and the V_T roll-off issues also exist in previous reports [3-9].

To shed light on the function of oxygen annealing, XPS of O 1 s spectrum for 1 and 10 min O_2-annealed IGZO films with T_{ch} of 1.5 nm were taken. A significant reduction in oxygen vacancy and hydrogen contamination can be observed with the increased O_2 annealing time in Fig. 9(b). Both oxygen vacancy and hydrogen states have been recognized as donor states in IGZO, giving rise to excessive electrons and negative V_T in IGZO TFTs [20], [21], [22]. Thus, by reducing donor traps such as oxygen vacancy and hydrogen states, a more positive V_T, a reduced hysteresis window and smaller device-to-device variations can be achieved. The alleviated V_T roll-off could also be explained by the reduced donor traps in Fig. 9(c). These donor traps are promoted to migrate under high electric field in short-channel TFTs with less migration length, leading to the formation of current path under lower V_{GS} and resulting in lower V_T compared to that of long-channel TFTs. Thus, O_2 annealing could effectively reduce donor traps and suppress the formation of current path due to the migration of donor traps, alleviating the V_T roll-off at scaled L_{ch}. However, long-time O_2 annealing is also found to reduce I_{ON} significantly in Fig. 8. This could be explained by the increased R_C with the increased O_2 annealing time in Fig. 9(d), where R_C as a function of gate overdrive voltage ($V_{GS} - V_{th}$) are plotted for 1, 10, and 30 min O_2-annealed IGZO TFTs with T_{ch} of 1.5 nm. It is found that R_C is increased by ~four and ~tenfold when O_2 annealing time is increased from 1 to 10 min and 30 min, respectively. The increased R_C could be due to the reduced electron density in the channel, oxidation of metal contact, and the formation of interfacial barrier between metal contact and channel [23].

C. Positive Gate Bias Stability Test

The effects of O_2 annealing and T_{ch} on PBS performance of IGZO TFTs were also systematically investigated. During the PBS test, the gate is biased at V_T+ 3 V while the source and drain are grounded for a stress time of 2000 s. Fig. 10(a)–(c) exhibit the evolution of transfer characteristics of IGZO TFTs with L_{ch} of 80 nm and T_{ch} of 1.5 nm during PBS test, which have undergone different O_2 annealing time. It is interesting to note that the 1 min O_2-annealed TFTs show a negative ΔV_T of –134 mV whereas the 30 min O_2-annealed TFTs show a positive ΔV_T of +173 mV. The 10 min O_2-annealed TFTs exhibit a remarkably high PBS stability with a small ΔV_T of +53 mV. The transition of ΔV_T from negative to positive with increased O_2 annealing time can be observed in Fig. 10(d). On the other hand, the T_{ch} of IGZO TFTs is also found to play an important role in PBS performance. Fig. 10(e)–(g) exhibit the evolution of transfer characteristics of IGZO TFTs with L_{ch} of 80 nm and varying T_{ch} using the optimized 10 min O_2 annealing. It is also interesting to note that all TFTs exhibit negative ΔV_T and the magnitude of negative ΔV_T is also increased with the increased T_{ch}. The IGZO TFTs with T_{ch} of 2.2, 3.5, and 4.3 nm exhibit ΔV_T of –19, –160, and –231 mV, respectively. It is noted that the IGZO TFTs with T_{ch} of 2.2 nm also exhibit excellent PBS stability, with only marginal negative ΔV_T. Fig. 10(h) summaries the ΔV_T of IGZO TFTs with different T_{ch} and same O_2 annealing duration of 10 min as a function of stress time, where the transition from negative to positive can be observed with reduced T_{ch}.

Based on these observations, we propose a TNL model to explain the dependence of the electrical performance of IGZO TFTs on O_2 annealing and T_{ch} (Fig. 11). It is generally believed that the electron trapping at interface trap states leads to the positive ΔV_T under PBS test [24]. This could explain the electrical performance of IGZO TFTs in previous reports with large device dimensions and relatively low current drivability, aimed at display applications. However, for scaled devices with high current drivability, new defects could be generated under a high electric field and severe self-heating, which may be insignificant in previous IGZO TFTs. Thus, it is believed that the generation of different types of traps in addition to electron trapping could be the underlying mechanism, which can be described by the TNL model. In this model, the TNL level presents the branch point of the interface traps, below which traps are acceptor-like traps becoming electrically neutral if filled and above which are donor-like becoming electrically positive if empty [15], [25]. This could explain the PBS stability of IGZO TFTs with different T_{ch}, where the TNL moves from the conduction band into the E_g of IGZO with the reduced T_{ch}. As a result, the Fermi level (E_F) may reside in the conduction band of IGZO TFTs with

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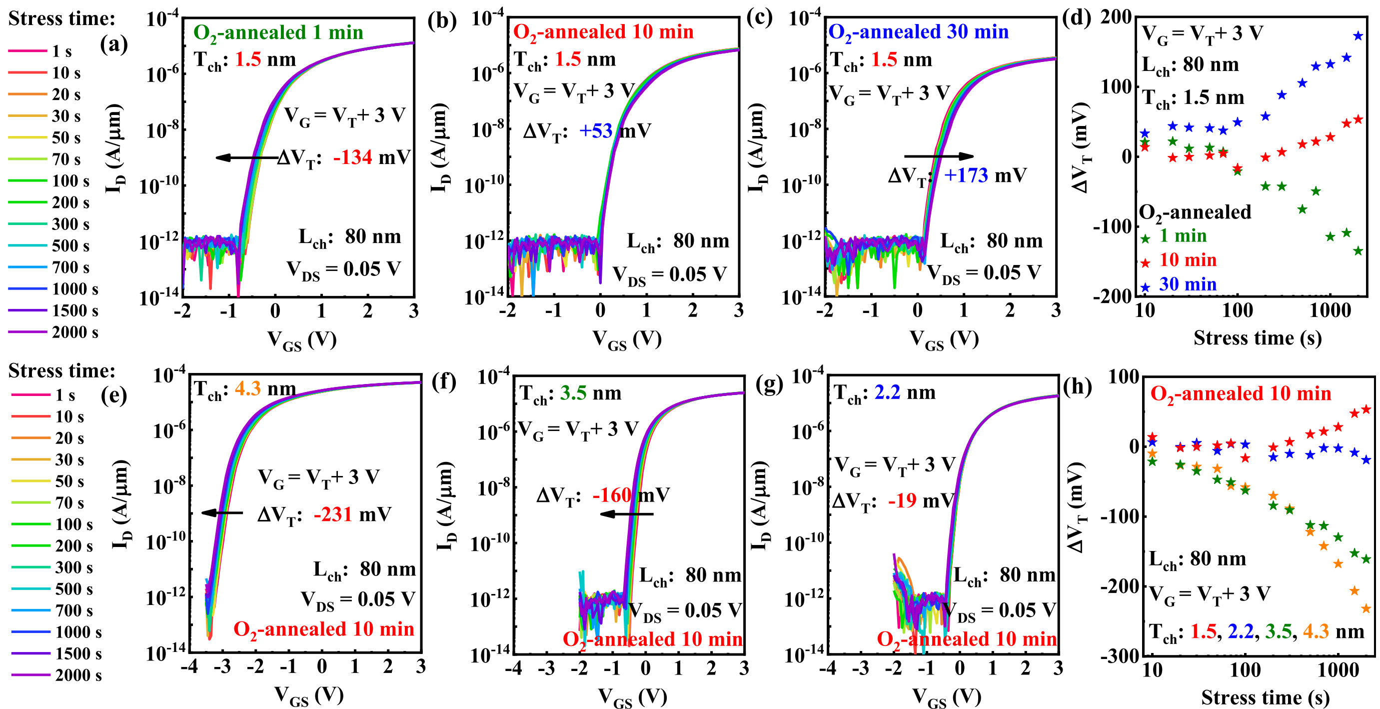

Fig. 10. Evolution of transfer curves of IGZO TFTs with L_{ch} of 80 nm and T_{ch} of 1.5 nm under gate stress voltage of V_T+ 3 V upon (a) 1 min, (b) 10 min, and (c) 30 min O_2 annealing. (d) Extracted ΔV_T as a function of stress time for IGZO TFTs with T_{ch} of 1.5 nm, where a transition from negative to positive can be observed with increased annealing time. Evolution of transfer curves of IGZO TFTs with L_{ch} of 80 nm and varying T_{ch} under gate stress voltage of V_T+ 3 V using 10 min O_2 annealing. (e) T_{ch} of 4.3 nm. (f) 3.5 nm. (g) 2.2 nm. (h) Extracted ΔV_T as a function of stress time for 10 min O_2-annealed IGZO TFTs with varying T_{ch}, where a transition from negative to positive can be observed with reduced T_{ch}.

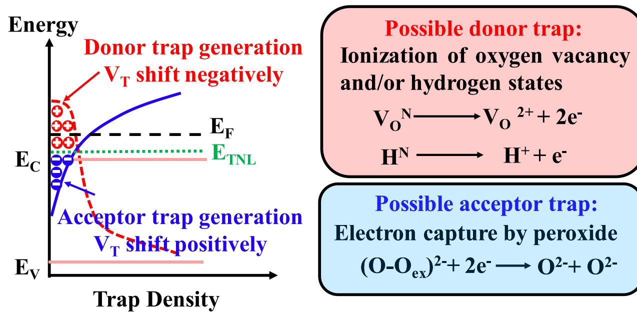

Fig. 11. Proposed TNL models and possible origins of two different types of traps, explaining the ΔV_T behaviors under PBS test for IGZO TFTs with different O_2 annealing conditions and varying T_{ch}.

large T_{ch} during the PBS test, precipitating the formation of donor-like traps and leading to the negative ΔV_T. For IGZO TFTs with small T_{ch}, the E_F still lies in the E_g of IGZO during PBS test and these in-gap states could function as acceptor-like traps, causing positive ΔV_T. The TNL model could also explain the dependence of PBS stability performance on O_2 annealing time. Similar to T_{ch}, increased O_2 annealing time could also move the TNL down toward the E_g of IGZO, which is evidenced by the positively shifted V_T, explaining the transition of ΔV_T from negative to positive. In addition, from XPS spectrum, these donor-like traps could be the ionized oxygen vacancy and/or hydrogen state [20], [21], [22], which could be significantly reduced by O_2 annealing. On the other hand, acceptor-like traps may origin from the peroxide state with excessive oxygen upon long-time O_2 annealing, which have been reported previously [26], [27], [28]. Thus, the TNL model could explain well the dependence of ΔV_T behaviors for IGZO TFTs on both O_2 annealing and T_{ch}, which provides a guidance of achieving a high bias stability by balancing these two types of traps.

D. Benchmarks

Table I benchmarks our ALD IGZO TFTs with other recently reported sputtered IGZO TFTs with sub-100 nm L_{ch}. Our ALD IGZO TFTs show comparable electrical performance with L_{ch} of 60 nm and a much thinner T_{ch} of 1.5 nm, including a high $I_{ON}/I_{OFF} \sim 10^{11}$, a decent high I_{ON} of 208 μA/μm under V_{DS} of 1 V and gate overdrive of 2 V, a steep SS of 68 mV/dec, a small DIBL of 30 mV/V and a normal-off operation, which is comparable to the state-of-art sputtered IGZO TFTs. Furthermore, the V_T roll-off at scaled L_{ch} is significantly resolved by optimizing O_2 annealing in this work, which also exists in previous sputtered IGZO TFTs [3], [4], [5], [6], [7], [8], [9]. Additionally, a remarkably high degree of stability to the PBS is also achieved in our ALD IGZO TFTs, which has not been evaluated in previous reports [3], [4], [5], [6], [7], [8], [9] and is of great importance for practical applications.

IV. Conclusion

In summary, we report for the first time BEOL-compatible IGZO TFTs with extremely scaled T_{ch} down to 1.5 nm and L_{ch} down to 60 nm by ALD. The effects of T_{ch} and O_2 annealing on the electrical performance of IGZO TFTs were systematically investigated. By using optimized O_2 annealing

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conditions, the ALD IGZO TFTs with scaled T_{ch} of 1.5 nm and L_{ch} of 60 nm exhibit desirable electrical performance including a high $I_{ON}/I_{OFF} \sim 10^{11}$, a decent high I_{ON} of 354 μA/μm under V_{DS} of 1.2 V, a steep SS of 68 mV/dec, a small DIBL of 30 mV/V, and a normal-off operation. Furthermore, the V_T roll-off issue at scaled L_{ch} is resolved together with a remarkably high degree of stability to the PBS, which could be explained well by a TNL trap model with possible microscopic origin. This study not only proves that ALD IGZO TFTs with excellent electrical performance could be highly promising for BEOL-compatible logic and memory applications toward monolithic 3-D integration, but also provide some new insights into underlying reason for reliability issues and undesirable electrical properties such as DIBL, V_T roll-off in scaled oxide TFTs.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[2] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, Feb. 2010, Art. no. 044305, doi: 10.1088/1468-6996/11/4/044305.

[3] J. Liu et al., "Low-power and scalable retention-enhanced IGZO TFT eDRAM-based charge-domain computing," in *IEDM Tech. Dig.*, Dec. 2021, p. 21, doi: 10.1109/IEDM19574.2021.9720576.

[4] K. Han et al., "First demonstration of oxide semiconductor nanowire transistors: A novel digital etch technique, IGZO channel, nanowire width down to 20 nm, and ion exceeding 1300 μA/μm," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[5] S. Subhechha et al., "First demonstration of sub-12 nm L_g gate last IGZO-TFTs with oxygen tunnel architecture for front gate devices," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[6] S. Samanta, K. Han, C. Sun, C. Wang, A. V. Thean, and X. Gong, "Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high $G_{m,max}$ of 125 μS/μm at V_{DS} of 1 V and I_{ON} of 350 μA/μm," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265052.

[7] C. Wang et al., "Extremely scaled bottom gate a-IGZO transistors using a novel patterning technique achieving record high gm of 479.5 μS/μm (VDS of 1 V) and fT of 18.3 GHz (VDS of 3 V)," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2022, pp. 294–295, doi: 10.1109/VLSITechnologyandCir46769.2022.9830393.

[8] K. Chen et al., "Scaling dual-gate ultra-thin a-IGZO FET to 30 nm channel length with record-high $G_{m,max}$ of 559 μS/μm at V_{DS} = 1 V, record-low DIBL of 10 mV/V and nearly ideal SS of 63 mV/dec," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2022, pp. 298–299, doi: 10.1109/VLSITechnologyandCir46769.2022.9830389.

[9] Q. Li et al., "BEOL-compatible high-performance a-IGZO transistors with record high $I_{ds,max}$ = 1207 μA/μm and on-off ratio exceeding 10^{11} at V_{DS} = 1 V," in *IEDM Tech. Dig.*, Dec. 2022, pp. 1–4, doi: 10.1109/IEDM45625.2022.10019448.

[10] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," *Nature Electron.*, vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: 10.1038/s41928-022-00718-w.

[11] M. Si et al., "Why In_2O_3 can make 0.7 nm atomic layer thin transistors," *Nano Lett.*, vol. 21, no. 1, pp. 500–506, Jan. 2021, doi: 10.1021/acs.nanolett.0c03967.

[12] J. Zhang, D. Zheng, Z. Zhang, A. Charnas, Z. Lin, and P. D. Ye, "Ultrathin InGaO thin film transistors by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 273–276, Feb. 2023, doi: 10.1109/LED.2022.3233080.

[13] M. H. Cho et al., "High-performance amorphous indium gallium zinc oxide thin-film transistors fabricated by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 688–691, May 2018, doi: 10.1109/LED.2018.2812870.

[14] M. H. Cho, C. H. Choi, H. J. Seul, H. C. Cho, and J. K. Jeong, "Achieving a low-voltage, high-mobility IGZO transistor through an ALD-derived bilayer channel and a Hafnia-based gate dielectric stack," *ACS Appl. Mater. Interfaces*, vol. 13, no. 14, pp. 16628–16640, Apr. 2021, doi: 10.1021/acsami.0c22677.

[15] A. Charnas, M. Si, Z. Lin, and P. D. Ye, "Improved stability with atomic-layer-deposited encapsulation on atomic-layer In_2O_3 transistors by reliability characterization," *IEEE Trans. Electron Devices*, vol. 69, no. 10, pp. 5549–5555, Oct. 2022, doi: 10.1109/TED.2022.3198926.

[16] S. Lee et al., "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 20, May 2011, Art. no. 203508, doi: 10.1063/1.3589371.

[17] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[18] P.-Y. Liao et al., "Alleviation of self-heating effect in top-gated ultrathin In_2O_3 FETs using a thermal adhesion layer," *IEEE Trans. Electron Devices*, vol. 70, no. 1, pp. 113–120, Jan. 2023, doi: 10.1109/TED.2022.3221358.

[19] P.-Y. Liao et al., "Transient thermal and electrical co-optimization of BEOL top-gated ALD In_2O_3 FETs on various thermally conductive substrates including diamond," in *IEDM Tech. Dig.*, Dec. 2022, p. 12, doi: 10.1109/IEDM45625.2022.10019438.

[20] B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," *Appl. Phys. Lett.*, vol. 97, no. 2, Jul. 2010, Art. no. 022108, doi: 10.1063/1.3464964.

[21] A. D. J. de Meux, A. Bhoolokam, G. Pourtois, J. Genoe, and P. Heremans, "Oxygen vacancies effects in a-IGZO: Formation mechanisms, hysteresis, and negative bias stress effects," *Phys. Status Solidi (A)*, vol. 214, no. 6, Jun. 2017, Art. no. 1600889, doi: 10.1002/pssa.201600889.

[22] Q. Kong et al., "New insights into the impact of hydrogen evolution on the reliability of IGZO FETs: Experiment and modeling," in *IEDM Tech. Dig.*, Dec. 2022, p. 30, doi: 10.1109/IEDM45625.2022.10019394.

[23] J. Zhang et al., "Fluorine-passivated In_2O_3 thin film transistors with improved electrical performance via low-temperature CF_4/N_2O plasma," *Appl. Phys. Lett.*, vol. 121, no. 17, Oct. 2022, Art. no. 172101, doi: 10.1063/5.0113015.

[24] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, Sep. 2008, Art. no. 093504, doi: 10.1063/1.2977865.

[25] D. Zheng et al., "First demonstration of BEOL-compatible ultrathin atomiclayer-deposited InZnO transistors with GHz operation and record high bias-stress stability," in *IEDM Tech. Dig.*, Dec. 2022, pp. 1–4, doi: 10.1109/IEDM45625.2022.10019452.

[26] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, "Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 9, Aug. 2011, Art. no. 093507, doi: 10.1063/1.3633100.

[27] H.-H. Nahm, Y.-S. Kim, and D. H. Kim, "Instability of amorphous oxide semiconductors via carrier-mediated structural transition between disorder and peroxide state," *Phys. Status Solidi (B)*, vol. 249, no. 6, pp. 1277–1281, Jun. 2012, doi: 10.1002/pssb.201147557.

[28] S. Choi et al., "Systematic decomposition of the positive bias stress instability in self-aligned coplanar InGaZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 580–583, May 2017, doi: 10.1109/LED.2017.2681204.

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