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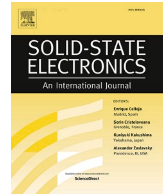

Current annealing to improve drain output performance of β-Ga_2O_3 field-effect transistor

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ABSTRACT

Current annealing, which utilizes high level of drain current during device fabrication, is proposed. A semiconductor device β-Ga_2O_3 field-effect transistor is preferred as test vehicle because of its inherently high drain current. With just a few seconds of current annealing, drain output performance can be boosted more than 50% without adding other processes. Both electrical measurements and numerical simulations are performed to investigate the annealing behavior. Especially, proposed substrate engineering to promote thermal isolation enables better power consumption during current annealing.

1. Introduction

Semiconductor technologies to improve drain output current (I_D) of field-effect transistors (FET) have been intensively studied for a long time. Most approaches can be put into three categories: material advances, device modifications, and development of novel fabrication processes. In terms of material engineering, traditional research has focused on improvement of wafer quality, which means minimization of surface roughness, defect density, and doping concentration. Nowadays, research challenges include discovering precursors for atomic layer deposition (ALD), controlling lattice strain in channels [1], engineering dipoles for high-*k* gate dielectric, and developing low resistive metal layers. In view of device design, source/drain (S/D) silicide and raised S/D have been applied to improve contact resistance. Moreover, multiple channel FET, which enlarges channel perimeter under the same footprint, has been spotlighted as a way to move beyond the FinFET era [2]. In addition, novel transistors employing vacuum channel have been introduced [3,4]. In terms of fabrication processing, extreme ultraviolet (EUV) has enabled device scaling below 10 nm. Moreover, interconnection delay can be reduced by aid of through-silicon vias (TSV).

However, despite the abovementioned research attempts, improvement in device performance has been modest. Hence, novel semiconductor technologies should evolve to keep Moore's law alive. Recently, transistor-level wafer annealing has been introduced as a novel semiconductor process [5]. The operation principle of the transistor-level annealing is based on the heating generated by current flowing through the electrodes on an FET. Hence, this type of annealing is known as electrothermal annealing (ETA) and current annealing (CA).

Implanted dopants can be thermally activated or poly-Si grain can be grown when the Joule heat temperature becomes sufficiently high [6–10]. Compared with traditional thermal annealing processes such as rapid thermal annealing (RTA), CA shows fast speed (sub-millisecond), and the maximum temperature can reach near the material melting point. Moreover, in the case of RTA, it is impossible to apply heat selectively within a wafer. Hence, there are layouts that are inevitably affected by unwanted high temperature heat. In contrast to RTA, CA shows excellent annealing selectivity, which enables annealing without affecting other layouts on the wafer. Considering these annealing speed and selectivity, CA can minimize unwanted dopant diffusion, and hence seems suitable for fabrication of extremely-scaled semiconductor devices below 5 nm. Moreover, CA can be applicable in back-end processes such as electrical testing (ET) or electrical die sorting (EDS).

In this work, we experimentally demonstrate the improvement of drain output performance of β-Ga_2O_3 FET. High drain bias (V_D) is intentionally applied for CA after fab-out. The output performance of β-Ga_2O_3 can be improved by 78% after CA. Then, electrothermal simulations based on a 3-D geometry were carried to understand heat distribution behavior during CA. Power consumption and annealing time

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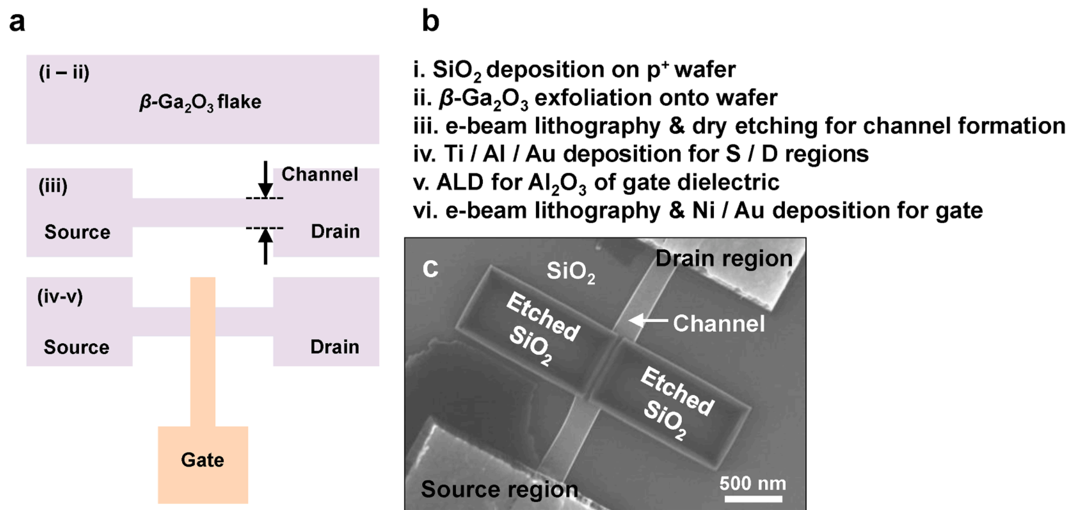

Fig. 1. (a) Top-view schematic of device fabrication process. (b) Summary of fabrication process flow. (c) SEM image of a β-Ga_2O_3 channel in step (iii).

Table 1
Bias conditions of β-Ga_2O_3 FET for CA.

	Bias Conditions
Gate Voltage, V_G	0 V
Source Voltage, V_S	0 V
Drain Voltage, V_D	25 V
Drain Current, I_D	170 μA
Power = $V_D \times I_D$	4.25 mW
Power Density = Power / nano-membrane size	708 W/mm^2
Annealing Time, t	10 s

optimization required for CA are studied with respect to substrate engineering. Finally, thermal interferences among other patterns are discussed to verify the possibility of using CA as a unit process.

2. Experimental details

A top-gated β-Ga_2O_3 FET was fabricated on a p^+- type (100) bulk silicon wafer as shown in Fig. 1. The buried oxide (BOX) with thickness of 270 nm was thermally oxidized, and Sn doped β-Ga_2O_3 nano-membranes with dimension of 5 μm length, 1.2 μm width, and 120 nm thickness were transferred from a crystal stone. To narrow the width of β-Ga_2O_3, BCl_3 / Ar gas mixture was used for inductively coupled plasma-reactive ion etching (ICP-RIE) [11]. The width of β-Ga_2O_3 shrank to 100 nm.

The average transferred nano-membrane size (A) was 6.0×10^{-6} mm^2. Then, S/D electrodes were formed by e-beam lithography and metal deposition (*i.e.*, Ti/Al/Au). Al_2O_3 gate dielectric with thickness of 15 nm was conformally deposited by ALD. Finally, gate with 1 μm length was defined by e-beam lithography and metal deposition (*i.e.*, Ni/Au). Detailed fabrication process flow and DC characteristics have been reported in previous works [12].

After device fabrication, CA based on DC measurements was performed by the parameter analyzer (Keithley 4200) under air ambient at room temperature. The detailed bias conditions for CA are summarized in Table 1.

3. Results and discussion

Fig. 2 shows measured *I-V* characteristics of fabricated β-Ga_2O_3 FET.

Table 2
Extracted device parameters after CA of β-Ga_2O_3 FET.

	Initial Fresh	Current Annealing	Improvement
SS (mV/dec)	226	106	53%
V_{TH} (V) @ 100 nA	−9.88	−8.74	11%
I_{ON} (μA) @ V_G = 0 V	2.79	4.98	78%
I_G (pA) @ V_G = −15 V	3.99	3.83	4%

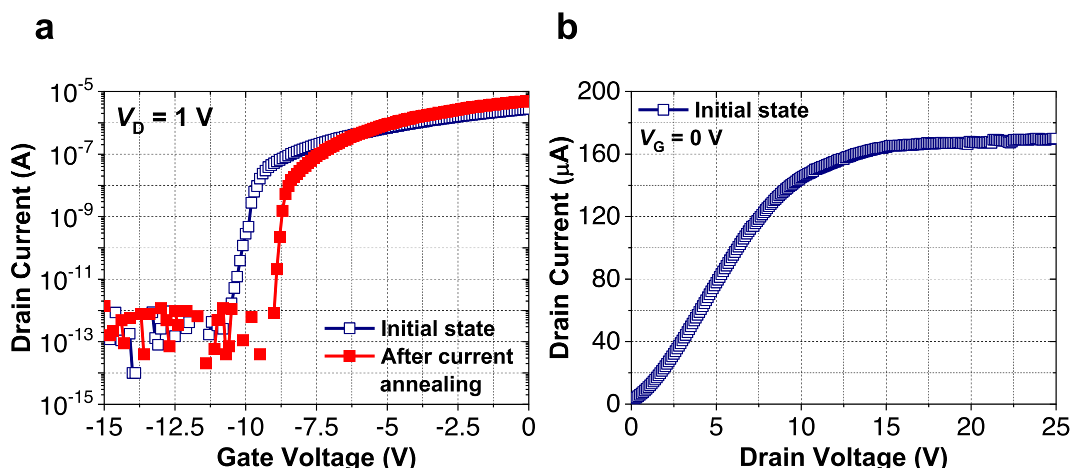

Fig. 2. (a) Measured I_D-V_G before and after CA. (b) I_D-V_D characteristic of β-Ga_2O_3 FET before CA.

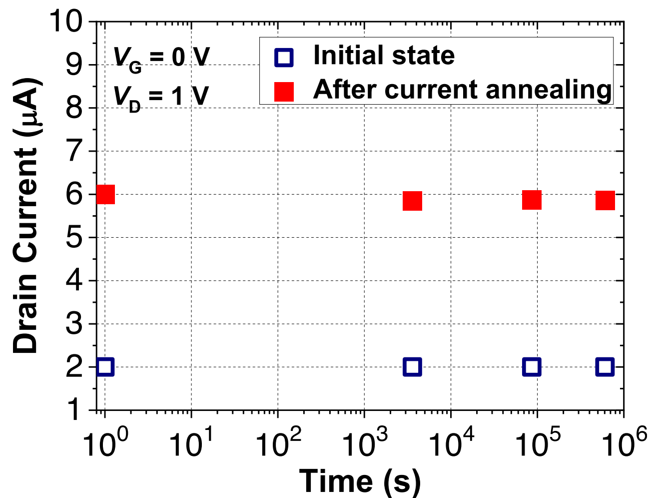

Fig. 3. Remeasured I_D of β-Ga_2O_3 FET until a few days later.

Table 3
Device Dimensions and Parameters for Simulations.

	Dimension	Material	κ [W/m·K]
Gate Length [μm]	1	Ni / Au	90 / 320
Gate Thickness [nm]	50 / 80		
Gate Dielectric Thickness [nm]	15	Al_2O_3	35
Channel Thickness [nm]	120	β-Ga_2O_3	10 [Ref. 13,14]
Channel Width [μm]	1.2		
S/D Thickness[nm]	15 / 60 / 50	Ti / Al / Au	22 / 237 / 320
Buried Oxide [nm]	270	SiO_2	1.4
Silicon Substrate Thickness [μm]	20	Si	130

After CA, drain output performance at $V_G = 0$ V, improved by 78% without increasing gate leakage (I_G). Moreover, the subthreshold swing (*SS*), which indicates power consumption during the off-state, decreased by 53% (Table 2). After CA, the contact resistance was reduced from 15 [Ω·cm] to 4.6 [Ω·cm], and the results coincided with those of the previous work [8]. Moreover, it is noteworthy that the improved I_D was sustained for a several days, as shown in Fig. 3. Considering previous results reported by H. Zhou *et al.*, [13] device temperature during CA is estimated to be around 120 °C under 708 W/mm^2 power density. The temperature range is low compared with the temperature in conventional thermal annealing processes such as RTA. Even though it is difficult to determine the exact mechanism involved in CA from current knowledge, trends similar to those found in this work have been reported. For example, J.-K. Han *et al.*, [7] and C.-K. Kim *et al.*, [9], reported I_D improvements of 29% and 158%, respectively, after CA. Both studies claimed that the mechanism of current boosting is associated with the removed contaminants such as photoresist (PR), moisture, or traps existing in channels. But, considering the generated heat, it can be inferred that the mechanism of current boosting in this work involves the removing of trap states, absorbed oxygen, and water molecules existing near the β-Ga_2O_3 flake. Even though the evidence is not sufficiently clear, it should be noted that there is something in common between the device structures in previous works [7,9] and this work. In terms of substrate, all studies have included thick SiO_2 isolation under devices. Moreover, applying Al_2O_3 as gate dielectric is also identical. Hence, it is difficult to clarify the origin of the improvement because it is still unclear whether specific isolation (*i.e.*, BOX) or the gate dielectric (*i.e.*, Al_2O_3) is associated with the current boosting.

In this context, the approach of using 3-D simulation seems suitable to investigate the heat distribution profile. Based on device geometry and the material properties as summarized in Table 3, numerical simulation was carried out with the aid of COMSOL. During the simulation, environment condition and heat transfer coefficient (*h*) were assumed to be air and 10 W/m^{2}K, respectively [13]. Fig. 4**a** shows the simulated heat distribution profile of the fabricated device. Most heat is concentrated at the middle of the channel; hence, the gate wrapping the channel shows the highest temperature in the image, as shown in Fig. 4**b**. The simulated hot-spot coincides that in the image taken by thermal reflectance (TR) microscopy [13].

Fig. 4**c** shows the simulated results from a distance. Considering the isothermal areas, the dominant heatsink is the substrate because of the high thermal conductivity of silicon. In other words, annealing efficiency can be further improved by modifying or engineering of the substrate. *J. Noh et al.*, [15] reported that temperature of a device fabricated on a diamond substrate was lower than that of a device on sapphire substrate. In this context, the better the thermal isolation in the substrate, the better the power efficiency in terms of CA. Fig. 5 shows the maximum simulated temperature during CA. Due to the severe thermal isolation stemming from the thicker BOX, device temperature increases under the same power density. However, power consumption efficiency during CA can be negligible when CA is built in an ET or EDS process. When CA is utilized as a unit process, the throughput is dependent not on the applied power but on the annealing time. Even though the annealing time in this work is 10 s, it is theoretically possible that the annealing time can be further shortened.

Hence, we should accomplish annealing time minimization based on the relationship between the temperature and the annealing time. The annealing time can be further reduced in two ways. The first is modification of isolation thickness. Fig. 6 shows time-dependent results according to BOX thickness. As the BOX thickness decreases, time required to reach the saturation region (*e.g.*, thermal time constant, τ_{th}) also decreases because the substrate lowers the thermal capacitance. For example, τ_{th} of 1.4 μs for a 270 nm BOX can be reduced to τ_{th} of 700 ns for a 100 nm BOX. Process can be made approximately 4 ns faster by reducing BOX layer by 1 nm. The second method of improvement is material engineering. Because a more highly thermally conductive isolation material (*e.g.* Si_3N_4) than SiO_2 is used as buried isolation in substrate, heat dissipation through the substrate increases [16,17]. Hence, thermal capacitance of the substrate decreases and τ_{th} becomes faster. When the 270 nm BOX layer is replaced by Si_3N_4 with the same thickness, τ_{th} decreased from 1.4 μs to 500 ns (not shown).

After CA, device drain output performance can be boosted. However, it is still not clear whether the boosting involves the applied electric-field or Joule heat. In this context, post-metal annealing (PMA) was performed for a device which had not been annealed by CA. PMA was performed by rapid thermal annealing (RTA) at 300 °C under 100% N_2 ambient for 30 s. Fig. 7 shows measured DC characteristic of device after PMA. After PMA, I_{ON} at $V_G = 0$ V improved by 25% without increasing *SS*. Thus, it can be inferred that the performance boosting after the CA is strongly associated with the heat generated during CA.

Fig. 8 shows simulation of device array to investigate the thermal interference during CA. Thermal interference along the patterns (or devices) should be considered when CA is applied as a unit process such as ET or EDS. The heat gradually decreased along the substrate (z) direction (Fig. 8**b**) due to the thermal isolation layer (*i.e.*, BOX). However, thermal interference along the x- and y-directions was negligible. In other words, owing to the high thermal conductivity of the gate metal, most of the Joule heat was emitted through the gate, and hence there was no thermal interference along the devices.

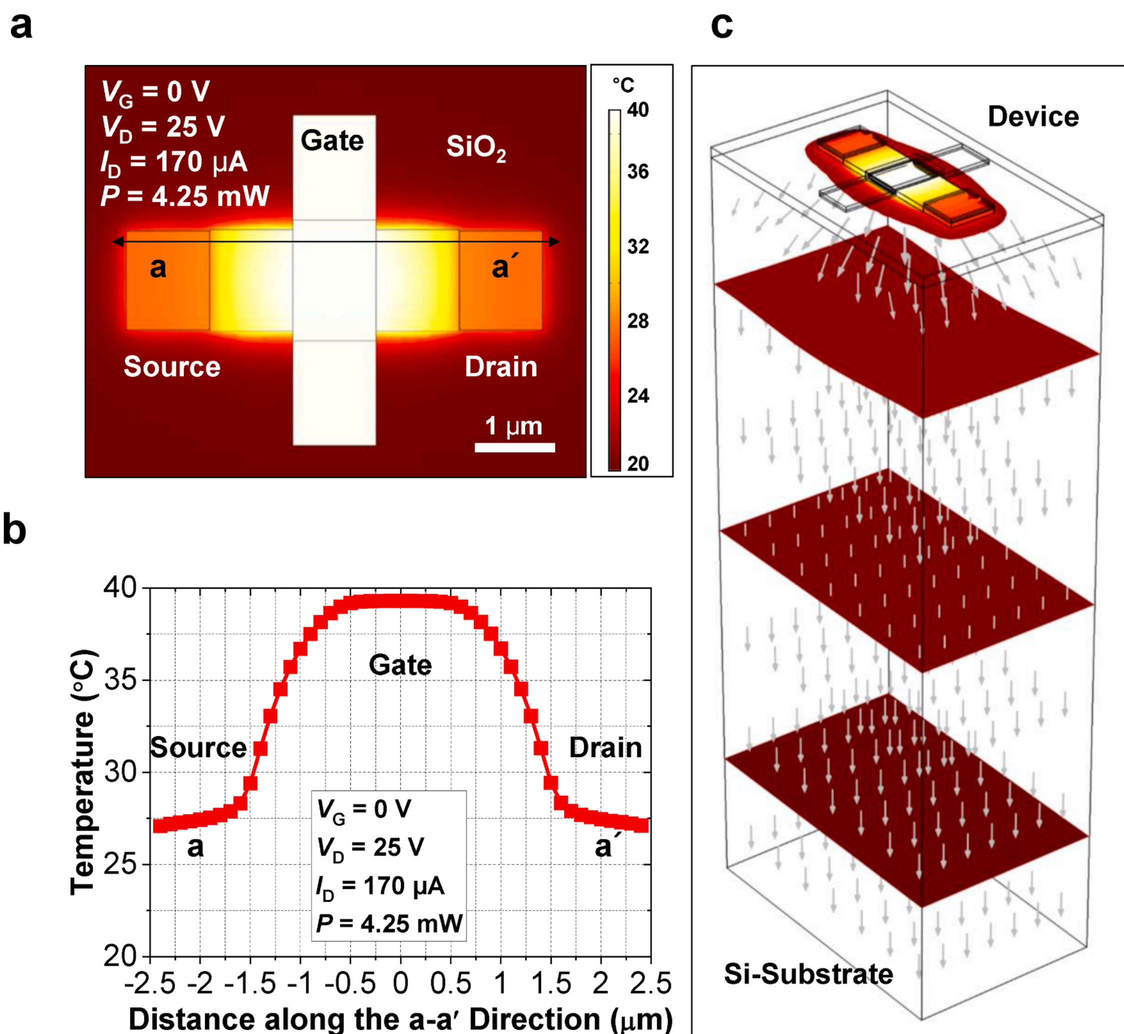

Fig. 4. (a) Top-view image of simulated heat distribution profile during CA. (b) Extracted temperature along a-á direction. (c) Bird's eye view with isothermal surfaces.

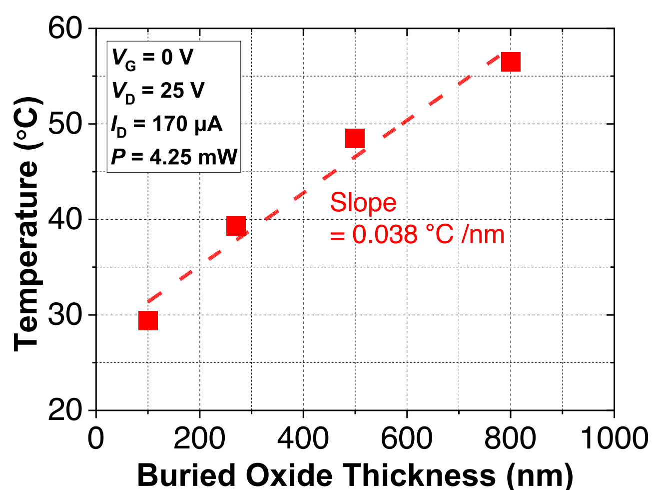

Fig. 5. Simulated maximum temperatures with various thicknesses of BOX in a substrate.

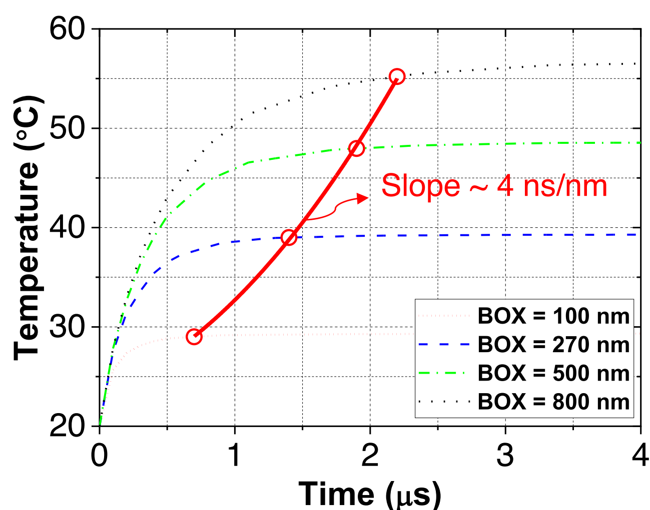

Fig. 6. Simulated transient characteristic of devices with various BOX thicknesses in substrate. $V_G = 0$ V, $V_D = 25$ V, $I_D = 170$ μA, Power = 4.25 mW. Open symbols indicate the saturation point (thermal time constant) for each BOX thickness.

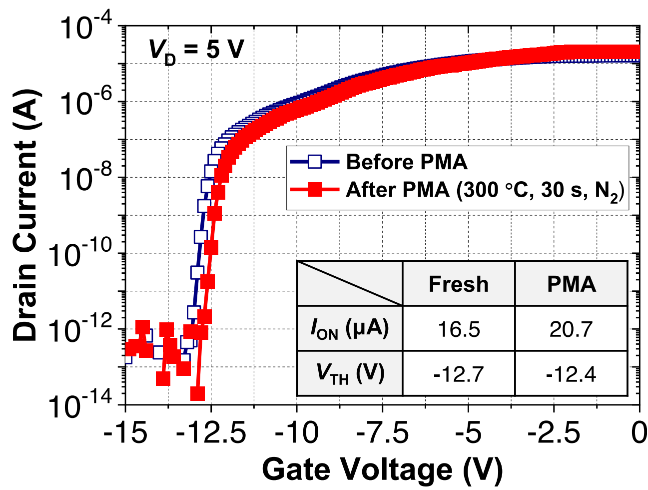

Fig. 7. Measured I_D-V_G characteristic after post-metal annealing.

4. Conclusion

Current annealing (CA), which utilizes current flow between the source and the drain, was suggested as an annealing process during device fabrication. After CA, the drain output performance of a β-Ga_2O_3 field-effect transistor (FET) was boosted by 78% without sacrificing other device parameters. Such performance boosting was associated with Joule heat induced during CA. Heat distribution profile including hot-spots and heat sink was obtained based on 3-D numerical simulations. Moreover, substrate engineering using buried oxide (BOX) was suggested to maximize annealing efficiency during CA. Finally, thermal interference for several devices on a chip was described to confirm the practicality of this work. There was no noticeable interference among the devices; hence, CA was found to be applicable to electrical testing (ET) and electrical die sorting (EDS) with auto-probing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

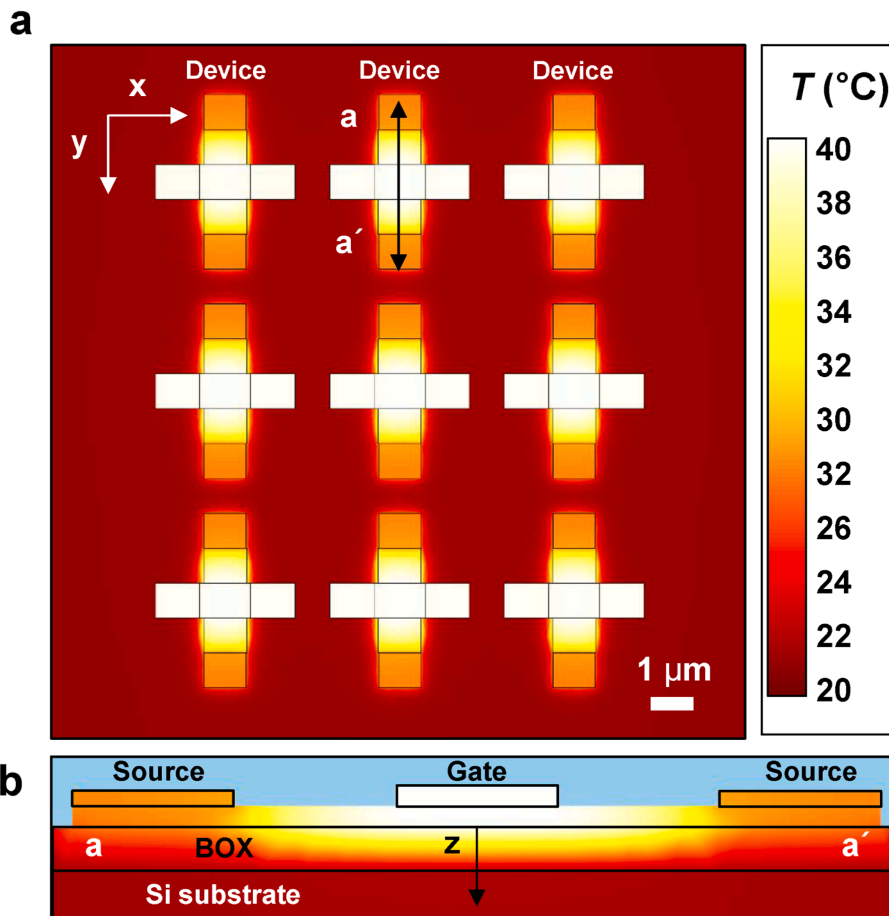

Fig. 8. (a) Heat distribution profile along devices. Maximum, minimum, and average device temperatures are 40.6 °C, 40.4 °C, and 40.5 °C, respectively. (b) Cross-sectional heat distribution profile along a-á direction.

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References

[1] Arimura H, et al. Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-DIT Si-cap-free Gate Stack and Optimizing the Channel Strain. IEEE Symp. VLSI Tech. 2020. https://doi.org/10.1109/VLSITechnology18217.2020.9265035.

[2] Mertens H, et al. Vertically stacked gate-all-around Si nanowire transistors: Key process optimizations and ring oscillator demonstration. *IEDM Tech. Dig.* 2017: 828–31. https://doi.org/10.1109/IEDM.2017.8268511.

[3] Han J-W, Sub Oh J, Meyyappan M. Vacuum nanoelectronics: Back to the future?—Gate insulated nanoscale vacuum channel transistor. Appl Phys Lett 2012;100(21): 213505. https://doi.org/10.1063/1.4717751.

[4] Han J-W, Seol M-L, Moon D-I, Hunter G, Meyyappan M. Nanoscale vacuum channel transistors fabricated on silicon carbide wafers. Nature Electron. 2019;2(9): 405–11. https://doi.org/10.1038/s41928-019-0289-z.

[5] Park J-Y, Lee B-H, Lee G-B, Bae H, Choi Y-K. Localized Electrothermal annealing with nanowatt power for a silicon nanowire field-effect transistor. ACS Appl Mater Interfaces 2018;10(5):4838–43. https://doi.org/10.1021/acsami.7b1779410.1021/acsami.7b17794.s001.

[6] Sameshima T, Kaneko Y, Andoh N. Rapid crystallization of silicon films using Joule heating of metal films. Appl Phys A, Solids Surf 2001;73(4):419–23. https://doi.org/10.1007/s003390100900.

[7] Han J-K, Park J-Y, Kim C-K, Kwon JH, Kim M-S, Hwang B-W et al. "Electrothermal Annealing to Enhance the Electrical Performance of an Exfoliated MoS2 Field-Effect Transistor," IEEE Electron Device Lett., in press. doi: 10.1109/LED.2018.2867569.

[8] Jeon C-H, Park J-Y, Seol M-L, Moon D-I, Hur J, Bae H, et al. Joule heating to enhance the performance of a gate-all-around silicon nanowire transistor. IEEE Trans. Electron Devices 2016;63(6):2288–92. https://doi.org/10.1109/TED.2016.2551751.

[9] Kim C-K, Kim E, Lee MK, Park J-Y, Seol M-L, Bae H, et al. Electrothermal Annealing (ETA) Method to Enhance the Electrical Performance of Amorphous-Oxide-Semiconductor (AOS) Thin-Film Transistors (TFTs). ACS Appl Mater Interfaces 2016;8(36):23820–6. https://doi.org/10.1021/acsami.6b06377.

[10] Moser J, Barreiro A, Bachtold A. Current-induced cleaning of graphene. pp. 163513-1–163513-3 Appl Phys Lett 2007;91. https://doi.org/10.1063/1.2789673.

[11] H. Bae et al., "First Demonstration of Robust Tri-Gate β-Ga2O3 Nano-Membrane Field-Effect Transistors Operated Up to 400 °C," arXiv:2105.01721, 2021.

[12] Zhou H, Si MW, Alghamdi S, Qiu G, Yang LM, Ye PD. High-Performance Depletion/Enhancement-Mode β-Ga_2O_3 on Insulator (GOOI) Field-Effect Transistors with Record Drain Currents of 600/450 mA/mm. IEEE Electron Device Lett. Jan. 2017; 38(1):103–6. https://doi.org/10.1109/led.2016.2635579.

[13] Zhou H, Maize K, Noh J, Shakouri A, Ye PD. Thermodynamic Studies of β-Ga_2O_3 nanomembrane field-effect transistors on a sapphire substrate. ACS Omega 2017;2 (11):7723–9. https://doi.org/10.1021/acsomega.7b0131310.1021/acsomega.7b01313.s001.

[14] Santia MD, Tandon N, Albrecht JD. Lattice thermal conductivity in β-Ga2O3 from first principles. pp. 041907-1–041907-4 Appl Phys Lett 2015;107(4). https://doi.org/10.1063/1.4927742.

[15] Noh J, et al. High performance $\beta-Ga_2O_3$ nano-membrane field effect transistors on a high thermal conductivity diamond substrate. IEEE J Electron Devices Soc 2019; 7:914–8. https://doi.org/10.1109/JEDS.2019.2933369.

[16] Zhang ZX, Lin Q, Zhu M, Lin CL. A new structure of SOI MOSFET for reducing self-heating effect. Ceram Int 2004;30(7):1289–93. https://doi.org/10.1016/j.ceramint.2003.12.033.

[17] Roig J, Flores D, Vellvehi M, Rebollo J, Millan J. Reduction of self-heating effect on SOIM devices. Microelectron Reliab 2002;42(1):61–6. https://doi.org/10.1016/S0026-2714(01)00116-0.

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