TWO-DIMENSIONAL MATERIALS

Negative capacitance gives a positive boost

Negative capacitance effect in a ferroelectric-based gate stack provides an effective solution for hysteresis-free steep-slope operation in a MoS_2 field-effect transistor.

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Nanoelectronics is facing many challenges at present in addition to aggressive scaling of complementary metal–oxide–semiconductor (CMOS) technology nodes (that is, the specific manufacturing processes and their design rules), driven by Moore's Law. For gate lengths of less than 10 nm, making metal–oxide–semiconductor field-effect transistors (MOSFETs) is no longer satisfactory, as the operation voltage scaling saturates at 0.7 V owing to exponentially increasing leakage power, creating inefficient energy consumption in the subthreshold region. This limitation has generated the intense quest for steep-slope transistors, devices with an inverse subthreshold slope (the amount of gate voltage required to achieve a tenfold increase in drain current) below 60 millivolts per decade at room temperature. The main solid-state contenders for steep-slope devices are tunnel FETs[1] and negative capacitance FETs (NC-FETs)[2]. Tunnel FETs show low currents, owing to fundamental limitations on current density of quantum mechanical band-to-band tunnelling, and therefore require sophisticated heterojunction embodiments to achieve a complementary MOSFET technology that offers reasonable logic performance[3]. Negative capacitance, in contrast, could act as a performance booster on any CMOS platform by improving both the slope and the overdrive voltage (Fig. 1).

Other performance limitations associated with the top-down silicon-based CMOS technology include low mobility, 2D quantum confinement and direct source-to-drain tunnelling at sub-10-nm channel dimensions, for which the fin field-effect transistor (FinFET) and the ultra-thin-body silicon-on-insulator architectures cannot offer satisfactory answers. Two-dimensional transition metal dichalcogenide semiconductors[4] may have the potential to address these challenges at ultimate scaling limits, potentially enabling the realization of a 1 nm transistor.

Now Si et al.[5], writing in *Nature Nanotechnology*, have taken advantage of negative capacitance to demonstrate a MoS_2 2D steep-slope transistor with a ferroelectric hafnium zirconium oxide layer (HZO) integrated in a bottom-gate dielectric stack. The device (Fig. 1d) shows low-voltage operation (below 1 V) and, most remarkably, quasi-non-hysteretic MOSFET behaviour, a challenging *sine qua non* condition to be fulfilled by ferroelectric high-*k* gate stacks with negative capacitance effect, if they are to be used in nanoscale logic circuits. The transistor consists of a monolayer to few-layer MoS_2 channel with a gate stack made of 2 nm amorphous aluminium oxide (Al_2O_3) and 20 nm polycrystalline

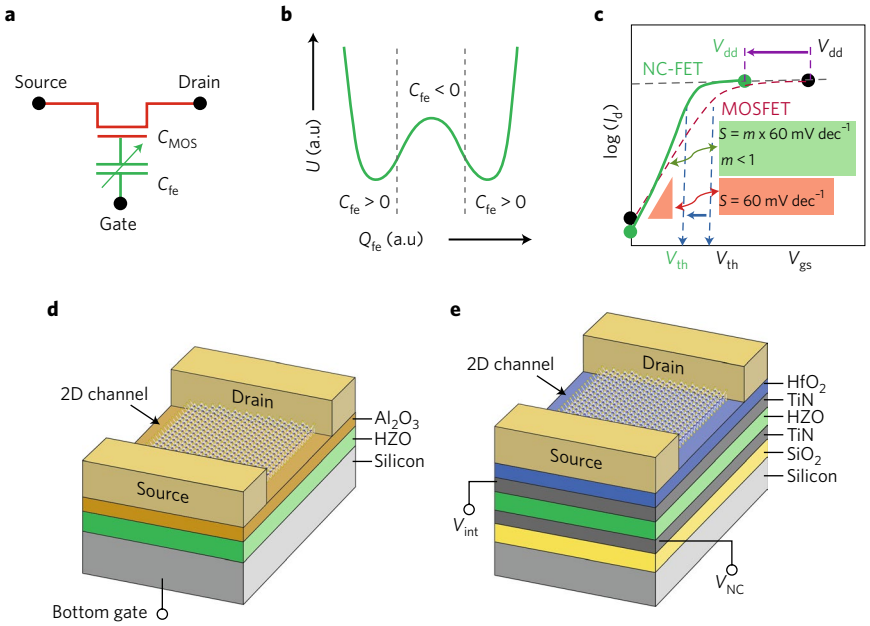

Fig. 1 | Negative capacitance FETs. a, Schematic of FET with a ferroelectric gate stack (ferroelectric capacitor on top of a classical dielectric). In this figure, C_{MOS} and C_{fe} are the equivalent capacitances of the MOSFET (including the connection of the depletion/semiconducting capacitance, C_S, and oxide capacitance) and of the ferroelectric, respectively. **b**, Energy landscape, U, of a ferroelectric capacitor in the absence of an applied voltage, highlighting the regions of positive and negative capacitance. When switching from one stable polarization to the other, the ferroelectric material passes through a region where the differential capacitance is negative, $C_{fe} = (d^2U/dQ_{fe}^2)^{-1} < 0$ (where Q_{fe} is charge) which makes the FET body factor m smaller than unity, providing internal amplification of the voltage in the gate, therefore lowering the subthreshold swing and reducing the overdrive voltage. **c**, Effect of negative capacitance performance boosting on the subthreshold slope, $S = [d\log(I_d)/dV_{gs}]^{-1}$ via a sub-unity body factor, $m = 1 + C_{MOS}/C_{fe}$, and on the overdrive voltage, $V_{dd} - V_{th}$, of the baseline FET. Here S is the subthreshold swing, I_d is the drain current, V_{th} is the threshold voltage and V_{gs} is the gate voltage. **d**, NC-FET device architecture proposed by Si et al.[5], featuring a HZO/Al_2O_3 bottom-gate stack. **e**, NC-FET device architecture reported by McGuire et al.[6], using a TiN/HZO/Tin/HfO_2 bottom-gate stack with an internal TiN plane (at internal potential V_{int}). The newly reported device[5] provides a unique simultaneous combination of hysteresis-free operation, low voltage and subthermionic steep slope.

HZO as the gate dielectric, all combined in a bottom-gate configuration built on a heavily doped silicon substrate. The ferroelectric HZO layer ensures the negative capacitance condition and CMOS-compatible manufacturing. In contrast to the recent report[6] showing a negative capacitance effect in a 2D device with relatively high gate voltages (close to −10 V) and hysteretic features in a structure with a metal plane (see Fig. 1e), this 2D steep-slope transistor has no metal plane in the gate stack and exhibits nearly hysteresis-free operation at CMOS-compatible voltages, which is consistent with the negative capacitance effect. This translates into a small subthermionic slope over up to four decades of current.

The result is supported by a systematic study of HZO polarization dependence on sweep-rate and the extraction of a negative drain-induced barrier lowering responsible for the observed negative differential resistance. Moreover, the slope shows no dependence on the channel thicknesses, which further reinforces the findings. In addition, the drain on-current level, I_d, of 510 μA μm^{-1} is among the highest values for state-of-the-art steep-slope tunnel FETs reported so far. The paper reports that a high on-current induces a self-heating effect in this type of 2D device. The demonstrated steep slope, high on/off ratio and hysteresis-free characteristics of the MoS_2 2D NC-FETs clearly show the potential of this device concept for future ultra-low-power 2D nanoelectronics. ❒

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