nature nanotechnology

LETTERS

https://doi.org/10.1038/s41565-017-0010-1

Steep-slope hysteresis-free negative capacitance MoS_2 transistors

Mengwei Si[1,2], Chun-Jung Su[3], Chunsheng Jiang[1,4], Nathan J. Conrad[1,2], Hong Zhou[1,2], Kerry D. Maize[1,2], Gang Qiu[1,2], Chien-Ting Wu[3], Ali Shakouri[1,2], Muhammad A. Alam[1] and Peide D. Ye[1,2]*

The so-called Boltzmann tyranny defines the fundamental thermionic limit of the subthreshold slope of a metal-oxide-semiconductor field-effect transistor (MOSFET) at 60 mV dec^{-1} at room temperature and therefore precludes lowering of the supply voltage and overall power consumption[1,2]. Adding a ferroelectric negative capacitor to the gate stack of a MOSFET may offer a promising solution to bypassing this fundamental barrier[3]. Meanwhile, two-dimensional semiconductors such as atomically thin transition-metal dichalcogenides, due to their low dielectric constant and ease of integration into a junctionless transistor topology, offer enhanced electrostatic control of the channel[4–12]. Here, we combine these two advantages and demonstrate a molybdenum disulfide (MoS_2) two-dimensional steep-slope transistor with a ferroelectric hafnium zirconium oxide layer in the gate dielectric stack. This device exhibits excellent performance in both on and off states, with a maximum drain current of 510 μA μm^{-1} and a sub-thermionic subthreshold slope, and is essentially hysteresis-free. Negative differential resistance was observed at room temperature in the MoS_2 negative-capacitance FETs as the result of negative capacitance due to the negative drain-induced barrier lowering. A high on-current-induced self-heating effect was also observed and studied.

Transition-metal dichalcogenides (TMDs) have been extensively explored as two-dimensional (2D) semiconductors for future device technologies. Atomically thin MoS_2 has been widely studied as a highly promising channel material because it offers ideal electrostatic control of the channel, ambient stability, an appropriate direct bandgap and moderate mobility. The TMD is generally configured in a junctionless (JL) form, with metal–semiconductor contacts replacing the source–drain p–n junctions of a bulk transistor. JL MoS_2 field-effect transistors (FETs) exhibit high on/off ratios and strong immunity to short channel effects for transistor applications with channel length L_{ch} down to sub-5 nm (refs. [4–12]). However, the power dissipation issue remains unresolved, similar to the situation for silicon-based metal–oxide–semiconductor FET (MOSFET) scaling. To overcome the thermionic limit, several novel device concepts have been proposed that have potential subthreshold slopes (SS) less than 60 mV dec^{-1} at room temperature, including impact-ionization FETs (II-FET)[13], tunnelling FETs (T-FET)[14,15], nanoelectromechanical FETs (NEMFET)[16] and negative-capacitance (NC) FETs[17–28]. In a NC-FET, the insulating ferroelectric layer serves as a negative capacitor so that the channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV dec^{-1} at room temperature[3]. The simultaneous fulfilment of internal gain and the non-hysteretic condition is crucial to the proper design of capacitance matching in a stable NC-FET. Meanwhile, channel transport in NC-FETs remains unperturbed. Therefore, coupled with the flatness of the body capacitance of TMD materials and symmetrical operation around the zero-charge point in a JL transistor, performance in 2D JL-NC-FETs is expected to improve for both on and off states. Accordingly, it would be highly desirable to integrate a ferroelectric insulator and 2D ultrathin channel materials to create a 2D JL-NC-FET to achieve high on-state performance for high operating speed and sub-thermionic SS for low power dissipation.

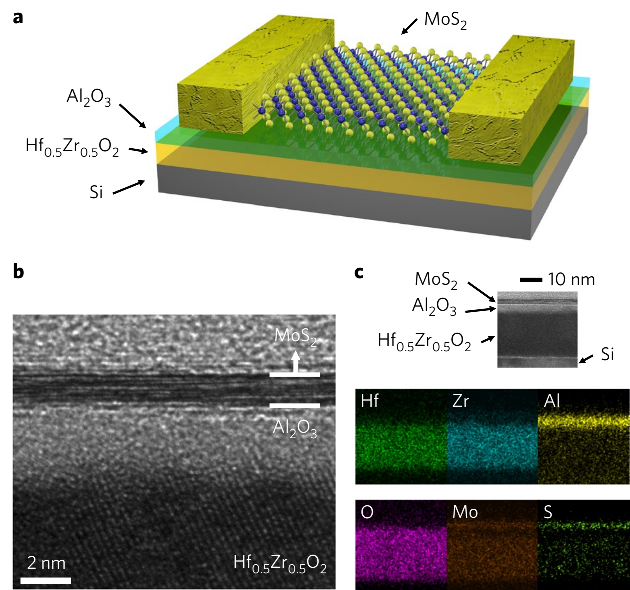

Fig. 1 | Schematic and fabrication of MoS_2 NC-FETs. a, Schematic view of a MoS_2 NC-FET. The gate stack includes heavily doped Si as the gate electrode, 20 nm HZO as the ferroelectric capacitor, 2 nm Al_2O_3 as the capping layer and capacitance-matching layer. A 100 nm Ni layer was deposited using an electron-beam evaporator as the source–drain electrode. **b**, Cross-sectional view of a representative sample showing the bilayer MoS_2 channel, amorphous Al_2O_3 and polycrystalline HZO gate dielectric. **c**, Corresponding EDS elemental map showing the distribution of Hf, Zr, Al, O, Mo and S.

[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA. [2]Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, USA. [3]National Nano Device Laboratories, Hsinchu 300, Taiwan. [4]Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, China. *e-mail: yep@purdue.edu

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.

Here, we demonstrate steep-slope MoS_2 NC-FETs by introducing ferroelectric hafnium zirconium oxide (HZO) into the gate stack. These transistors exhibit essentially hysteresis-free switching characteristics with a maximum drain current of 510 μA μm^{-1} and sub-thermionic SS. The maximum drain current of the NC-FETs fabricated in this work was found to be around five times larger than in MoS_2 FETs fabricated on 90 nm SiO_2 using the same process. As will be discussed in the following, this is a direct consequence of on-state current enhancement in a JL-NC-FET. Negative differential resistance (NDR), correlated to the negative drain-induced barrier lowering (DIBL) at the off state, is observed because of the drain-coupled negative capacitance effect. Remarkably, the high performance is sustained despite significant self-heating in the transistors, in contrast to traditional bulk MOSFETs.

The MoS_2 NC-FET shown in Fig. 1a consists of a monolayer to a dozen layers of MoS_2 as the channel, a 2 nm amorphous aluminium oxide (Al_2O_3) layer and a 20 nm polycrystalline HZO layer as the gate dielectric, heavily doped silicon substrate as the gate electrode and nickel source–drain contacts. HZO was chosen for its ferroelectricity, its CMOS-compatible manufacturing, and the ability to scale down its equivalent oxide thickness (EOT) to ultrathin dimensions[23–28]. The amorphous Al_2O_3 layer was applied for capacitance matching and gate leakage current reduction through the polycrystalline HZO. A cross-sectional transmission electron microscopy (TEM)

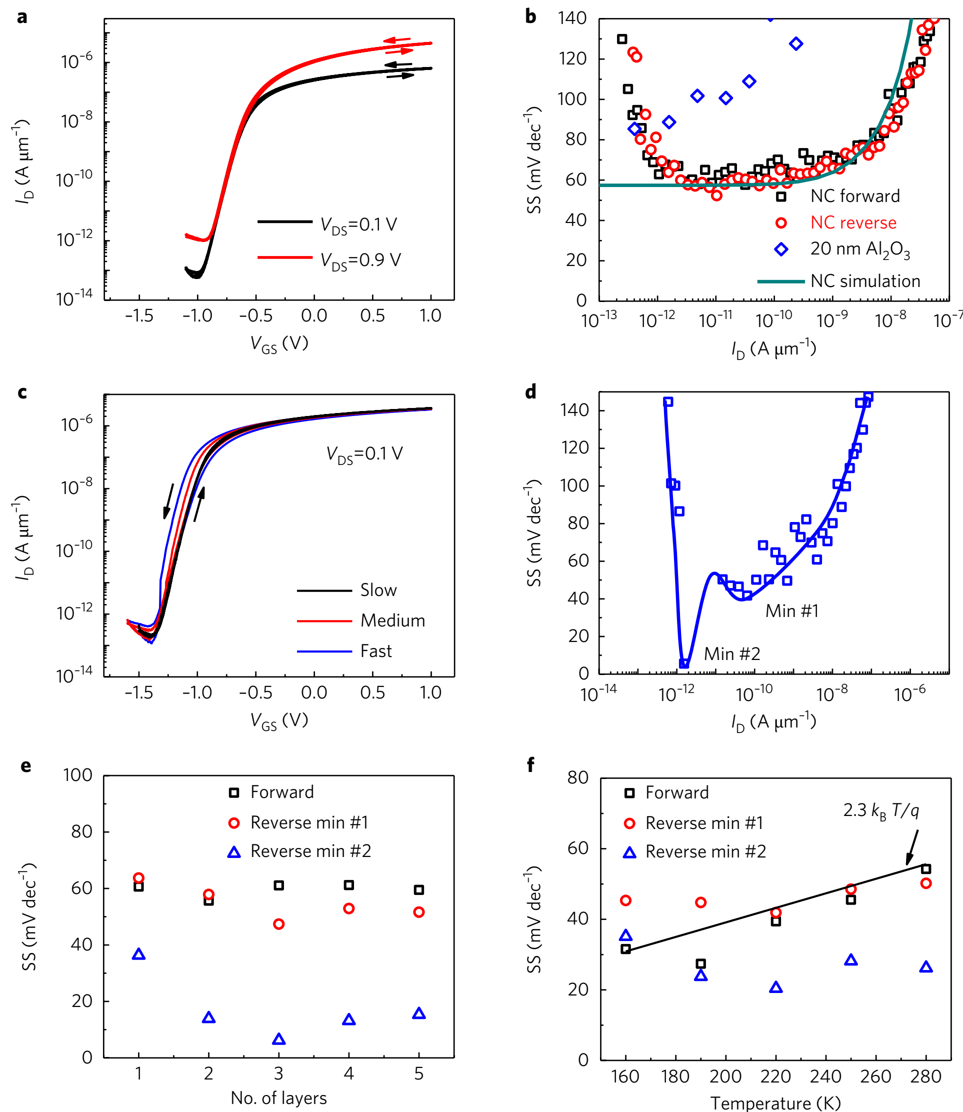

Fig. 2 | Off-state switching characteristics of MoS_2 NC-FETs. a, I_D–V_{GS} characteristics measured at room temperature and at V_{DS} = 0.1 V and 0.9 V. V_{GS} step is 0.5 mV. The thickness of the MoS_2 flake is 8.6 nm, measured by AFM. The device has a channel length of 2 μm and channel width of 3.2 μm, and RTA was performed at 500 °C during substrate preparation. **b**, SS versus I_D characteristics of the device in **a**, showing minimum SS below 60 mV dec^{-1} for both forward and reverse sweeps. Also shown is a comparison of SS versus I_D characteristics with simulation results on the same device structure and an experimental MoS_2 FET with 20 nm Al_2O_3 only as gate oxide. **c**, I_D–V_{GS} characteristics measured at room temperature and at V_{DS} = 0.1 V at different gate voltage sweep speeds. V_{GS} steps were set to be from 0.3 to 5 mV. The thickness of the MoS_2 flake is 5.1 nm. This device has a channel length of 1 μm and channel width of 1.56 μm. The RTA temperature was 400 °C for the gate dielectric. **d**, SS versus I_D characteristics during fast reverse sweep of the device in **c**. The SS versus I_D characteristics show two local minima (min #1 and min #2). min #2 suggests switching between different polarization states of the ferroelectric HZO. **e**, Layer dependence of SS for one to five layers. The SS of the MoS_2 NC-FETs shows weak thickness dependence. **f**, Temperature dependence of SS from 160 K to 280 K. The measured SS is below the thermionic limit down to 220 K. SS below 190 K is above the thermionic limit because of the stronger impact of the Schottky barrier on SS.

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.

image of a representative MoS_2 NC-FET is shown in Fig. 1b, and a detailed energy-dispersive X-ray spectrometry (EDS) elemental map is presented in Fig. 1c. The EDS analysis confirmed the presence and uniform distribution of elements Hf, Zr, Al, O, Mo and S. No obvious interdiffusion of Hf, Zr and Al was found. The gate stack was assessed for its rapid thermal annealing (RTA) temperature dependence with a metal–oxide–semiconductor capacitor structure by carrying out fast I–V measurements. Measured hysteresis loops for polarization versus electric field (P–E) as well as X-ray diffraction (XRD) results suggest that RTA at 400–500 °C after atomic layer deposition (ALD) enhances the ferroelectricity (Supplementary Section 1).

The electrical characteristics of MoS_2 NC-FETs are strongly dependent on the ferroelectricity of the HZO layer, which is defined by the film annealing temperature and gate–source voltage (V_{GS}) sweep speed. In addition to standard I–V measurements, hysteresis was measured as the difference in V_{GS} in forward (from low to high) and reverse (from high to low) V_{GS} sweeps at $I_D = 1$ nA μm^{-1} and $V_{DS} = 0.1$ V. Here, we study the room-temperature characteristics of MoS_2 NC-FETs. Figure 2a presents the I_D–V_{GS} characteristics of a device with the gate dielectric annealed at 500 °C, measured in V_{GS} steps of 0.5 mV. This device has a channel length of 2 μm, channel width of 3.2 μm and channel thickness of 8.6 nm. The hysteresis (~12 mV) is small and essentially negligible, consistent with theory for the NC-FET, and the gate leakage current I_G is negligible (Supplementary Section 2). Figure 2b presents SS vs I_D data for the device examined in Fig. 2a, as well as a comparison of the simulation results and experimental results with only 20 nm Al_2O_3 as the gate dielectric. MoS_2 FETs fabricated on a 20 nm Al_2O_3 conventional dielectric present a typical SS of 80–90 mV dec^{-1}, much larger than the values for NC-FETs. The SS was extracted for both forward sweep (SS_{For}) and reverse sweep (SS_{Rev}), and the device was observed to exhibit $SS_{Rev} = 52.3$ mV dec^{-1} and $SS_{For} = 57.6$ mV dec^{-1}. SS values below 60 mV dec^{-1} at room temperature are thus conclusively demonstrated for both forward and reverse sweeps in this near hysteresis-free device.

Because the HZO polarization depends on the sweep rate, electrical characterization of the MoS_2 NC-FETs was also carried out at different V_{GS} sweep speeds. This speed was controlled by modifying the V_{GS} measurement step from 0.3 mV to 5 mV. Figure 2c presents I_D–V_{GS} characteristics for a few-layer MoS_2 NC-FET measured at slow, medium and fast sweep speeds, corresponding to V_{GS} steps of 0.3, 1 and 5 mV. Hysteresis of the MoS_2 NC-FETs was found to be diminished by reducing the sweep speed. A plateau and a minimum characterize the SS vs I_D plot during the reverse sweep. These features ($SS_{Rev,min\#1}$ and $SS_{Rev,min\#2}$) were observed in almost all the fabricated devices when measured with fast sweep V_{GS}, as shown in Fig. 2d. The second local minimum of SS is the result of switching between two polarization states of the ferroelectric oxide, which is associated with loss of capacitance matching at high speed. When measured in fast sweep mode with a V_{GS} step of 5 mV, the device exhibits $SS_{For} = 59.6$ mV dec^{-1}, $SS_{Rev,min\#1} = 41.7$ mV dec^{-1} and $SS_{Rev,min\#2} = 5.6$ mV dec^{-1}. Overall, the average SS is less than 60 mV dec^{-1} for over four decades of drain current. In slow sweep

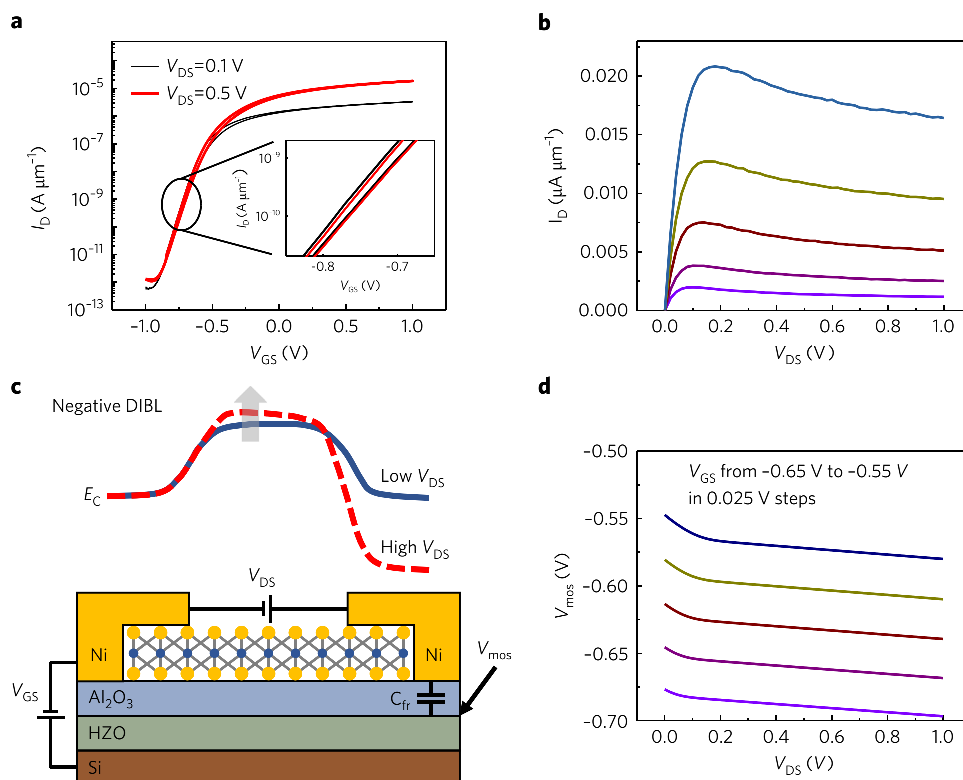

Fig. 3 | NDR and negative DIBL in MoS_2 NC-FETs. a, I_D–V_{GS} characteristics measured at room temperature and at $V_{DS} = 0.1$ V and 0.5 V. The V_{GS} step during measurement was 5 mV. Inset: Zoom-in of the I_D–V_{GS} curve between −0.8 and −0.7 V. A threshold voltage shift towards the positive can be observed at high V_{DS}, indicating a negative DIBL effect. The thickness of the MoS_2 flake is 5.3 nm, estimated from AFM characterization. This device has a channel length of 2 μm and channel width 5.6 μm. A 500 °C RTA procedure in N_2 was performed for 1 min during preparation of the gate dielectric. **b**, I_D–V_{DS} characteristics measured at room temperature at V_{GS} from −0.65 to −0.55 V in 0.025 V steps. Clear NDR can be observed because of the negative DIBL effect induced by negative capacitance. **c**, Band diagram of the negative DIBL effect. The negative DIBL origins from capacitance coupling from the drain to the interfacial layer between Al_2O_3 and HZO. **d**, Simulation of interfacial potential vs V_{DS}. When V_{DS} is increased, the interfacial potential is reduced, and the carrier density in the MoS_2 channel is reduced. Thus, the channel resistance is increased and drain current is reduced.

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.

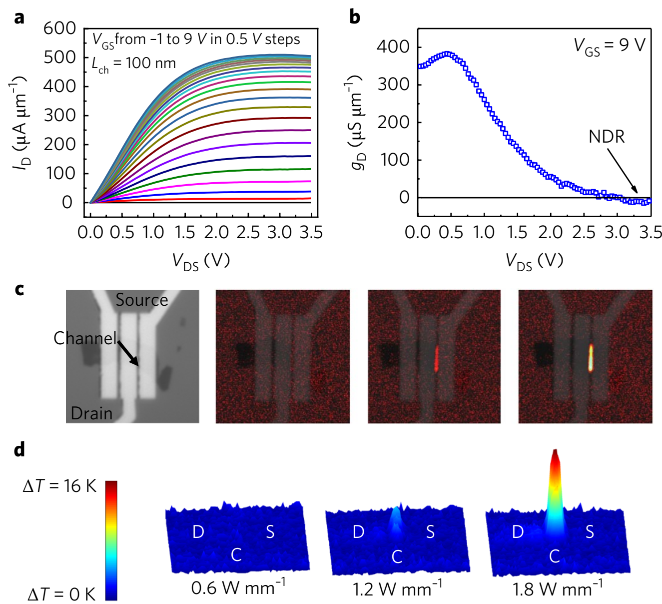

Fig. 4 | On-state characteristics and self-heating of MoS_2 NC-FETs. **a**, I_D–V_{DS} characteristics measured at room temperature at V_{GS} from −1 V to 9 V in 0.5 V steps. The thickness of the MoS_2 flake is 3 nm. This device has a channel length of 100 nm. The maximum stress voltage/EOT in this device is about 2 V nm^{-1}. Maximum drain current is 510 μA μm^{-1}. Clear negative drain differential resistance can be observed at high V_{GS}. **b**, g_D–V_{DS} characteristics for the device in **a** at V_{GS} = 9 V. g_D less than zero at high V_{DS} highlights the NDR effect due to self-heating. **c**,**d**, Thermoreflectance images (**c**) and temperature maps (**d**) at power densities from 0.6 W mm^{-1} to 1.8 W mm^{-1}. The heated channel suggests that the self-heating effect has to be taken into account in MoS_2 NC-FETs with large drain current.

mode, no obvious second local minimum and hysteresis can be observed, as shown in Fig. 2a, reflecting well-matched capacitances throughout the subthreshold region. Figure 2e shows the thickness dependence of SS from a monolayer to five layers of MoS_2 for the channel (see Supplementary Section 4 for determination of layer number). No obvious thickness dependence is observed. Figure 2f shows the temperature dependence of SS for a MoS_2 NC-FET measured from 280 K to 160 K. The measured SS is below the thermionic limit down to 220 K. SS below 190 K is above the thermionic limit because of the stronger impact of the Schottky barrier at lower temperatures. Detailed *I*–*V* characteristics at low temperature are provided in Supplementary Section 5.

Although the above MoS_2 NC-FET shows an average SS during reverse sweep of <60 mV dec^{-1} for more than four decades, low hysteresis is generally required for any transistor application. A detailed discussion of the non-hysteretic and internal gain conditions of the MoS_2 NC-FET is provided in Supplementary Section 7 using experimentally measured *P*–*E* results taken directly on HZO films. We found that both SS and hysteresis in MoS_2 NC-FETs are sensitive to the annealing temperature for the gate dielectric. The dependence of SS on different RTA temperatures was studied systematically (Supplementary Section 3), and it was found that MoS_2 NC-FETs with RTA at 400 °C and 500 °C have smaller SS values than as-grown samples and 600 °C annealed samples, as shown in Supplementary Fig. 4. This conclusion can also be obtained from the hysteresis loop of plots of *P*–*E*, because the gate stacks with RTA at 400 °C and 500 °C show larger remnant polarization, indicating stronger ferroelectricity. A statistical study on temperature-dependent hysteresis is provided in Supplementary Fig. 4d. It was found that MoS_2 NC-FETs with 500 °C RTA exhibit the lowest hysteresis when compared with devices without RTA and devices with RTA at 400 °C and 600 °C. Therefore, RTA temperature engineering could be useful in achieving both steep slope and low hysteresis.

DIBL is widely noted as major evidence for short-channel effects in MOSFETs[2]. In conventional MOSFETs, the threshold voltage V_{th} shifts in the negative direction, relative to the drain voltage. The DIBL, defined as $-\Delta V_{th}/\Delta V_{DS}$, is usually positive. It has been predicted theoretically that with a ferroelectric insulator introduced into the gate stack of a practical transistor, the DIBL could be reversed in NC-FETs[29]. NDR can occur naturally as a result of the negative DIBL effect. Figure 3a shows negative DIBL in the I_D–V_{GS} characteristics of another device with a channel length of 2 μm, channel width of 5.6 μm, channel thickness of 7.1 nm, and with 2 nm Al_2O_3 and 20 nm HZO as the gate dielectric. It is evident that the I_D–V_{GS} curve shifts positively when V_{DS} increases from 0.1 to 0.5 V. As this negative DIBL occurs around the off state, NDR is also observed simultaneously in the same device in the off state, as shown in Fig. 3b. Figure 3c presents the band diagram for the negative DIBL effect. This negative DIBL originates from capacitance coupling from the drain to the interfacial layer between Al_2O_3 and HZO. The interfacial layer potential V_{mos} can be estimated as a constant when the thickness of the ferroelectric oxide layer is thin (Supplementary Section 7). Simulation of V_{mos} shows that, when V_{DS} is increased, the interfacial potential is reduced (Fig. 3d), indicating that the carrier density in the MoS_2 channel is reduced. Thus, the channel resistance is increased, leading to the NDR effect.

The EOT of the gate stack (2 nm Al_2O_3 and 20 nm HZO) in this work was measured to be 4.4 nm by *C*–*V* measurements. The breakdown voltage was consistently measured to be ~11 V. Breakdown voltage/EOT was 2.5 V nm^{-1}, which is about 2.5 times larger than the value for SiO_2. It can be verified easily that breakdown voltage/EOT is proportional to the electric displacement field. As it is well known from Maxwell's equations that the electric displacement field is proportional to charge density, higher breakdown voltage/EOT could lead to a higher carrier density. Figure 4a presents the I_D–V_{DS} characteristics (measured at room temperature) of a MoS_2 NC-FET with 100 nm channel length. The thickness of the MoS_2 flake is 3 nm. The gate voltage was stressed up to 9 V and the maximum gate voltage/EOT in the device was ~2 V nm^{-1}. A maximum drain current of 510 μA μm^{-1} was achieved, which is about five times larger than in control devices using 90 nm SiO_2 as the gate dielectric. Note that this maximum drain current was obtained without special contact engineering such as doping[11] or using a heterostructure contact stack[10]; indeed, as discussed in the Supplementary Section 7, the JL topology is key to improving the performance of the transistor. This is an important but unexplored advantage of using a ferroelectric gate stack to enhance on-state performance. Another type of NDR (Fig. 4b) is also clearly observed when the device is biased at high V_{GS} because of the self-heating effect from large drain current and voltage. Figure 4c presents thermo-reflectance images taken at power densities from 0.6 W mm^{-1} to 1.8 W mm^{-1}. The heated channel, with its temperature increased to ~40 °C, suggests the self-heating effect. This potentially degrades channel mobility and limits the maximum drain current, and thus has to be taken into account in MoS_2 NC-FETs.

In conclusion, we have successfully demonstrated MoS_2 2D NC-FETs with promising on- and off-state characteristics. The stable, non-hysteretic and bidirectional sub-thermionic switching characteristics have been unambiguously confirmed to be the result of a NC effect. On-state performance is enhanced, with a maximum drain current of 510 μA μm^{-1} at room temperature, which leads to the self-heating effect. Finally, we have shown that the observed NDR is induced by the negative DIBL effect. After submission and during revision of this manuscript, the authors became aware of a related work being published[30].

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.

Methods

Methods, including statements of data availability and any associated accession codes and references, are available at https://doi.org/10.1038/s41565-017-0010-1.

Received: 21 March 2017; Accepted: 21 September 2017;
Published online: 18 December 2017

References

1. Ionescu, A. M. & Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329–337 (2011).
2. Sze, S. M. & Ng, K. *Physics of Semiconductor Devices* 3rd edn (Wiley, Hoboken, New Jersey, 2008).
3. Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett.* **8**, 405–410 (2008).
4. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nature Nanotech.* **6**, 147–150 (2011).
5. Liu, H., Neal, A. T. & Ye, P. D. Channel length scaling of MoS_2 MOSFETs. *ACS Nano* **6**, 8563–8569 (2012).
6. Das, S., Chen, H.-Y., Penumatcha, A. V. & Appenzeller, J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013).
7. Wang, H. et al. Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **12**, 4674–4680 (2012).
8. Desai, S. B. et al. MoS_2 transistors with 1-nanometer gate lengths. *Science* **354**, 99–102 (2016).
9. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
10. Liu, Y. et al. Pushing the performance limit of sub-100 nm molybdenum disulfide transistors. *Nano Lett.* **16**, 6337–6342 (2016).
11. Yang, L. et al. Chloride molecular doping technique on 2D materials: WS_2 and MoS_2. *Nano Lett.* **14**, 6275–6280 (2014).
12. Liu, L., Lu, Y. & Guo, J. On monolayer MoS_2 field-effect transistors at the scaling limit. *IEEE Trans. Electron. Dev.* **60**, 4133–4139 (2013).
13. Gopalakrishnan, K., Griffin, P. B. & Plummer, J. D. I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q. *Proc. IEEE Int. Electron. Dev. Meet.* 289–292 (2002).
14. Appenzeller, J., Lin, Y.-M., Knoch, J. & Avouris, P. Band-to-band tunneling in carbon nanotube field-effect transistors. *Phys. Rev. Lett.* **93**, 196805 (2004).
15. Sarkar, D. et al. A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **526**, 91–95 (2015).
16. Abele, N. et al. Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor. *Proc. IEEE Int. Electron. Dev. Meet.* 479–481 (2005).
17. Dubourdieu, C. et al. Switching of ferroelectric polarization in epitaxial $BaTiO_3$ films on silicon without a conducting bottom electrode. *Nature Nanotech.* **8**, 748–754 (2013).
18. Jain, A. & Alam, M. A. Stability constraints define the minimum subthreshold swing of a negative capacitance field-effect transistor. *IEEE Trans. Electron. Dev.* **61**, 2235–2242 (2014).
19. Khan, A. I. et al. Negative capacitance in a ferroelectric capacitor. *Nat. Mater.* **14**, 182–186 (2015).
20. Zubko, P. et al. Negative capacitance in multidomain ferroelectric superlattices. *Nature* **534**, 524–528 (2016).
21. McGuire, F. A., Cheng, Z., Price, K. & Franklin, A. D. Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer. *Appl. Phys. Lett.* **109**, 093101 (2016).
22. Wang, X. et al. Ultrasensitive and broadband MoS_2 photodetector driven by ferroelectrics. *Adv. Mater.* **27**, 6575–6581 (2015).
23. Salvatore, G. A., Bouvet, D. & Ionescu, A. M. Demonstration of subthreshold swing smaller than 60 mV/decade in Fe-FET with P(VDF-TrFE)/SiO_2 gate stack. *Proc. IEEE Int. Electron. Dev. Meet.* 167–170 (2008).
24. Muller, J. et al. Ferroelectricity in simple binary ZrO_2 and HfO_2. *Nano Lett.* **12**, 4318–4323 (2012).
25. Cheng, C. H. & Chin, A. Low-voltage steep turn-on pMOSFET using ferroelectric high-κ gate dielectric. *IEEE Electron. Dev. Lett.* **35**, 274–276 (2014).
26. Lee, M. H. et al. Prospects for ferroelectric $HfZrO_x$ FETs with experimentally CET = 0.98 nm, SS_{for} = 42 mV/dec, SS_{rev} = 28 mV/dec, switch-off <0.2V, and hysteresis-free strategies. *Proc. IEEE Int. Electron. Dev. Meet.* 616–619 (2015).
27. Zhou, J. et al. Ferroelectric $HfZrO_x$Ge and GeSn PMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved I_{DS}. *Proc. IEEE Int. Electron. Dev. Meet.* 310–313 (2016).
28. Li, K. S. et al. Sub-60mV-swing negative-capacitance FinFET without hysteresis. *Proc. IEEE Int. Electron. Dev. Meet.* 620–623 (2015).
29. Ota, H. et al. Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration. *Proc. IEEE Int. Electron. Dev. Meet.* 318–321 (2016).
30 McGuire, F. A. et al. Sustained sub-60 mV/decade switching via the negative capacitance effect in MoS transistors. *Nano Lett.* **17**, 4801–4806 (2017).

Acknowledgements

This material is based upon work partly supported by the Air Force Office of Scientific Research (AFOSR)/National Science Foundation (NSF) Two-Dimensional Atomic-layer Research and Engineering (2DARE) programme, Army Research Office (ARO) and Semiconductor Research Corporation (SRC).

Author contributions

P.D.Y. conceived the idea and supervised the experiments. C.J.S. performed the ALD of HZO and Al_2O_3 and dielectric physical analysis. M.S. performed the device fabrication, d.c. and *C*–*V* measurements, and data analysis. M.S. and N.J.C. carried out the fast *I*–*V* measurement. M.S. and G.Q. performed the AFM measurement. H.Z., K.D.M. and A.S. did the thermo-reflectance imaging. G.Q. performed the Raman and photoluminescence experiment. C.T.W. conducted TEM and EDS analyses. C.J. and A.M.A. conducted the theoretical calculations and analysis. M.S., A.M.A. and P.D.Y. summarized the manuscript and all authors commented on it.

Competing financial interests

The authors declare no competing financial interests.

Additional information

Supplementary information is available for this paper at https://doi.org/10.1038/s41565-017-0010-1.

Reprints and permissions information is available at www.nature.com/reprints.

Correspondence and requests for materials should be addressed to P.D.Y.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.

Methods

ALD deposition. $Hf_{1-x}Zr_xO_2$ film was deposited on a heavily doped silicon substrate. Before deposition, the substrate was cleaned by RCA standard cleaning and a diluted HF dip to remove organic and metallic contaminants, particles and unintentional oxides, followed by a deionized water rinse and drying. The substrate was then transferred to an ALD chamber to deposit $Hf_{1-x}Zr_xO_2$ film at 250 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr) and H_2O as the Hf precursor, Zr precursor and oxygen source, respectively. The $Hf_{1-x}Zr_xO_2$ film ($x=0.5$) was achieved by controlling the HfO_2:ZrO_2 cycle ratio of 1:1. To encapsulate the $Hf_{1-x}Zr_xO_2$ film, an Al_2O_3 layer was in situ deposited using $Al(CH_3)_3$ (TMA) and H_2O, also at 250 °C.

Device fabrication. A 20 nm $Hf_{0.5}Zr_{0.5}O_2$ layer was deposited by ALD as a ferroelectric insulator layer on the heavily doped silicon substrate after standard surface cleaning. Another 10 nm aluminium oxide layer was deposited as an encapsulation layer to prevent the degradation of HZO by reaction with moisture in the air. A BCl_3/Ar dry etching process was carried out to adjust the thickness of the Al_2O_3 down to 2 nm for capacitance matching. The rapid thermal annealing process was then performed in nitrogen ambient for 1 min at various temperatures. MoS_2 flakes were transferred to the substrate by scotch tape-based mechanical exfoliation. Electrical contacts formed from a 100 nm nickel electrode were fabricated using electron-beam lithography, electron-beam evaporation and a lift-off process.

Device characterization. The thickness of the MoS_2 was measured using a Veeco Dimension 3100 atomic force microscope (AFM) system. Electrical (d.c.) characterization was carried out with a Keysight B1500 system. Fast I–V measurements were performed using a Keysight B1530A fast measurement unit, and C–V measurements with an Agilent E4980A LCR meter. Room-temperature electrical data were collected with a Cascade Summit probe station and low-temperature electrical data were collected with a Lakeshore TTP4 probe station. Thermoreflectance imaging was done with a Microsanj thermoreflectance image analyser. Raman and photoluminescence measurements were carried out on a HORIBA LabRAM HR800 Raman spectrometer.

Data availability. The data that support the findings of the study are available from the corresponding author upon reasonable request.

© 2017 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.