Fabrication of fully transparent nanowire transistors for transparent and flexible electronics

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The development of optically transparent and mechanically flexible electronic circuitry is an essential step in the effort to develop next-generation display technologies, including ‘see-through’ and conformable products. Nanowire transistors (NWTs) are of particular interest for future display devices because of their high carrier mobilities compared with bulk or thin-film transistors made from the same materials, the prospect of processing at low temperatures compatible with plastic substrates, as well as their optical transparency and inherent mechanical flexibility. Here we report fully transparent In$_2$O$_3$ and ZnO NWTs fabricated on both glass and flexible plastic substrates, exhibiting high-performance n-type transistor characteristics with ~82% optical transparency. These NWTs should be attractive as pixel-switching and driving transistors in active-matrix organic light-emitting diode (AMOLED) displays. The transparency of the entire pixel area should significantly enhance aperture ratio efficiency in active-matrix arrays and thus substantially decrease power consumption.

In view of the inherent limitations of silicon-based electronic circuits and the demand for portable display/communication/computational/identification products, the development of high-performance transparent devices is the focus of much activity. The availability of optically transparent and mechanically flexible electronic circuitry could open the door to next-generation display technologies, including ‘see-through’ and conformable products.

Poly-silicon thin-film transistors (poly-Si TFTs) and amorphous-silicon thin-film transistors (α-Si TFTs) are widely used to fabricate commercial displays1–3, but their lack of transparency limits their utility in transparent device applications. In this regard, recent transparent transistor research efforts have focused on enhancing transparency and flexibility while maintaining or enhancing key TFT performance metrics. There have been several recent reports of transparent transistors fabricated with ZnO, SnO$_2$, In$_2$O$_3$ or other semiconducting oxide thin films, or with carbon nanotube networks as the active channel layers and opaque source and drain metals, or with carbon nanotube films and transparent source/drain electrodes4–11. However, there have been no reports of fully transparent oxide nanowire transistors (NWTs) fabricated with all-transparent gate and source/drain electrodes and displaying high transistor performance.

In$_2$O$_3$ and ZnO nanowires are particularly promising candidates for transistor active channels satisfying these requirements because they are both transparent and mechanically robust/flexible. Furthermore, indium-tin oxide (ITO) and indium-zinc oxide (IZO) are attractive transparent conductors for gate and source/drain electrodes12–14. In addition to transparency, transistor performance metrics such as high on-current ($I_{on}$), high on/off current ratio ($I_{on}/I_{off}$), high field-effect mobility ($\mu_{eff}$), steep subthreshold slope (S) and small threshold voltage ($V_{th}$) variation during transistor operation are required to realize commercially viable logic circuits and display devices.

Recent studies of NWTs have reported stable, high-performance transistor characteristics rivalling or surpassing those of α-Si and poly-Si TFTs, especially for $\mu_{eff}$ and S (refs 15–18). The mobility observed in the present study exceeds the typical bulk mobility$^{19}$ reported for In$_2$O$_3$ as well as the reported mobility$^9$ in transparent In$_2$O$_3$ thin-film transistors. Similar phenomena, that is, nanowire mobilities exceeding bulk mobilities, have been reported in a number of materials16–18. Although the exact mechanisms for this are not completely clear, the quasi-one-dimensional nature of nanowires may play a significant role in terms of reducing low-angle carrier scattering$^{20–24}$. The use of preformed nanowires allows low-temperature device processing, which is essential for applications such as circuits fabricated on plastic substrates.

The present results build on recent NWT studies indicating that the desired semiconductor properties can be achieved and that post-treatments such as ozone and electrical stressing further enhance device performance$^{25}$. Here, we report fully transparent NWTs fabricated using all-transparent In$_2$O$_3$ and ZnO nanowire active channels, Al$_2$O$_3$ gate insulators, ITO source/drain electrodes and IZO gate electrodes. The representative In$_2$O$_3$...
NWTs on glass substrates exhibit n-type transistor characteristics with ~82% visible transparency, and $\mu_{\text{eff}}$ varies from approximately 514 to 300 cm$^2$V$^{-1}$s$^{-1}$ as the gate bias is increased from 0 V to 2 V. The representative ZnO NWTs on glass substrates exhibit ~83% visible transparency, with $\mu_{\text{eff}}$ varying from ~96 to 70 cm$^2$V$^{-1}$s$^{-1}$ over the gate bias range of 0–3 V. Fully transparent and mechanically flexible In$_2$O$_3$ NWTs with optical transmission of ~81% are also fabricated on PET plastic substrates, with $\mu_{\text{eff}}$ ≈ 120–167 cm$^2$V$^{-1}$s$^{-1}$ over the reported gate bias range. We show here that the excellent transparency and semiconducting properties of In$_2$O$_3$ and ZnO nanowires combined with Al$_2$O$_3$ as the gate insulator, and with ITO and IZO contacts, affords high-performance NWTs that are attractive candidates for future flexible transparent display applications.

**EXPERIMENTAL RESULTS AND DISCUSSION**

A cross-sectional view of the fully transparent NWT structure with an individually addressed bottom gate is shown in Fig. 1a. The structure consists of a SiO$_2$ buffer layer, a patterned IZO gate electrode, an atomic layer deposition (ALD)-derived high-$\kappa$ Al$_2$O$_3$ gate insulator, a single-crystal semiconducting In$_2$O$_3$ (ref. 26) or ZnO (ref. 27) nanowire for the active channel, and ITO for the source/drain electrodes. No further passivation layers are used, so the dielectric above the nanowire is air. Figure 1b shows a top view of an NWT device, including all transparent components. Field-emission scanning electron microscope (FE-SEM) images of single In$_2$O$_3$ and ZnO nanowires between source and drain electrodes are shown in Fig. 1c,d, respectively. The corresponding nanowire diameters and lengths ($D/L$) of single In$_2$O$_3$ or ZnO nanowires addressed between source and drain on the glass substrates are 20 nm/1.80 µm and 120 nm/1.66 µm, respectively.

Figure 2a shows the gate and drain leakage currents of a representative In$_2$O$_3$ NWT device for the bias configurations shown in the inset. Note that the drain leakage current here is the summation of the body current leakage of the In$_2$O$_3$ nanowire (~40 pA at 2 V) and the leakage current through the gate dielectric (~1 pA at 2 V). The Al$_2$O$_3$ gate dielectric exhibits excellent insulating properties, with an electrical breakdown field of >8 MV cm$^{-1}$ (ref. 28) and a dielectric constant of ~9. The thin Al$_2$O$_3$ gate dielectric allows the channel potential to be modulated at a relatively low gate voltage without significant gate leakage, resulting in a steep $S$ and a high $I_{\text{on}}/I_{\text{off}}$. Figure 2b shows linear-scale and log-scale drain current versus gate–source voltage ($I_{\text{ds}}$–$V_{\text{gs}}$) characteristics for the same In$_2$O$_3$ NWT at $V_{\text{ds}} = 0.5$ V before 2 min of ozone treatment (black squares) and after 2 min of ozone treatment (red solid line). Ozone treatments for 2 min resulted in significant device performance enhancement in terms of $S$, $V_T$ and $I_{\text{on}}$. Compared with as-fabricated devices, $S$ was reduced from 600 mV dec$^{-1}$ to 160 mV dec$^{-1}$, along with improvement in $I_{\text{on}}/I_{\text{off}}$ (~1 × 10$^6$), and a shift in $V_T$ from −1.16 V to −0.27 V. The improvement in $S$ is due to change in terms of a reduction in the interfacial trap states and in fixed surface charge states$^{23}$. Ozone treatment not only removes defects and contamination from the nanowire surface, but also changes the work function$^{29,30}$. Ozone is also expected to increase the density of oxygen vacancies near the nanowire surface. Because oxygen vacancies act as donor states$^{31,32}$, this should increase nanowire conductivity. Although the ITO and IZO microstructures and chemical bonding states

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**Figure 1** Fully transparent NWTs. a. Cross-sectional view of fully transparent NWT device structures consisting of a SiO$_2$ buffer layer (500 nm), patterned IZO gate electrode (120 nm), ALD-deposited Al$_2$O$_3$ gate insulator (18 nm), a single In$_2$O$_3$ nanowire ($D \sim 20$ nm) or ZnO nanowire ($D \sim 120$ nm) for the active channel, and ITO for the source/drain electrodes (120 nm). b. Top-view FE-SEM images of the devices. The IZO gate overlaps with the ITO source/drain electrodes to improve transistor performance with coverage all nanowire channel. Scale bar represents 100 µm. c. Top-view SEM of a single In$_2$O$_3$ nanowire region ($D/L \sim 20$ nm/1.80 µm). Scale bar represents 1.5 µm. d. Top-view SEM of a single ZnO nanowire region ($D/L \sim 120$ nm/1.66 µm). Scale bar represents 1.5 µm.
are more complex, the basic crystal structures are sufficiently similar to those of In$_2$O$_3$ and ZnO to reasonably expect that the In$_2$O$_3$ and ZnO nanowire work functions will increase similarly upon ozone treatment$^{10,32}$. Thus, the source/drain–nanowire contact should not significantly change with ozone treatment. However, because the ozone treatment plausibly reduces nanowire surface dangling bonds and carbon contamination, and forms an oxygen vacancy-rich surface, the transistor characteristics including $I_{on}/I_{off}$, $S$ and $V_T$ should be enhanced$^{34}$. Figure 2c shows $I_{ds}$–$V_{gs}$ curves for another device during four successive sweeps from $-2$ $V$ to $+2$ $V$, illustrating the excellent stability of the In$_2$O$_3$ NWs. The $I_{ds}$–$V_{gs}$ curves are comparable following bias sweeps, with consistent $I_{on}/I_{off}$, $S$ and $V_T$ values. Furthermore, for the same device, $I_{ds}$–$V_{gs}$ curves were swept from negative gate voltage ($V_{gs}(-)$) to positive gate voltage ($V_{gs}(+) ) and back to $V_{gs}(-)$ as shown in Fig. 2d. Over this bias range, the hysteresis is modest, which illustrates the excellent quality of the Al$_2$O$_3$ gate insulator and indicates negligible charge trapping and detrapping in the gate insulator. Note that the nanowire channel active regions are not passivated in these devices.

Figure 3a,c shows the $I_{ds}$–$V_{gs}$ characteristics for representative single In$_2$O$_3$ and ZnO NWs. The In$_2$O$_3$ device (the same device as in Fig. 2a,b) exhibits $S = 160$ mV dec$^{-1}$, $I_{on}/I_{off} = 1 \times 10^6$ and $V_T = -0.27$ V. The $\mu_{eff}$ of the representative In$_2$O$_3$ NWT, deduced from transconductance ($g_m = dI_d/dV_g$), varies from $\sim$514 to 300 cm$^2$ V$^{-1}$ s$^{-1}$ as the gate bias is increased from 0 V to 2 V, following a trend that is observed in NWs, TFTs and MOSFETs. The ZnO NWT device exhibits $S = 0.3$ V dec$^{-1}$, $I_{on}/I_{off} \approx 1 \times 10^6$ and $V_T = -0.07$ V, and $\mu_{eff}$ varies from $\sim$96 to 70 cm$^2$ V$^{-1}$ s$^{-1}$ over the gate bias range of 0 V to 3 V. One important device performance metric for high-speed and low-power operation is the $S = dV_{gs}/d\log I_{ds}$ (mV dec$^{-1}$). A small $S$ value is required for switching transistors, ideally approaching the theoretical limit of $\sim$60 mV dec$^{-1}$. The present $S$ values were extracted from the linear portion of the $\log I_{ds}$ versus $V_{gs}$ plot (Fig. 3a,c). The very small $S$ values in In$_2$O$_3$ and ZnO devices are comparable to other reports$^{35,36}$. The drain current versus drain–source voltage ($I_{ds}$–$V_{ds}$) characteristics of fully transparent single In$_2$O$_3$ and ZnO NWs are shown in Fig. 3b,d. These devices exhibit typical enhancement mode long-channel FET
Figure 3 Characteristics of fully transparent In$_2$O$_3$ and ZnO NWTs. a, The $I_{ds}$–$V_{gs}$ characteristic of an In$_2$O$_3$ NWT ($D/L \sim 20$ nm/1.80 μm) at $V_g = 0.5$ V. Blue, red and green data points correspond to linear-scale $I_{ds}$–$V_{gs}$, log-scale $I_{ds}$–$V_{gs}$ and $\mu_{eff}$, respectively. Arrows indicate appropriate axis. b, The $I_{ds}$–$V_{gs}$ characteristic of fully transparent In$_2$O$_3$ NWTs. $V_f$ ranges from $-0.5$ V to $2.5$ V in $0.5$ V steps, with the maximum current observed at $V_g = 2.5$ V. c, The $I_{ds}$–$V_{gs}$ characteristic of ZnO NWTs ($D/L \sim 120$ nm/1.66 μm) at $V_g = 0.5$ V. Blue, red and green data points correspond to linear-scale $I_{ds}$–$V_{gs}$, log-scale $I_{ds}$–$V_{gs}$ and $\mu_{eff}$, respectively. Arrows indicate appropriate axis. d, The $I_{ds}$–$V_{gs}$ characteristic of fully transparent ZnO NWTs. $V_f$ ranges from $0.0$ V to $3.0$ V in $0.5$ V steps, with the maximum current observed at $V_g = 3.0$ V.

behaviour. For the fully transparent In$_2$O$_3$ single NWT device, $I_{on}$ is $\sim 1 \times 10^{-5}$ μA at $V_{ds} = 1.0$ V and $V_{gs} = 2.0$ V. The $I_{on}$ of a ZnO single NWT device is $\sim 2$ μA at $V_{ds} = 1.0$ V and $V_{gs} = 2.0$ V. The performance of In$_2$O$_3$ and ZnO NWT devices is comparable to that of previously reported non-transparent In$_2$O$_3$ and ZnO NWT devices$^{35-40}$. Because the extraction procedure for $\mu_{eff}$ involves uncertainties due to the required capacitance estimation (see Methods), NWTs can be compared with planar transistors by comparing the $I_{on}$ and $g_{m}$ per unit width ($g_{m}/W$), using the nanowire diameter as the device width. The In$_2$O$_3$ nanowire on glass exhibits an $I_{on}$ density of $\sim 600$ mA mm$^{-1}$ and a $g_{m}/W$ of $\sim 212$ mS mm$^{-1}$. Both values are more than five times higher than those obtained in previous studies on transparent transistors using In$_2$O$_3$ thin films, even after adjusting for the differences in gate lengths and gate capacitance. The single-crystal nature of the nanowires and the formation of relatively high-quality interfaces are believed to play key roles in achieving this performance.

The optical transmission spectra through the In$_2$O$_3$ and ZnO NWT structures, with the substrate absorption removed, are shown in Fig. 4, showing the optical transmissions to be about 90% for both transistor types. With the substrate included, the optical transmissions are $\sim 82\%$ (In$_2$O$_3$ NWT + glass substrate) and $\sim 83\%$ (ZnO NWT + glass substrate) in the 350–1,350 nm wavelength range. The NWT array regions are $1.0 \times 0.5$ inch (the glass substrate is $1.5 \times 1.0$ inch), contain 23,000 NWT device patterns, and the substrates are entirely covered by the SiO$_2$ buffer layer and the Al$_2$O$_3$ gate insulator. The source/drain regions and the gate regions cover $\sim 45\%$ and $\sim 25\%$ of the total NWT array region, respectively. The optical absorption of the In$_2$O$_3$ and ZnO nanowires should thus be negligible because the diameter of the nanowires is small and the area covered by the nanowires is relatively small compared with the entire NWT array. The observation of $\sim 90\%$ optical transmission indicates that the transmission losses due to the various layers, including the nanowires, are negligible, and that visible light can readily penetrate the dense NWTs. The image in the inset of Fig. 4 shows a transparent In$_2$O$_3$ NWT device structure, with text on an underlying opaque layer clearly visible.

Fully transparent and flexible In$_2$O$_3$ NWT devices using a polyethylene terephthalate (PET) plastic substrate (Melinex,
DuPont) were also fabricated. A cross-sectional view of the present fully transparent and flexible In$_2$O$_3$ NWT device structure with an individually addressed bottom gate is shown in Fig. 5a. D and L for the single In$_2$O$_3$ nanowires addressed between source and drain on the plastic substrate are 20 nm and 1.79 μm, respectively. In order to suppress the leakage current due to tensile/compressive stress of the plastic substrate during photolithographic processing (up to 130 °C) and gate insulator deposition (up to 200 °C), a relatively thick Al$_2$O$_3$ gate insulator (50 nm) is used. A fully transparent and flexible In$_2$O$_3$ NWT using In$_2$O$_3$ nanowires as the active material, ITO as the bottom gate electrodes and ITO as source/drain electrodes is shown in Fig. 5b. The optical transmission through the NWT structure and substrate, with spectra shown in Fig. 5c, is ~81% in the 350–1,350 nm wavelength range. Figure 5d shows the $I_{ds}$–$V_{gs}$ characteristic of a representative single In$_2$O$_3$ NWT on the plastic substrate. Here $S = 0.9 \text{V dec}^{-1}$, $I_{on}/I_{off} \approx 1 \times 10^5$, $V_{th} = -0.6 \text{V}$, and $\mu_{eff}$ varies from ~167 to 120 cm$^2$ V$^{-1}$ s$^{-1}$ over the gate bias range of 1–3.5 V. The lower but respectable response characteristics on the plastic substrate may reflect the effects of high-temperature deposition (300 °C) and post rapid thermal annealing (500 °C for 30 s in N$_2$). Further optimization efforts are presently in progress.

Possible applications of the present transparent NWTs include pixel drivers for AMOLED displays. For AMOLEDs, increasing the

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**Figure 4** Optical transmission spectra through entire NWT structures. Blue and red lines correspond to In$_2$O$_3$ and ZnO NWTs, respectively. The inset shows the image of a transparent In$_2$O$_3$ NWT substrate having 23,000 devices, showing that text on the layer behind the substrate is clearly visible.

**Figure 5** Fully transparent and flexible In$_2$O$_3$ NWTs. a. Cross-sectional view of fully transparent and flexible NWT device structure consisting of a plastic substrate, patterned ITO gate electrode (120 nm), ALD-deposited Al$_2$O$_3$ gate insulator (50 nm), a single In$_2$O$_3$ nanowire (D/L ~ 20 nm/1.79 μm) for the active channel, and ITO for the source/drain electrodes (120 nm). b. Image of In$_2$O$_3$ NWTs on the plastic substrate, showing the optical clarity and mechanical flexibility. c. Optical transmission spectrum of region containing In$_2$O$_3$ NWTs on the plastic substrate (ITO/S/D)/In$_2$O$_3$ nanowires/Al$_2$O$_3$ /ITO(G)/plastic substrates. d. The $I_{ds}$–$V_{gs}$ characteristic of In$_2$O$_3$ NWTs at $V_g = 0.5 \text{V}$. Blue, red and green data points correspond to linear-scale $I_{ds}$–$V_{gs}$, log-scale $I_{ds}$–$V_{gs}$ and $\mu_{eff}$, respectively. Arrows indicate approximate axis.
aperture ratio is necessary to increase efficiency and reduce power consumption. For non-transparent transistors, maximizing the aperture ratio corresponds to minimizing the transistor and capacitor physical sizes. Transparent transistors would allow stacking of the drive transistors with the OLEDs, which would allow a larger transistor size (width/length) and capacitor size (single or dual capacitors). Device geometries could then be optimized to improve metrics such as peak luminescence.

Characterization Methodology

The work function of an as-grown ITO thin film was measured using an AC-2, RKI Instruments photoelectron spectrometer. The UV-Vis spectra were recorded with a Varian Cary 1E spectrophotometer. Electrical I–V measurements were performed using a Keithley 4200 semiconductor characterization system. The nanowires within a device were imaged with a Hitachi S-4800 FE-SEM following electron characterization.

Calculation of Mobility and Threshold Voltage

In contrast with planar transistors in which carrier concentration and mobility can be determined independently, for example, through Hall effect and conductivity measurements, the lack of extended lateral geometries in NWTs dictates an alternative approach for determining mobility. Following the typical approach used earlier in NWT studies, we calculated a field-effect mobility (μ_eff) using a combination of the cylinder-on-plate (COP) capacitance model 

\[
\frac{1}{C} = \frac{2\pi \varepsilon_0 \varepsilon_r}{L} \cosh^{-1}(1 + \frac{T}{V_{th}})
\]

and the relationship

\[
\mu = \frac{dL/dV_T}{C} \times \frac{1}{1/V_{ds}}
\]

obtained from the MOSFET linear region model\(^a\), where \(\varepsilon_0\) is the effective dielectric constant of Al2O3, \(L\) is the channel length of the NWTs (~1.80 μm for an In2O3 nanowire, ~1.66 μm for a ZnO nanowire), \(r\) is the radius of the NWTs (10 nm for the In2O3 nanowire, 60 nm for the ZnO nanowire), \(t_m\) ~ 18 nm is the thickness of the gate insulator, \(dL/dV_T\) is the transconductance and \(V_{ds}\) is drain voltage. In the case of flexible and transparent In2O3 NWTs, \(L = 1.79 \mu m\) and \(r = 10 \mu m\) are used. Our device geometry consists of the gate dielectric \((k_{eff} \sim 9)\) below and air \((k_{eff} \sim 1)\) above the nanowire. A previous comparison\(^b\) between electrostatic simulations and an analytic formula for capacitance (a form of the COP equation valid for \(V_{th} \gg r\)) for a comparable geometry to SiO2/air showed good agreement between the two capacitances over a range of \(t_m/r\) from 8 to 40, provided that a value of \(k_{eff} \sim 0.5\) was used. As our geometry uses a higher k dielectric constant and smaller \(t_m/r\) (~1.8), the fringing fields are more tightly confined to the gate dielectric layer. We have therefore chosen to use \(k_{eff} \sim 0.4\) which would tend to overestimate the capacitance (because the appropriate correction factor is greater than 0.5 but less than 1.0), and therefore underestimate the mobility. The conductances shown in Fig. 3a,b and Fig. 4d have been smoothed by polynomial fit to three orders with 20 points fit to the curve. In order to extract \(V_{th}\) here we used the extrapolated \(V_T = V_T(V_{ds}) = \frac{1}{\phi_m} \frac{dL}{dV_T} (V_T = 0.5 V)\), because it gives an accurate \(V_T\). The gate voltage at the maximum \(\phi_m(V_{ds})\), the drain current at the maximum \(\phi_m(V_{ds})\), and the maximum \(\phi_m(V_{ds})\) are obtained from Fig. 3a,c and Fig. 5d. These values are confirmed with \(V_T\) values obtained from the \(I_{th} = I_{ds}\) curve at \(V_T = 0.1 V\).

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\(^{26}\)F-120 ALCD system using trimethyl aluminium (Al(CH3)3) (TMA) and water as precursors. Following Al2O3 deposition, the substrates were annealed at 500 °C for 30 s under N2 to improve the film quality. Next, a suspension of In2O3 or ZnO nanowires in VLSI-grade 2-propanol solution was disbursed on the gate patterned substrates. Single-crystal semiconducting In2O3 nanowires were synthesized by a pulsed laser ablation process\(^25\), with average diameter and length of 20 nm and 5 μm, respectively. Powdered ZnO nanowires synthesized by thermal evaporation and condensation were purchased from Nanolab. The average diameter and length were 120 nm and 5 μm, respectively, and microstructural characterization indicated that they were highly crystalline\(^27\).

Finally, ITO source/drain electrodes were deposited by IAD at room temperature and patterned by photolithography. Following source/drain electrode patterning, the NWTs were subjected to an ozone treatment (UV-Ozone cleaner, UVO 42-220, Jelight) for 2 min to achieve optimum transistor performance in terms of \(t_m, I_{th}, t_{ds}, \) and \(r\). The ozone environment was obtained by setting the oxygen content to 50 p.p.m., the ultraviolet (UV) wavelength to 184.9 nm and UV lamp power to 28 mW cm−2 at 254 nm. Note that the devices were shielded from UV light. Fully transparent and flexible In2O3 NWT devices using PET (Melinex, DuPont) were also fabricated with a PET/ITO/Al2O3/ITO/In2O3/ITO nanowire/ITO/S/D structure (Fig. 5a).

The 50-nm-thick Al2O3 layer was deposited at 200 °C. The ITO for the gate and source/drain electrodes was deposited using IAD. The nanowire lengths of gate transistors between source and drain were obtained from the FE-SEM image, and account for the angle between the nanowire and the electrode edges.

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Author contributions
All authors contributed equally to this work and all discussed the results and commented on the manuscript.

Competing financial interests
The authors declare no competing financial interests.

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