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A ferroelectric semiconductor field-effect transistor

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Ferroelectric field-effect transistors employ a ferroelectric material as a gate insulator, the polarization state of which can be detected using the channel conductance of the device. As a result, the devices are potentially of use in non-volatile memory technology, but they suffer from short retention times, which limits their wider application. Here, we report a ferroelectric semiconductor field-effect transistor in which a two-dimensional ferroelectric semiconductor, indium selenide (α-In_2Se_3), is used as the channel material in the device. α-In_2Se_3 was chosen due to its appropriate bandgap, room-temperature ferroelectricity, ability to maintain ferroelectricity down to a few atomic layers and its potential for large-area growth. A passivation method based on the atomic layer deposition of aluminium oxide (Al_2O_3) was developed to protect and enhance the performance of the transistors. With 15-nm-thick hafnium oxide (HfO_2) as a scaled gate dielectric, the resulting devices offer high performance with a large memory window, a high on/off ratio of over 10^8, a maximum on current of 862 μA μm^{-1} and a low supply voltage.

Ferroelectric materials exhibit a spontaneous polarization in the absence of an external electric field. This polarization can be reoriented by ion displacement in the crystal, and polarization switching can be triggered by an external electrical field such that ferroelectric materials can have two electrically controllable non-volatile states[1]. As a result, ferroelectric random access memory (FeRAM) has long been studied as a non-volatile memory technology[2–14]. FeRAM uses a ferroelectric capacitor to build a one-transistor–one-capacitor (1T1C) cell. However, the reading process in the capacitor-type FeRAM is destructive and requires a rewrite after each reading operation. This structure has been commercialized but has a limited market share.

Ferroelectric field-effect transistors (Fe-FETs; Fig. 1a) can be used to build a type of one-transistor (1T) non-volatile memory. In a Fe-FET, a ferroelectric insulator is employed as the gate insulator in a metal–oxide–semiconductor field-effect transistor (MOSFET). The channel conductance is used to detect the polarization state in the ferroelectric gate insulator so that the data reading operation in Fe-FETs is non-destructive. Fe-FET is a promising memory technology due to the fast switching speed in ferroelectric materials (nanoseconds or less[4,9,11,15,16]), its non-destructive readout, its non-volatile memory state and its simple structure for high-density integration.

Despite the fact that this Fe-FET structure was first proposed in 1957 (ref. [17]), it has not yet been commercialized because of its short retention time. The two major causes of this are the depolarization field and the gate leakage current. The depolarization field is the result of the potential drop across the interfacial dielectric and the band bending of the semiconductor, which leads to charge trapping at the ferroelectric insulator/semiconductor interface[2,6,14,18]. Therefore, charge trapping and gate leakage current can cause charge accumulation at the ferroelectric insulator/semiconductor interface, which leads to threshold voltage (V_T) drift and destruction of the memory state.

In this Article, we report a ferroelectric semiconductor field-effect transistor (FeS-FET), which has the potential to address the issues of Fe-FETs in non-volatile memory applications. In our FeS-FET, a ferroelectric semiconductor is used as the channel material while the gate insulator is the dielectric (Fig. 1b). The two non-volatile polarization states in the FeS-FETs exist in the ferroelectric semiconductor. Therefore, a high-quality amorphous gate insulator can be used instead of the common polycrystalline ferroelectric insulator found in Fe-FETs. Furthermore, the mobile charges in the semiconductor can screen the depolarization field across the semiconductor. Thus, the charge trapping and leakage current through the ferroelectric insulator found in conventional Fe-FETs can potentially be eliminated. As a result, our approach could offer performance improvements over conventional Fe-FETs in non-volatile memory applications.

Our FeS-FETs use the two-dimensional (2D) ferroelectric semiconductor α-In_2Se_3 as the channel material. α-In_2Se_3 was selected[19–25] because of its appropriate bandgap of ~1.39 eV, its room-temperature ferroelectricity[23] with a Curie temperature above 200 °C, the ability to maintain ferroelectricity down to a few atomic layers[20,22] and the feasibility for large-area growth[26,27]. When using a scaled HfO_2 gate insulator, the fabricated FeS-FETs exhibit high performance with a large memory window, a high on/off ratio of over 10^8, a maximum on current of 862 μA μm^{-1} and a low supply voltage.

FeS-FET device physics

The working mechanism of a FeS-FET is fundamentally different from a traditional Fe-FET. In a Fe-FET, only the polarization bound charges at the gate insulator/semiconductor interface can affect the electrostatics. The ferroelectric polarization switching can tune the threshold voltage (V_T) of the device by reversing the polarity of the polarization bound charge, and so a counterclockwise I_D–V_{GS} hysteresis loop can be achieved. However, in a FeS-FET, the polarization charges accumulate at both the bottom surface (BS) and top surface (TS) of the ferroelectric semiconductor, as shown in Fig. 1c. As a result, the drain current (I_D) of the FeS-FET is determined by both the bottom and top surfaces of the semiconductor. As shown

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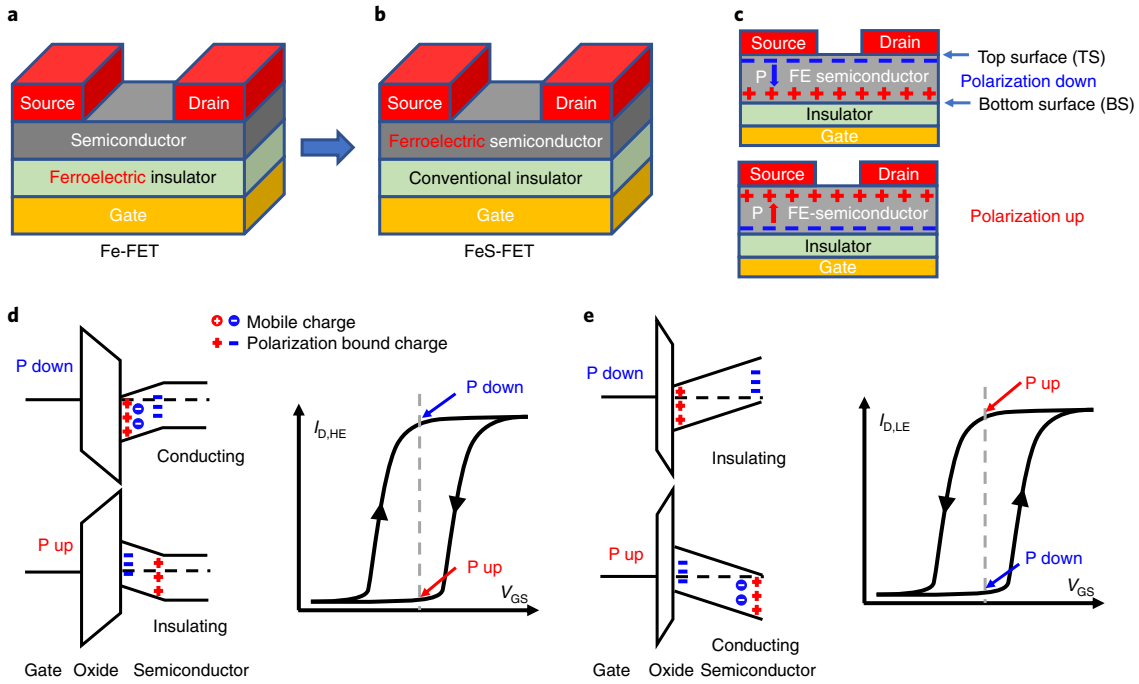

Fig. 1 | Schematic diagram and proposal for a ferroelectric semiconductor field-effect transistor (FeS-FET). a, Schematic of a Fe-FET. **b**, Schematic of a FeS-FET. In the FeS-FET, the conventional semiconductor channel is replaced by a ferroelectric semiconductor, while the gate insulator is still conventional dielectric. **c**, Polarization bound charge distribution in a FeS-FET in polarization down (after negative gate bias) and polarization up (after positive gate bias) states. **d**, Band diagram of a FeS-FET with high effective oxide thickness (EOT) in polarization (P) up and polarization down states and the corresponding I_D–V_{GS} characteristics. A clockwise hysteresis loop is achieved due to partial polarization switching. **e**, Band diagram of a FeS-FET with low EOT in polarization up and polarization down states and the corresponding I_D–V_{GS} characteristics. A counterclockwise hysteresis loop is achieved due to full polarization switching.

in Fig. 1c, if the FeS-FET is in the polarization down state, negative bound charges accumulate at the TS while positive bound charges accumulate at the BS, and vice versa for the polarization up state.

The coupled ferroelectric and semiconducting nature of α-In_2Se_3 is critical to analyse and understand the device operation of the FeS-FET. Due to its semiconducting nature, the channel can exhibit mobile charges depending on the relative positions of the conduction/valence band edges and the Fermi level, E_F. The presence of such mobile charges can allow a non-uniform distribution of the electric field (E field) across the different layers of α-In_2Se_3. The amount of E field in the channel, in turn, determines the extent of polarization switching in the α-In_2Se_3 layers. Such complex interactions in the proposed device lead to unique characteristics, which can be broadly categorized into clockwise hysteretic and counterclockwise hysteretic. The direction of hysteresis is dependent on E field in the channel, determined by the gate dielectric thickness and the applied gate voltage, V_{GS}. To explain this in more detail, two different EOTs are considered: high EOT and low EOT.

For simplicity, the band diagram of the FeS-FET is first discussed without considering the band bending induced by its semiconducting nature. The major difference between a high-EOT device and a low-EOT device is the strength of the electric field across the semiconductor. For example, in the experiments in this work, the maximum voltage applied for the high-EOT device with 90 nm SiO_2 gate insulator is 50 V (EOT ≈ 90 nm, max voltage/EOT ≈ 0.56 V nm^{-1}). The maximum voltage applied for the low-EOT device with 15 nm HfO_2 gate insulator is 5 V (EOT ≈ 3 nm, max voltage/EOT ≈ 1.7 V nm^{-1}). The huge difference on the displacement field (D field) is critical to the I–V characteristics of the FeS-FET. For high-EOT devices, the electric field across the semiconductor is not strong enough to penetrate to the top surface of the ferroelectric semiconductor, as shown in Fig. 1d. Accordingly, only partial switching happens near the oxide/semiconductor interface. For low-EOT devices, the electric field is sufficiently strong to trigger full polarization switching in the ferroelectric semiconductor, as shown in Fig. 1e. The high and low EOT conditions are applied for the following discussion. Numerical simulation confirmed the validity of all these conditions and will be discussed later.

In the high EOT condition (shown in the band diagram in Fig. 1d) in the polarization down state, mobile charges can accumulate at the BS because of band bending, so the channel resistance is low. Similarly, in the polarization up state, the mobile charge density at the BS is low, resulting in high channel resistance. A negative voltage below the coercive voltage (V_{C-}) leads to the polarization down state and a positive voltage above the coercive voltage (V_{C+}) leads to the polarization up state. Therefore, the curve of drain current in the high EOT condition ($I_{D,HE}$) versus V_{GS} has a clockwise hysteresis loop. In low EOT conditions, the electric field across the semiconductor is sufficiently large that it can penetrate fully into the semiconductor. In this case, the TS can become conducting due to full polarization switching. As shown in the band diagram in Fig. 1e, in the polarization down state, mobile charges do not exist at the TS, so the channel resistance is high. Similarly, in the polarization up state, mobile charges can accumulate at the TS, resulting in low channel resistance. Note that the BS is much easier to control with the gate voltage, so by adjusting the gate voltage the mobile charge at the BS can be fully depleted. Therefore, the curve of drain current in low EOT conditions ($I_{D,LE}$) versus V_{GS} has a counterclockwise hysteresis loop. Both directions of hysteresis loop can be realized depending on the EOT of the dielectric. Note that the above discussion is a simplified picture that does not consider the band bending induced by mobile carriers. Sophisticated and complete theory and

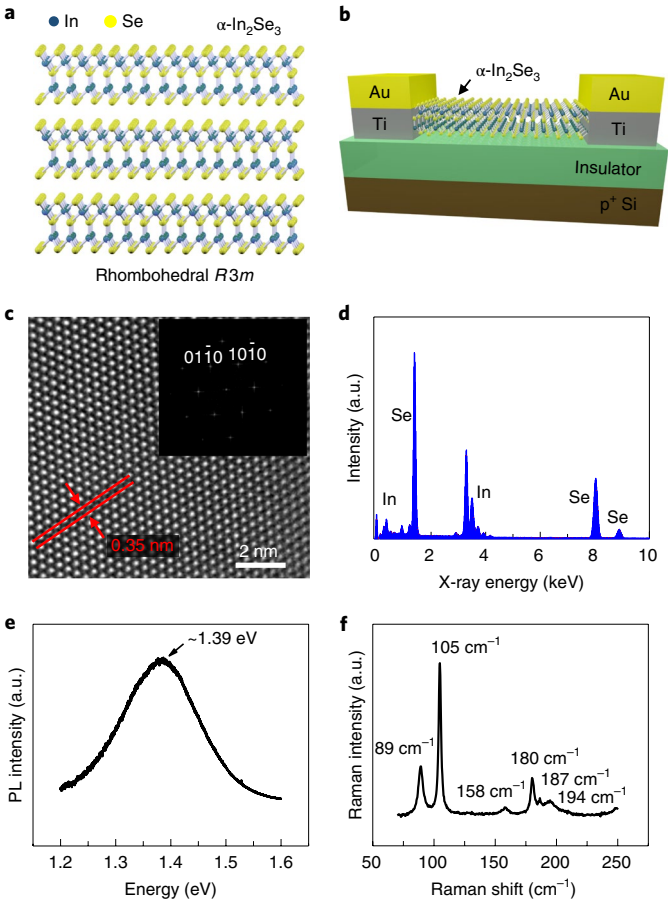

Fig. 2 | Material properties of the ferroelectric semiconductor α-In_2Se_3. **a**, Crystal structure of the ferroelectric semiconductor α-In_2Se_3. **b**, Schematic of the experimental α-In_2Se_3 FeS-FET, which consists of a heavily doped silicon substrate as the back-gate electrode, 15 nm HfO_2 or 90 nm SiO_2 as the gate dielectric, 2D thin-film α-In_2Se_3 as the channel ferroelectric semiconductor and 30 nm Ti/50 nm Au as source/drain electrodes. **c**, HAADF-STEM image and the corresponding SAED image (inset) of thin α-In_2Se_3 film. **d**, EDS spectrum of the thin α-In_2Se_3 film. The measured at% values for In and Se are 37 and 63, respectively. **e**,**f**, Photoluminescence (PL) spectrum (**e**) and Raman spectrum (**f**) of bulk α-In_2Se_3, showing a bandgap of ~1.39 eV without considering the 2D exciton binding energy. Raman and photoluminescence spectrums are measured at room temperature and confirm the semiconducting properties of the α-In_2Se_3.

numerical simulations considering both ferroelectric and semiconducting natures have been developed and provide the same conclusion; these will be discussed later. Experimentally, α-In_2Se_3 FeS-FETs with 90 nm SiO_2 as the gate insulator, as in the high EOT condition, show a clockwise hysteresis loop, while α-In_2Se_3 FeS-FETs with 15 nm HfO_2, as in the low EOT condition, show a counterclockwise hysteresis loop.

Experiments on α-In_2Se_3 FeS-FETs

α-In_2Se_3 is a recently discovered 2D ferroelectric semiconductor, which is used in this work to demonstrate the FeS-FET operation. α-In_2Se_3 bulk crystals were grown by the melt method with a layered non-centrosymmetric rhombohedral *R*3*m* structure[19], as shown in Fig. 2a. The α-In_2Se_3 FeS-FET (Fig. 2b) consists of a heavily p-doped Si substrate as the back-gate electrode, 15 nm HfO_2 or 90 nm SiO_2 as the gate insulator, 2D α-In_2Se_3 as the ferroelectric semiconductor channel and 30 nm Ti/50 nm Au as source/drain electrodes. An optimized 10 nm Al_2O_3 capping layer was grown by atomic layer deposition (ALD) at 175 °C on top of the α-In_2Se_3 channel, which provided a significant performance enhancement when compared with α-In_2Se_3 FeS-FETs without passivation. A high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of a thin α-In_2Se_3 flake is shown in Fig. 2c. The distinct arrangement of atoms can be clearly identified, with the fringe space of (100) planes measured to be 0.35 nm, confirming an ideal hexagonal lattice structure for the α-In_2Se_3. The corresponding selected-area electron diffraction (SAED) image (Fig. 3c, inset) shows six-fold symmetry with a perfect hexagonal crystal structure, indicating that the α-In_2Se_3 flake is highly single-crystallized. Energy dispersive spectroscopy (EDS) results (Fig. 2d) confirm the atomic percentage (at%) ratio between In and Se of ~2:3. Figure 2e presents a photoluminescence spectrum of a bulk α-In_2Se_3 crystal, measured from 1.2 eV to 1.6 eV, indicating a direct bandgap of ~1.39 eV. Figure 2f shows a Raman spectrum measured from a bulk α-In_2Se_3 crystal, showing peak positions consistent with literature reports[24].

A strong piezoelectric response is observed from a 78.7-nm-thick α-In_2Se_3 flake, which is shown in Fig. 3a–c by piezoresponse force microscopy (PFM). To extract the piezoelectric coefficient, different a.c. voltages were applied on the sample from a conductive atomic force microscopy (AFM) tip, showing a linear relationship between the mechanical deformation (PFM amplitude) and the electric field. The effective piezoelectric coefficient (d_{33}) of the α-In_2Se_3 flake is 32 pm V^{-1} (Supplementary Section 1). From the background noise shown in Fig. 3c, it is clear that the mechanical deformation in the PFM measurement is dominated by the intrinsic ferroelectric polarization. Figure 3d,g shows two different measurement schematics on α-In_2Se_3, the metal–semiconductor–metal (MSM) structure and the metal–oxide–semiconductor (MOS) structure. Figure 3e,f shows the PFM phase and PFM amplitude versus voltage hysteresis loop of a 15.3-nm-thick α-In_2Se_3 flake on conductive Ni, showing clear ferroelectric polarization switching under an external electric field. The photoluminescence measurement of the bandgap and PFM measurement of polarization switching together suggest the α-In_2Se_3 used in this work is a ferroelectric semiconductor. Note that PFM hysteresis is just a necessary condition but is not a sufficient condition for ferroelectric materials. As mobile charges exist in a semiconductor, such charges may screen and prevent the electric field penetrating into the body of the semiconductor, so the ferroelectric polarization switching may be different in a MOS structure. Therefore, it is important to test whether the polarization in α-In_2Se_3 can be switched by an external electric field in a MOS structure. Figure 3h,i shows the PFM phase and PFM amplitude versus voltage hysteresis loop of 6 nm Al_2O_3/16.3 nm α-In_2Se_3 on Ni. The ferroelectric hysteresis loop suggests that α-In_2Se_3 has switchable polarization in a MOS device structure. Thus, it is viable to apply α-In_2Se_3 as the channel for a FeS-FET. The raw data for the PFM measurements are provided in Supplementary Section 1.

Figure 4a presents a top-view false-colour scanning electron microscope (SEM) image of a fabricated α-In_2Se_3 FeS-FET with ALD passivation, capturing the α-In_2Se_3 thin film and Ti/Au electrodes. The electrical performance of the unpassivated device is described in Supplementary Section 2. The α-In_2Se_3 FeS-FET without ALD passivation shows a clear clockwise hysteresis loop and a large memory window over 70 V. A high on/off ratio of over 10^7 at V_{DS} = 0.5 V between on and off states is also achieved. It was found that the performance of the α-In_2Se_3 FeS-FET could be further enhanced by ALD Al_2O_3 passivation, as shown in Fig. 4a. Figure 4b shows the I_D–V_{GS} characteristics of a representative α-In_2Se_3 FeS-FET with ALD passivation and 90 nm SiO_2 as gate insulator. Low-temperature ALD-grown Al_2O_3 not only offers passivation on the α-In_2Se_3 surface, but also provides an electron doping effect due to the positive fixed charges[28,29]. The transfer curve was measured by a double gate voltage sweep at different V_{DS} for a device with a channel length (L_{ch}) of 1 μm and channel thickness (T_{ch}) of 52.2 nm. The

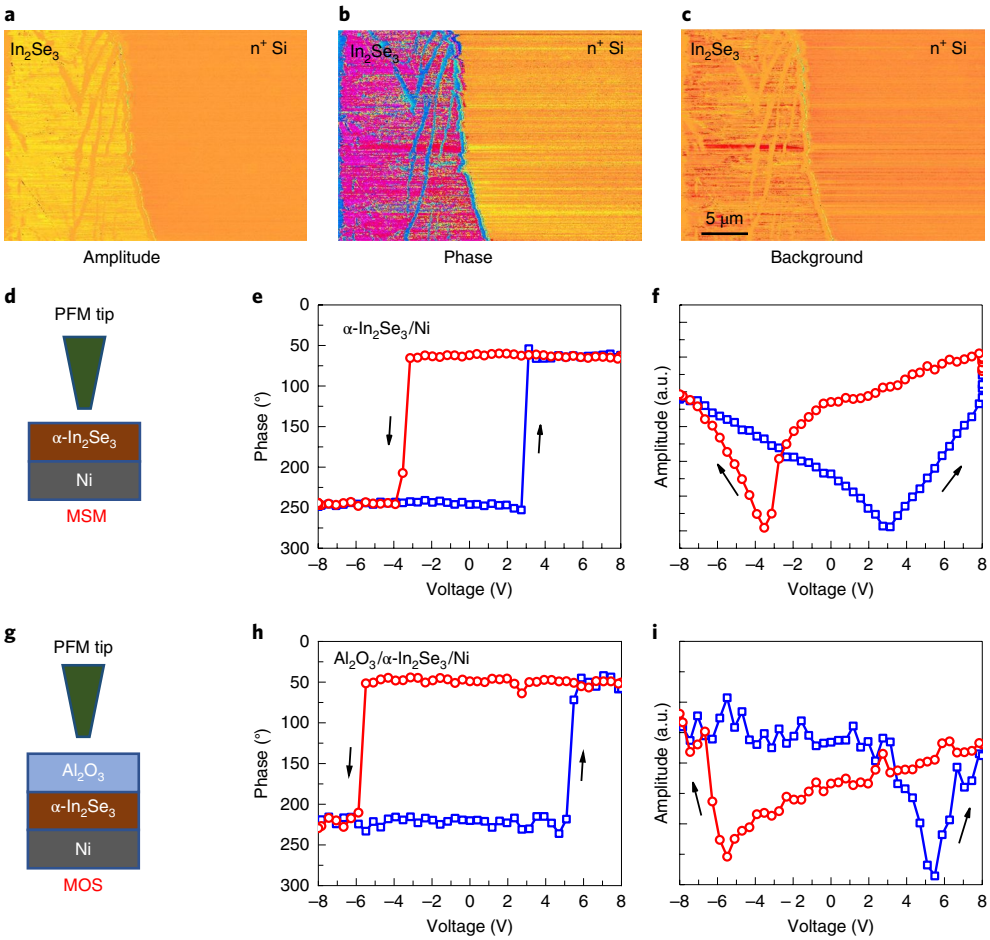

Fig. 3 | PFM measurement on an α-In_2Se_3 thin film. a–**c**, PFM amplitude (**a**), PFM phase (**b**) and PFM background (**c**) images of a 78.7-nm-thick α-In_2Se_3 flake on a heavily doped silicon substrate. **d**, Schematic of PFM measurements using the MSM structure. **e**,**f**, PFM phase (**e**) and PFM amplitude (**f**) versus voltage hysteresis loop of 15.3 nm α-In_2Se_3 on Ni, showing clear ferroelectric polarization switching under an external electric field. **g**, Schematic of PFM measurements using the MOS structure. **h**,**i**, PFM phase (**h**) and PFM amplitude (**i**) versus voltage hysteresis loop of 6 nm Al_2O_3/16.3 nm α-In_2Se_3 on Ni. The ferroelectric hysteresis loop suggests that α-In_2Se_3 has switchable polarization in the MOS device structure.

transfer curve shows a clear clockwise hysteresis loop. A high on/off ratio of over 10^8 at $V_{DS}=1$ V is also achieved, suggesting a high-quality oxide/semiconductor interface. The minimum subthreshold slope (SS) at $V_{DS}=0.05$ V achieved in this device is 650 mV dec^{-1}, indicating an estimated interface trap density (D_{it}) of 2.6×10^{12} cm^{-2} without considering the semiconductor capacitance. Figure 4c presents the I_D–V_{DS} characteristics of the same α-In_2Se_3 FeS-FET as used for Fig. 4b. A maximum drain current of 671 μA μm^{-1} is achieved. Considering the long channel length ($L_{ch}=1$ μm) used here, the α-In_2Se_3 FeS-FETs can have a much higher on current at a shorter channel length, with the potential for high-speed applications. Figure 4d shows the g_m–V_{GS} characteristics at $V_{DS}=0.05$ V for the same device as in Fig. 4b. Maximum values of transconductance (g_m) at $V_{DS}=0.05$ V of 0.60 μS μm^{-1} and 0.94 μS μm^{-1} are obtained for the forward and reverse gate voltage sweeps, respectively. The extrinsic field-effect mobility (μ_{FE}) calculated using the maximum g_m in forward sweep is found to be 312 cm^2 V^{-1} s^{-1} and in reverse sweep 488 cm^2 V^{-1} s^{-1} without extracting the relative large contact resistance due to the Schottky contacts. Note that the extrinsic field-effect mobility is different from the intrinsic mobility of α-In_2Se_3. Here, it only serves as a reference for the transport properties of the devices (a discussion about the accuracy of field-effect mobility estimation is provided in Supplementary Section 5). The performances of the α-In_2Se_3 FeS-FETs are significantly improved by the 10 nm Al_2O_3 ALD passivation when comparing to the unpassivated devices shown in Supplementary Section 2 ($\mu_{FE}=19.3$ cm^2 V^{-1} s^{-1} in forward sweep and $\mu_{FE}=68.1$ cm^2 V^{-1} s^{-1} in reverse sweep). The α-In_2Se_3 FeS-FET with 90 nm SiO_2 gate insulator was also characterized at very low temperatures down to 80 mK. The existence of a hysteresis window similar to the one at room temperature indicates that the clockwise I_D–V_{GS} hysteresis loop is caused by ferroelectric polarization switching instead of charge trapping[30,31]. A detailed discussion is provided in Supplementary Section 3. Note that the clockwise hysteresis properties in the FeS-FETs can be integrated together with Fe-FETs as a Fe^2-FET, where both insulator and semiconductor are ferroelectric. In the Fe^2-FET, a deep steep-slope subthreshold and hysteresis-free perfomance can be achieved at the same time (see Supplementary Section 8 for details) if all the device parameters are optimized.

The clockwise hysteresis loop in α-In_2Se_3 FeS-FETs indicates that the BS is the dominating conducting channel (Fig. 1d). The counterclockwise hysteresis loop can be achieved by careful design of the device structure. By scaling the gate oxide thickness and applying high-k dielectrics (HfO_2), a much higher D field can be applied inside the gate oxide, where k is the dielectric constant. By applying the high D field, the I_D–V_{GS} curve of the α-In_2Se_3 FeS-FET with 15 nm HfO_2 as gate dielectric becomes counterclockwise (and also with a high on/off ratio > 10^8), as shown in Fig. 4e. The device has a channel

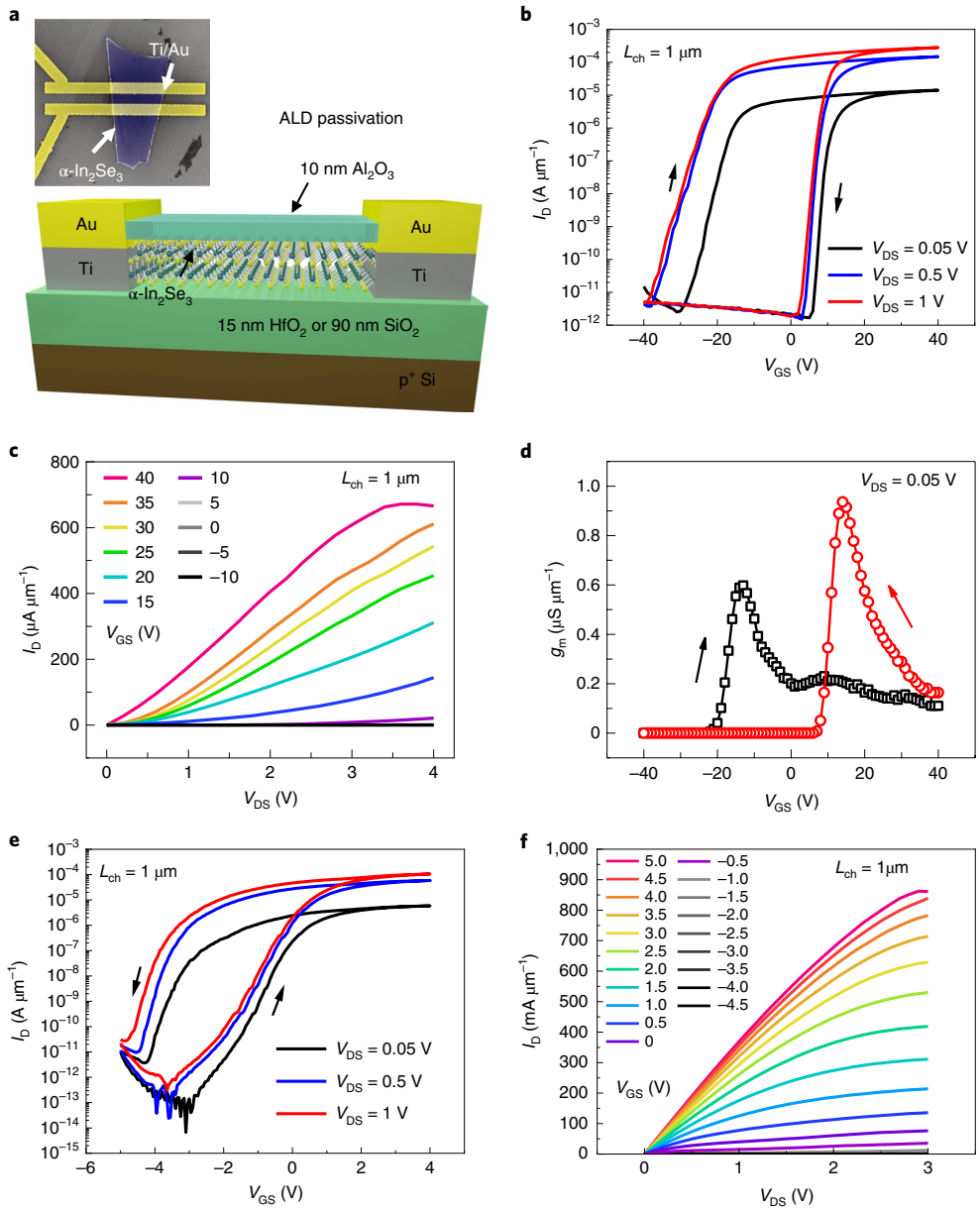

Fig. 4 | Switching characteristics of α-In_2Se_3 FeS-FETs. a, Schematic of the experimental α-In_2Se_3 FeS-FET with ALD passivation and a false-colour top-view SEM image of a fabricated α-In_2Se_3 FeS-FET. **b**–**d**, I_D–V_{GS} (**b**), I_D–V_{DS} (**c**) and g_m–V_{GS} (**d**) characteristics at room temperature of a representative α-In_2Se_3 FeS-FET with 90 nm SiO_2 as gate dielectric and ALD passivation. The device has a channel length of 1 μm and channel thickness of 52.2 nm. The device exhibits a large memory window, maximum drain current of 671 μA μm^{-1}, on/off ratio > 10^8, high electron mobility with μ_{FE} = 312 cm^2 V^{-1} s^{-1} measured in forward sweep and μ_{FE} = 488 cm^2 V^{-1} s^{-1} measured in reverse sweep. **e**, I_D–V_{GS} characteristics at room temperature of a representative α-In_2Se_3 FeS-FET with 15 nm HfO_2 as gate insulator and ALD passivation. The device has a channel length of 1 μm and channel thickness of 79 nm. **f**, I_D–V_{DS} characteristics of an α-In_2Se_3 FeS-FET device with 15 nm HfO_2 as gate dielectric and ALD passivation. The device has a channel length of 1 μm and a channel thickness of 92.1 nm. The device with 15 nm HfO_2 as gate dielectric and ALD passivation exhibits a significantly reduced supply voltage, high on/off ratio > 10^8 and maximum drain current of 862 μA μm^{-1}.

length of 1 μm and a channel thickness of 79 nm. The enhanced electric field inside α-In_2Se_3 can penetrate through to the top surface so that full polarization switching happens instead of partial switching as in the 90 nm SiO_2 case. As a result, TS conduction can lead to a counterclockwise hysteresis loop, as shown in Fig. 1e. As the charge trapping process cannot lead to a counterclockwise hysteresis loop, this result serves as conclusive proof of the existence of ferroelectricity and polarization switching. Figure 4f shows the I_D–V_{DS} characteristics of an α-In_2Se_3 FeS-FET. The device has a channel length of 1 μm and channel thickness of 92.1 nm. A maximum drain current of 862 μA μm^{-1} is achieved. The devices with 15 nm HfO_2 as gate dielectric and ALD passivation exhibit a significantly reduced supply voltage compared to the devices with 90 nm SiO_2 as the gate insulator, suggesting the potential of α-In_2Se_3 FeS-FETs for low-power non-volatile memory application.

Simulation of α-In_2Se_3 FeS-FETs

Theoretical analysis of the FeS-FETs and device-level simulations were conducted to investigate the clockwise and counterclockwise hysteresis in the I–V characteristics of FeS-FETs. More specifically,

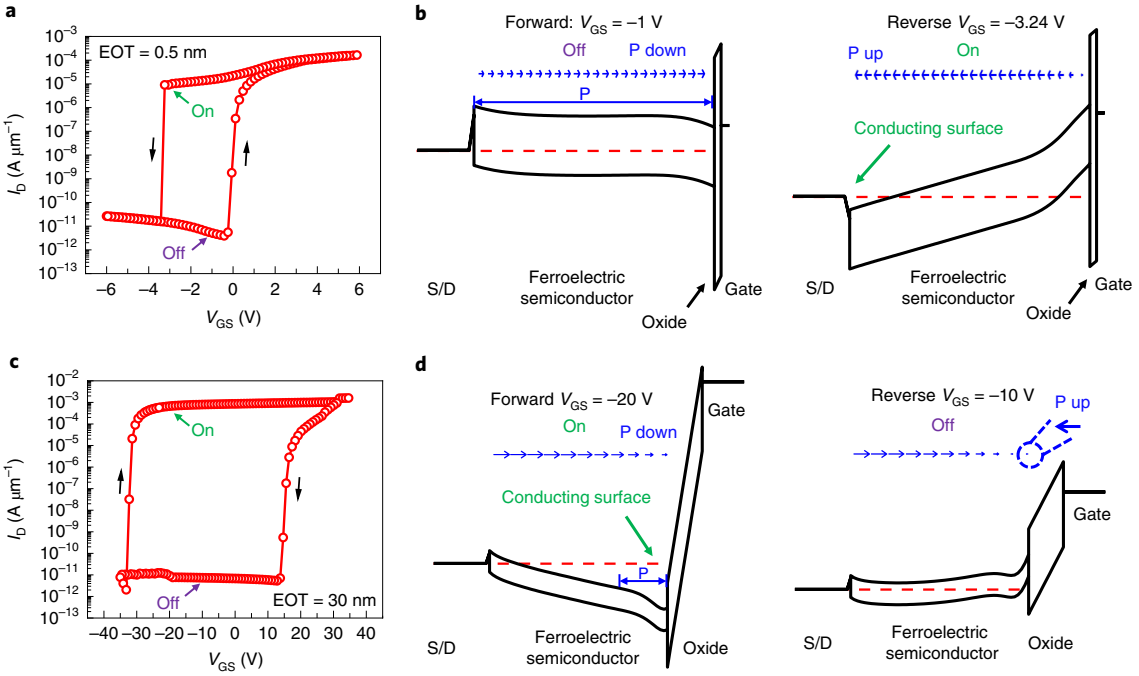

Fig. 5 | Simulation of α-In_2Se_3 FeS-FETs. a, Simulation of I_D–V_{GS} characteristics of an α-In_2Se_3 FeS-FET with EOT = 0.5 nm. **b**, Band diagram at V_{GS} = –1 V in a forward gate voltage sweep, where the device is in the off state, and the band diagram at V_{GS} = –3.24 V in a reverse gate voltage sweep, where the device is in the on state. The counterclockwise hysteresis loop originates from TS conduction because of full polarization switching. S/D, source/drain. **c**, Simulation of the I_D–V_{GS} characteristics of an α-In_2Se_3 FeS-FET with EOT = 30 nm. **d**, Band diagram at V_{GS} = –20 V in a forward gate voltage sweep, where the device is in the on state, and the band diagram at V_{GS} = –10 V in a reverse gate voltage sweep, where the device is in the off state. The polarization vector near the gate insulator/semiconductor interface is enlarged for better illustration. Note that the polarization direction near the interface is opposite the ones in the bulk and surface. The clockwise hysteresis loop originates from the bottom surface conduction because of partial polarization switching. S/D, source/drain. A detailed analysis via band diagrams at different gate voltages during a bidirectional gate voltage sweep for both low EOT and high EOT is discussed in Supplementary Section 6.

physics-based self-consistent simulations of the FeS-FET devices were performed by coupling Poisson's equation, the Ginzburg–Landau equation and the 2D charge equation. A van der Waals gap was assumed between the source/drain contacts and the semiconductor channel because of the 2D layered nature of α-In_2Se_3. Detailed simulation methods are provided in Supplementary Section 6. As shown in the simulation results in Fig. 5a,c, a clockwise I_D–V_{GS} hysteresis loop is achieved for the high-EOT (30 nm) device and a counterclockwise hysteresis loop for the low-EOT (0.5 nm) device. For the low-EOT device, at V_{GS} = –1 V in the forward gate voltage sweep, the device is in the polarization down state. As shown in the band diagram in Fig. 5b, the mobile charge density in the semiconductor is low, so the device is in the off state. At V_{GS} = –3.24 V in the reverse gate voltage sweep, the device is in the polarization up state. This is full polarization switching, as shown in the polarization vector map. For the high-EOT device, at V_{GS} = –20 V in the forward gate voltage sweep, the device is in the polarization down state. The device is in the on state due to BS inversion. At V_{GS} = –10 V in the reverse gate voltage sweep, the ferroelectric semiconductor is in the polarization up state only near the gate oxide/semiconductor interface, indicating that this is a partial polarization switching. As a result, the device is in the off state without TS conduction (Fig. 5d). A detailed analysis with band diagrams at different gate voltages during a bidirectional gate voltage sweep for both low EOT and high EOT is discussed in Supplementary Section 6. The simulation results considering both the ferroelectric and semiconducting nature of the α-In_2Se_3 confirm the validity of the simple picture discussed in Fig. 1.

Conclusions

We have reported a FeS-FET in which the 2D ferroelectric semiconductor α-In_2Se_3 is used as channel material. An ALD Al_2O_3 passivation method was developed to protect and enhance the performance of the α-In_2Se_3 FeS-FETs. The fabricated FeS-FETs exhibit high performance with a large memory window, a high on/off ratio of over 10^8, a maximum on current of 862 μA μm^{-1} and a low supply voltage. Our FeS-FETs have the potential to surpass the capabilities of existing Fe-FETs for non-volatile memory applications.

Methods

Device fabrication. α-In_2Se_3 was transferred onto 15 nm HfO_2 or 90 nm SiO_2 on a Si substrate using Scotch tape exfoliation. The p^+ Si wafers with 90 nm thermally grown SiO_2 were purchased from WaferPro. A 15 nm HfO_2 layer was deposited by ALD using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as precursors at 200 °C. 30 nm Ti and 50 nm Au were deposited by electron-beam evaporation and followed by a liftoff process for α-In_2Se_3 back-gate transistors. An optimized 10 nm Al_2O_3 layer was finally deposited by ALD using $Al(CH_3)_3$ (TMA) and H_2O as precursors at 175 °C.

Material characterization. Material characterizations on α-In_2Se_3 crystals were carried out to investigate α-In_2Se_3 as a single-crystal semiconducting and ferroelectric material, including STEM, photoluminescence, Raman spectroscopy and PFM. HAADF-STEM analysis was performed with an FEI Talos F200X equipped with a probe corrector. This microscope was operated with an acceleration voltage of 200 kV. Raman and photoluminescence measurements were carried out on a Horiba LabRAM HR800 Raman spectrometer. Dual a.c. resonance tracking PFM (DART-PFM) was carried out on Asylum Cypher ES AFM. Single-phase PFM characterization was carried out on a Keysight 5500 system in contact mode and the conductive AFM tip had an averaged spring constant of ~5 N m^{-1}.

Device characterization. The thickness of the α-In_2Se_3 was measured using a Veeco Dimension 3100 AFM system. SEM and EDS analyses were done using a Hitachi S-4800 FE-SEM system and an Oxford X-Max silicon drift detector. D.c. electrical characterization was performed with a Keysight B1500 system in a dark environment. Electrical data were collected with a Cascade Summit probe station at room temperature. Low-temperature Hall measurements at 80 mK were performed in an Oxford Triton 300 dilution fridge.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request. Raw data for the PFM measurements are provided in the Supplementary Information.

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Author contributions

P.D.Y. and M.S. conceived the idea and proposed the FeS-FET concept. M.S. carried out device fabrication, electrical measurements and analysis. A.K.S. and S.K.G. performed the numerical simulation. S.G. and W.W. performed PFM measurements. J.Q., J.J. and H.W. conducted the TEM and EDS measurements. Y.D. and M.S. carried out SEM imaging and EDS analysis. G.Q. obtained the Raman and photoluminescence measurements. G.Q. and C.N. performed the low-temperature *I*–*V* and Hall measurements. M.S. and P.D.Y. co-wrote the manuscript and all authors commented on it.

Competing interests

The authors declare no competing interests.

Additional information

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