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Scaled indium oxide transistors fabricated using atomic layer deposition

Mengwei Si[1,2], Zehao Lin[1], Zhizhong Chen[1], Xing Sun[3], Haiyan Wang[3] and Peide D. Ye[1]✉

To continue to improve integrated circuit performance and functionality, scaled transistors with short channel lengths and low thickness are needed. But further scaling of silicon-based devices and the development of alternative semiconductor channel materials that are compatible with current fabrication processes are challenging. Here we report atomic-layer-deposited indium oxide transistors with channel lengths down to 8.0 nm, channel thicknesses down to 0.50 nm and equivalent dielectric oxide thickness down to 0.84 nm. Due to the scaled device dimensions and low contact resistance, the transistors exhibit high on-state currents of 3.1 A mm^{-1} at a drain voltage of 0.5 V and transconductance of 1.5 S mm^{-1} at a drain voltage of 1.0 V. Our approach provides a promising alternative channel material for scaled transistors with back-end-of-line-processing compatibility.

The scaling of complementary metal–oxide–semiconductor (CMOS) technology has been the driving force in the advancement of modern integrated circuits over the past few decades. Enhancing gate electrostatic control to improve immunity to short-channel effects (SCEs) has, in particular, been a key strategy in the development of aggressively scaled transistor technology. This includes the development of high-κ/metal gate technology for equivalent oxide thickness (EOT) scaling, as well as ultrathin body, fin and stacked nanosheet channel transistors; stacked nanosheet transistors are currently being adopted by the semiconductor industry (following the fin field-effect transistor technology) beyond the 3 nm technology node[1]. To further scale the length dimensions as well as maintaining a good drive current, it is critical to suppress SCEs. This can be achieved using an increased number of thinner stacked channels. However, the performance of conventional semiconductor-based transistors rapidly decreases below a thickness of 3 nm for silicon and 10 nm for InGaAs.

Two-dimensional (2D) semiconductors are an alternate channel material with nanoscale thicknesses and higher mobilities at monolayer or few-layer thickness compared with conventional semiconductors[2–11]. However, 2D materials suffer from a lack of high-quality large-area CMOS-compatible growth techniques. It is also difficult to form dielectrics on their van der Waals surfaces. In addition, the materials are difficult to dope and suffer from high contact resistances induced at the Schottky metal/semiconductor contacts.

Oxide semiconductors—and amorphous indium–gallium–zinc oxide (IGZO) in particular—are leading semiconducting channel materials in thin-film transistors (TFTs) for flat-panel display applications[12]. But despite being a mature technology for high-volume manufacturing, oxide semiconductors are rarely considered as channel materials for scaled high-performance transistors. This is due to their low charge carrier mobility of about 10 cm^2 V^{-1} s^{-1} and the fact that when used in mass production, they typically require channel thicknesses of up to several tens of nanometres[13]. However, there has been interest in the use of oxide semiconductor transistors in CMOS back-end-of-line (BEOL) for monolithic three-dimensional (3D) integration applications[14–21]. In particular, an atomic layer deposition (ALD)-based oxide semiconductor and device technology was developed with channel thicknesses down to sub-1 nm and high field-effect mobility (μ_{FE}) of >100 cm^2 V^{-1} s^{-1} (refs. [20,22–25]). The wafer-scale homogeneous and conformal ALD indium oxide (In_2O_3) thin film has a low thermal budget of 225 °C and an atomically smooth surface. The ability to deposit conformal films on 3D structures by ALD could be useful for 3D integration applications, including 3D BEOL integration and 3D vertical NAND.

ALD-deposited In_2O_3 has a number of advantages for use in transistor applications. The layer-by-layer self-limited growth mechanism of ALD[26–29] enables an atomically smooth surface such that nanometre-thick uniform thin films can be achieved that suppress roughness-related carrier scattering and deterioration of band structure. In addition, the charge neutrality level (CNL) of In_2O_3 lies deep inside the conduction band; therefore, a high electron density exists in atomically thin channels, providing a more forgiving metal-to-semiconductor low-resistive contact due to Fermi-level pinning[24], thus leading to the high on-state currents in transistors that use nanometre-thick channels.

In this Article, we report high-performance In_2O_3 transistors fabricated using ALD. Our devices have channel lengths (L_{ch}) down to 8.0 nm, channel thickness (T_{ch}) as low as 0.50 nm and equivalent dielectric oxide thicknesses (EOT) down to 0.84 nm. The scaling and low contact resistance of the devices enable them to achieve on-state currents ($I_{D,max}$) of 3.1 A mm^{-1} at drain voltages (V_{DS}) of 0.5 V and transconductance values (g_m) of 1.5 S mm^{-1} at V_{DS} of 1.0 V. Our devices offer promising performance compared with devices based on conventional semiconducting materials (such as Si and GaAs), 2D semiconductors and other oxide semiconductors, particularly at the ultrathin scale of 1.0–3.5 nm.

Device architecture and fabrication

Figure 1a illustrates the schematic of the ALD In_2O_3 transistor in this work. The gate stack includes 40 nm Ni as the gate metal and HfO_2 as the gate dielectric, unless specified otherwise, and 0.5–3.5 nm In_2O_3 as the semiconducting channels. ALD In_2O_3 exhibits an atomically smooth surface with surface roughness as low as 0.16 nm

[1]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN, USA. [2]Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China. [3]School of Materials Engineering, Purdue University, West Lafayette, IN, USA.
✉e-mail: yep@purdue.edu

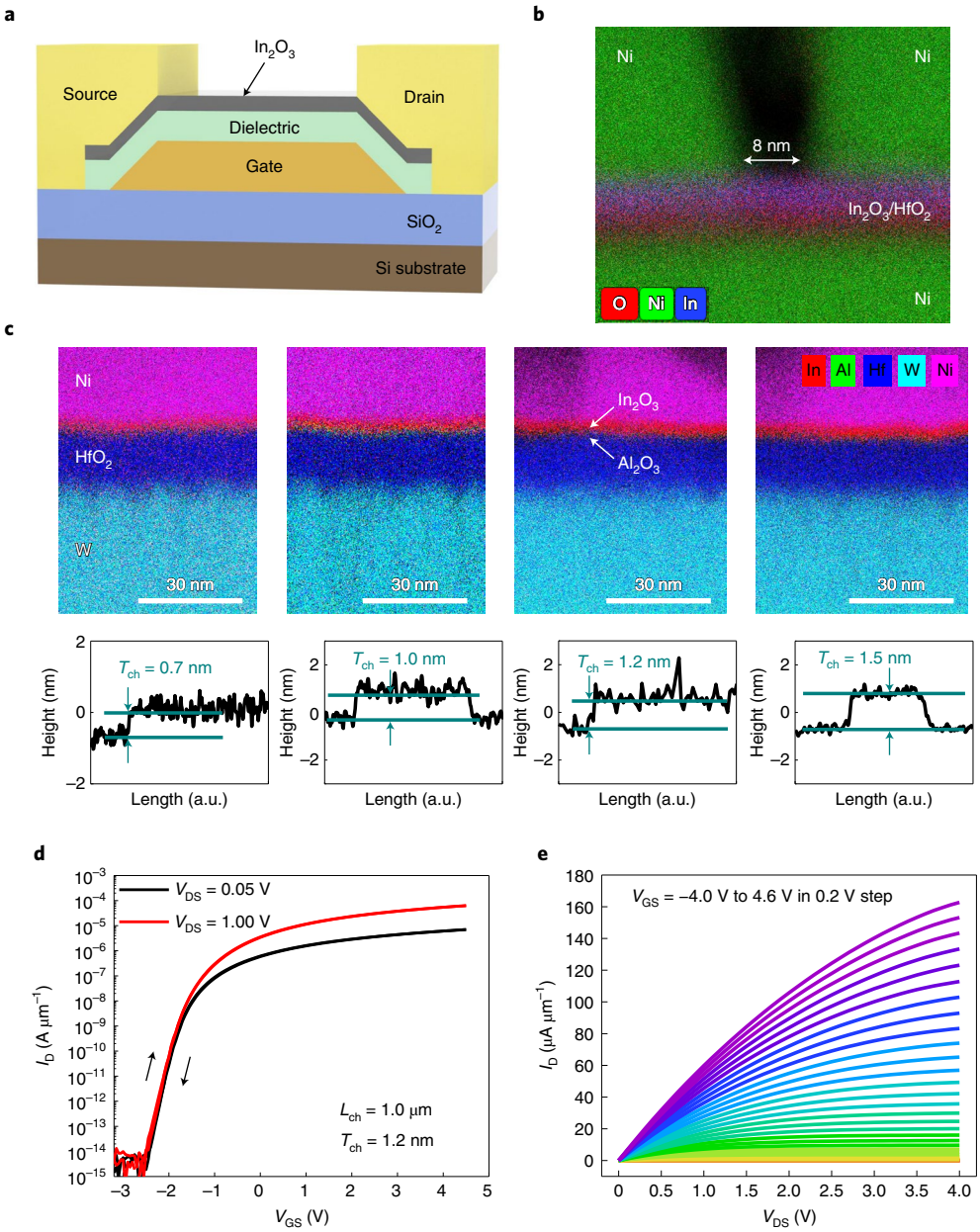

Fig. 1 | Schematic, TEM images and *I*–*V* characteristics of ALD In_2O_3 transistors. a, Schematic of an ALD In_2O_3 transistor. **b**, HAADF-STEM cross-sectional image with EDX elemental mapping of an In_2O_3 transistor with L_{ch} of 8.0 nm, T_{ch} of 3.5 nm and 3.0 nm HfO_2 as the gate insulator, capturing the 8.0 nm channel length. **c**, HAADF-STEM cross-sectional images with EDX elemental mapping and AFM measurements of In_2O_3 transistors with W/HfO_2/Al_2O_3/In_2O_3/Ni gate stack with T_{ch} ranging from 0.7 nm to 1.5 nm. **d**,**e**, I_D–V_{GS} (**d**) and I_D–V_{DS} (**e**) characteristics of a representative ALD In_2O_3 transistor with L_{ch} of 1 μm, T_{ch} of 1.2 nm and 10.0 nm HfO_2/1.0 nm Al_2O_3 as the gate insulator. The device exhibits a high on/off ratio of >10^{10} and negligible hysteresis due to the semiconductor with a relatively wide bandgap and high-quality oxide/semiconductor interface.

(ref. [22]), measured by atomic force microscopy (AFM), being beneficial to the thickness scaling of ALD In_2O_3. The device has a channel width (W_{ch}) of 2.0 μm for $L_{ch} \geq 40$ nm, whereas W_{ch} of 0.6 μm for $L_{ch} < 40$ nm. The W_{ch} value was accurately defined by electron-beam (e-beam) lithography and dry etching (Supplementary Fig. 1b). A reduced W_{ch} is used to suppress the self-heating effect. Ni by e-beam evaporation is used as the source/drain electrode. The device fabrication process is comprehensively discussed in Methods. Figure 1b shows the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) with energy-dispersive X-ray spectroscopy (EDX) mapping of a representative In_2O_3 transistor with L_{ch} of 8.0 nm, T_{ch} of 3.5 nm and hafnium oxide thickness (T_{ox}) of 3.0 nm, highlighting the Ni/In/O elements. EDX mapping with Ni/In/Hf/O elements is shown in Supplementary Fig. 1a. L_{ch}, defined as the distance between the source/drain Ni electrodes, is measured to be 8 nm in this device. Figure 1c presents the HAADF-STEM with EDX mapping images on a W/HfO_2/Al_2O_3/In_2O_3/Ni stack, with In_2O_3 thicknesses ranging from 0.7 to 1.5 nm. The thicknesses of In_2O_3 are determined by both AFM measurements and transmission electron microscopy (TEM) images (similar to a previous work[24]). Figure 1d,e shows the I_D–V_{GS} (gate-source voltage) and I_D–V_{DS} characteristics of a representative ALD In_2O_3 transistor with L_{ch} of 1 μm, T_{ch} of 1.2 nm and 10.0 nm HfO_2/1.0 nm Al_2O_3 as the gate insulator. The device exhibits a high on/off ratio of >10^{10} due to the relatively

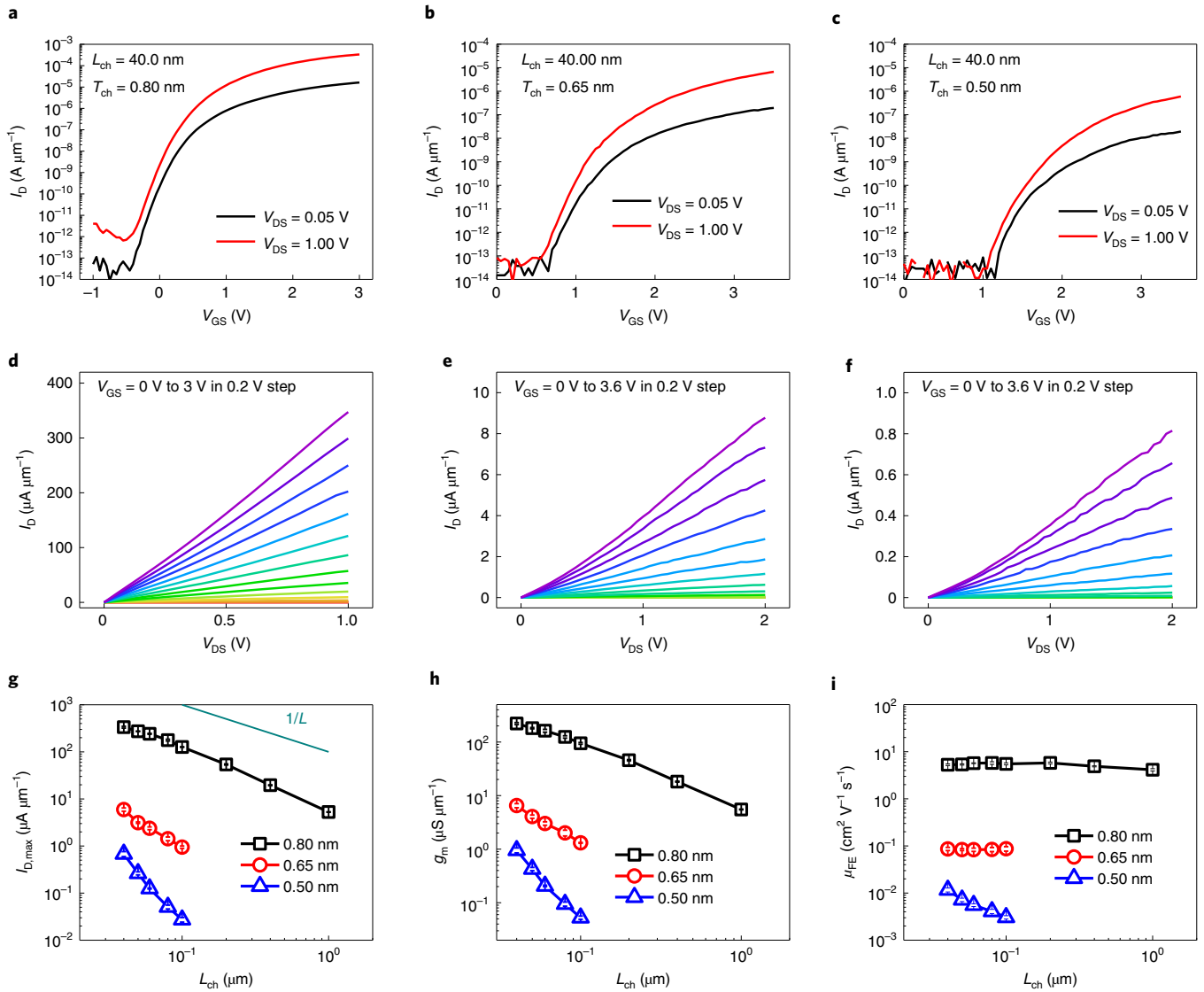

Fig. 2 | Thickness scaling of ALD In_2O_3 down to 0.5 nm. a–c, I_D–V_{GS} characteristics of ALD In_2O_3 transistors with L_{ch} of 40.0 nm; 5.0 nm HfO_2 as the gate insulator; and T_{ch} of 0.80 nm (**a**), 0.65 nm (**b**) and 0.50 nm (**c**). **d–f**, I_D–V_{DS} characteristics of the same ALD In_2O_3 transistors as **a–c** with L_{ch} of 40.0 nm; 5.0 nm HfO_2 as the gate insulator; and T_{ch} of 0.80 nm (**d**), 0.65 nm (**e**) and 0.50 nm (**f**). **g–i**, $I_{D,max}$ (**g**), g_m (**h**) and μ_{FE} (**i**) scaling metrics of ALD In_2O_3 transistors with different T_{ch} values and with 5 nm HfO_2 as the gate insulator at V_{DS} of 1 V. Each data point represents the average of at least five devices. Well-behaved transfer and output characteristics with an on/off ratio of >10^7 are achieved with channel thickness down to 0.5 nm. The impact of the Schottky barrier at the metal/semiconductor interface on the output characteristics is clearly observed with T_{ch} below 1 nm due to the effect of quantum confinement on the band structure of the ultrathin In_2O_3 film.

wide bandgap of In_2O_3 (~3.0 eV) and negligible hysteresis due to the high-quality oxide/semiconductor interface. This device has a subthreshold (SS) of 130.4 mV dec^{-1} at V_{DS} of 1 V, which can be further reduced by EOT scaling and proper interface engineering[22,23].

Device scaling

To further improve the performance of ALD In_2O_3 transistors, device scaling is performed including channel length scaling, EOT scaling and channel thickness scaling, where EOT scaling and channel thickness scaling are essential to enhance the gate electrostatic control to improve the immunity to SCEs. T_{ch} scaling down to 0.5 nm is achieved in this work as shown in the I_D–V_{GS} characteristics with T_{ch} of 0.80, 0.65 and 0.50 nm (Fig. 2a–c). The corresponding I_D–V_{DS} characteristics are shown in Fig. 2d–f. The devices have SS of 109.0, 114.3 and 108.2 mV dec^{-1} at V_{DS} of 1 V for T_{ch} of 0.80, 0.65 and 0.50 nm, respectively. Here 5 nm HfO_2 is used as the gate dielectric. Evidently, even with T_{ch} of 0.5 nm, well-behaved transfer characteristics with on/off ratios over seven orders are achieved. A functional transistor made of a 3D semiconducting channel material and with T_{ch} as low as 0.5 nm has never been reported before because of two reasons. First, it is very challenging to achieve an atomically smooth and uniform semiconducting film by conventional thin-film deposition techniques such as sputtering, chemical vapour deposition and so on, resulting in the degradation of electrical performance due to carrier scattering and change in band structures due to roughness. Second, it is difficult to form a good metal/semiconductor contact with low contact resistivity on an ultrathin semiconducting film. The Fermi-level pinning problem owing to the metal-induced gap states results in the Schottky barrier at the metal/semiconductor interface, which is more severe in an ultrathin film due to quantum confinement effects. ALD In_2O_3 is found to overcome these two challenges at the nanometre scale.

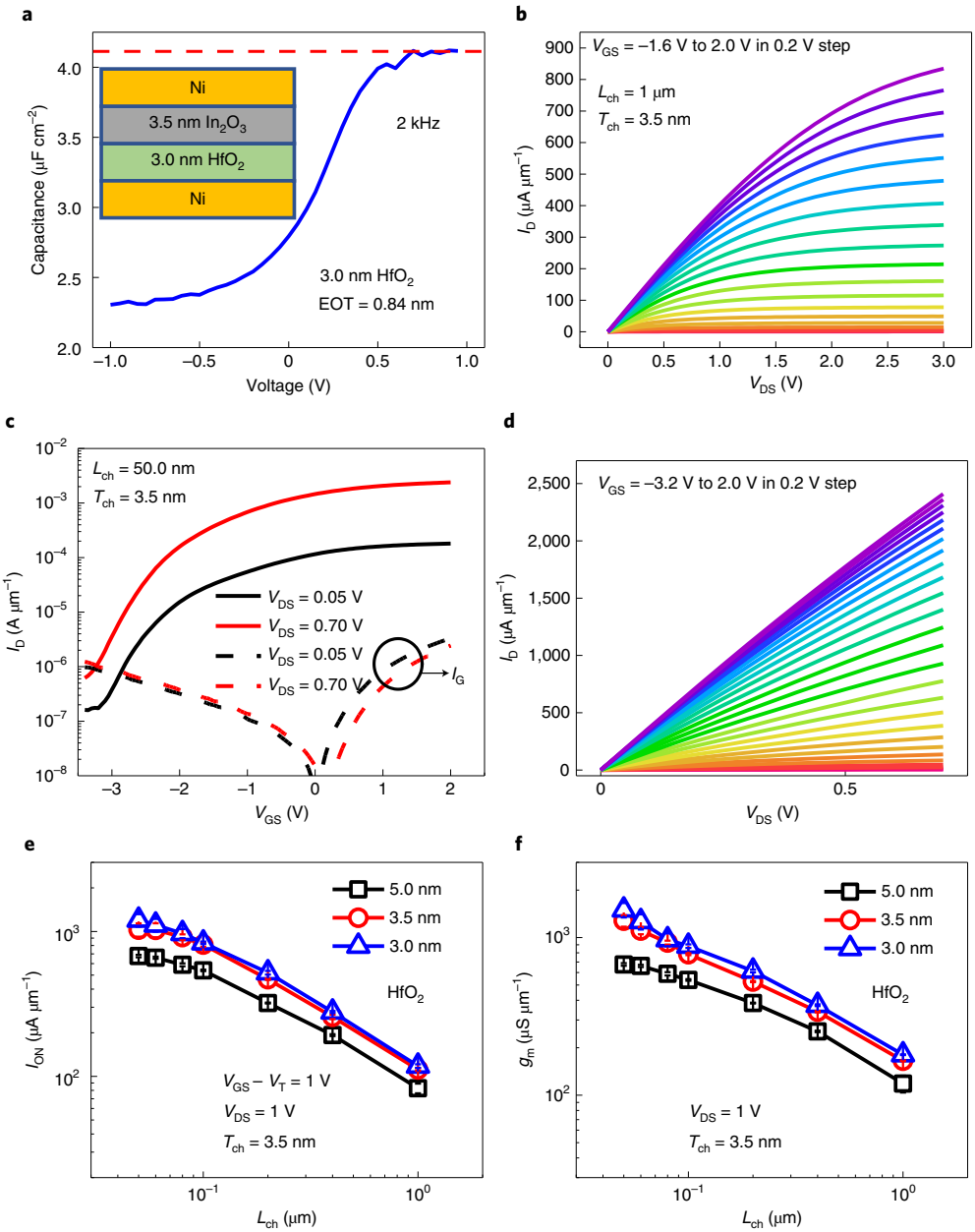

Fig. 3 | EOT scaling of ALD In_2O_3 transistors down to sub-1 nm. a, *C*–*V* measurement of the gate stack capacitor (Ni/3.0 nm HfO_2/3.5 nm In_2O_3/Ni) at 2 kHz, fabricated together with the ALD In_2O_3 transistor on the same chip. EOT of 0.84 nm is achieved, suggesting a high-quality HfO_2/In_2O_3 interface by ALD. **b**, I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 1 μm, T_{ch} of 3.5 nm and EOT of 0.84 nm, showing well-behaved drain saturation due to the high drain bias. A high drain current of 835 μA μm^{-1} is achieved at this long L_{ch} of 1 μm. **c**,**d**, I_D–V_{GS} (**c**) and I_D–V_{DS} (**d**) characteristics of an In_2O_3 transistor with L_{ch} of 50.0 nm, T_{ch} of 3.5 nm and EOT of 0.84 nm at V_{DS} of 0.05 V and 0.70 V. The relatively low on/off ratio is because of the gate leakage current (I_G) in the off state, which may be further improved by V_T tuning. **e**,**f**, I_{ON} (**e**) and g_m (**f**) scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm to 50.0 nm, T_{ch} of 3.5 nm and T_{ox} of 3.0 nm, 3.5 nm and 5.0 nm. I_{ON} is extracted at $V_{GS} - V_T = 1$ V and $V_{DS} = 1$ V. g_m is extracted at $V_{DS} = 1$ V. Each data point represents the average of at least five devices. High I_{ON} of 1.2 A mm^{-1} at $V_{GS} - V_T = 1$ V and $V_{DS} = 1$ V and g_m of 1.5 S mm^{-1} at $V_{DS} = 1$ V are achieved.

First, the layer-by-layer self-limiting growth mechanism ensures an atomically smooth surface and uniform film. Second, the CNL of bulk In_2O_3 aligns at about 0.4 eV above the conduction band edge (E_C); therefore, thick In_2O_3 behaves like a conducting oxide[30]. As a result, the Fermi level is pinned above E_C for a metal/In_2O_3 contact, leading to a low contact resistance below 0.1 Ω mm even at the nanometre scale. The contact resistance was extracted by the transmission line method[20]. Note that the above property is fundamental when searching for a 3D semiconductor with high performance for an ultrathin channel. It is expected that a 3D semiconductor with CNL aligning far above E_C (or far below the valence band edge as the valence band edge (E_V) for p-type devices) is necessary to achieve a high-performance transistor with an ultrathin channel at the nanometre scale. Figure 2g–i presents the maximum drain current ($I_{D,max}$), g_m and μ_{FE} scaling metrics. Here μ_{FE} is calculated using the maximum g_m at a low drain bias. The on-state performance rapidly degrades below 1 nm (Fig. 2). Devices with T_{ch} of 0.4 nm have no detectable drain currents (Supplementary Fig. 2a). Further, $I_{D,max}$ exponentially reduces when T_{ch} linearly decreases from 0.8 to 0.5 nm (Supplementary Fig. 2b) due to the impact of

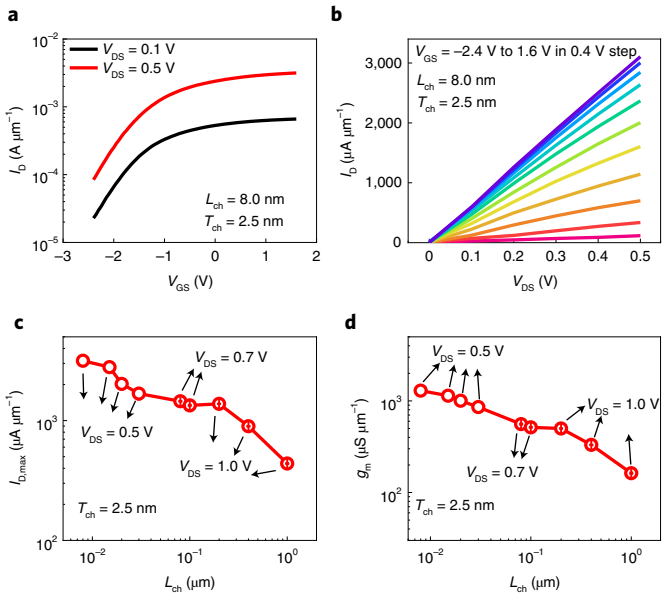

Fig. 4 | Channel length scaling of ALD In_2O_3 transistors down to 8 nm. **a**,**b**, I_D–V_{GS} (**a**) and I_D–V_{DS} (**b**) characteristics of In_2O_3 transistors with L_{ch} of 8.0 nm, T_{ch} of 2.5 nm and EOT of 0.84 nm. **c**,**d**, $I_{D,max}$ (**c**) and g_m (**d**) scaling metrics of the best-performance In_2O_3 transistors with L_{ch} from 1 μm to 8.0 nm with T_{ch} of 2.5 nm. Lower voltages are used for shorter channel devices to avoid the impact of self-heating on devices.

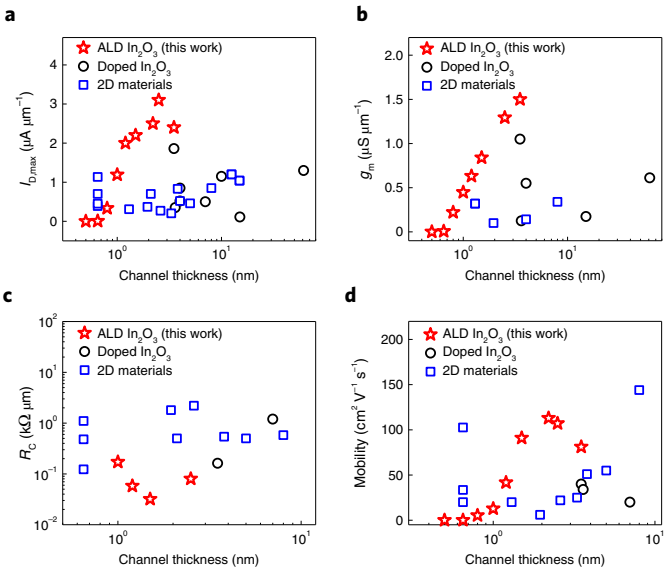

Fig. 5 | Benchmarking of ALD In_2O_3 with other ultrathin semiconductors. **a**–**d**, Comparison of $I_{D,max}$ (**a**), g_m (**b**), R_C (**c**) and mobility (**d**) versus channel thickness characteristics with other high-performance oxide semiconductor (doped In_2O_3) devices by sputtering and 2D semiconductor devices (MoS_2, WS_2 and black phosphorus). The data used in this figure are listed in Supplementary Table 1. ALD In_2O_3 demonstrates the best performance in terms of $I_{D,max}$, g_m, R_C and mobility in the 1.0–3.5 nm range compared with all known semiconducting materials to the best of our knowledge.

quantum confinement on the band structure of the In_2O_3 thin film. The drain-current scaling metrics are found to deviate from $1/L$ (Fig. 2g), indicating that it is more difficult to accumulate carriers in long channels, most likely due to the percolation mechanism[31]. Additional data on SS and threshold voltage (V_T) scaling metrics are shown in Supplementary Fig. 3.

A second approach to enhance the gate electrostatic control is EOT scaling. Here we demonstrate high-performance ALD In_2O_3 transistors with EOT scaled down to 0.84 nm. Figure 3a shows the capacitance–voltage (C–V) characteristics of the gate stack capacitor (Ni/3.0 nm HfO_2/3.5 nm In_2O_3/Ni), fabricated together with In_2O_3 transistors with the same gate stack. EOT is calculated to be 0.84 nm, using $C_{ox} = \epsilon_0\epsilon_{SiO2}/EOT$, where $\epsilon_{SiO2} = 3.9$ is the dielectric constant of SiO_2, $\epsilon_0 = 8.85 \times 10^{-14}$ F cm^{-1} is the vacuum permittivity and C_{ox} is measured from the C–V measurement at high V_{GS} and low frequency. These numbers confirm a high-quality bulk gate oxide and oxide/semiconductor interface. The doping concentration (N_D) of In_2O_3 can be extracted from the $1/C^2$ versus voltage characteristics according to $N_D = \frac{2}{q\epsilon_S\epsilon_0 d(1/C^2)/dV}$ (ref. [32]), where q is the elementary charge and ϵ_S is the relative dielectric constant of In_2O_3 (~8.9)[33]. Supplementary Fig. 4 shows the $1/C^2$ versus voltage characteristics obtained from Fig. 3a. From the slope of the $1/C^2$ versus voltage characteristics, N_D can be estimated as 9.0×10^{19} cm^{-3}. Figure 3b shows the I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 1 μm, T_{ch} of 3.5 nm and EOT of 0.84 nm, showing well-behaved drain current saturation. Figure 3c,d shows the I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 50.0 nm, T_{ch} of 3.5 nm and EOT of 0.84 nm. The device has SS of 387.3 mV dec^{-1} at V_{DS} of 0.7 V. The relatively large SS and apparent drain-induced barrier lowering is partly due to the gate leakage current in highly scaled EOT. The maximum I_D of 2.4 A mm^{-1} is achieved at a low V_{DS} of 0.7 V. Drain current saturation is not achieved because $V_{GS} - V_T$ is much larger than V_{DS}; therefore, the pinch-off condition is not fulfilled. Figure 3e,f summarizes the I_{ON} and g_m scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm down to 50.0 nm, T_{ch} of 3.5 nm and T_{ox} from 3.0 to 5.0 nm. Each data point represents the average of at least five devices. The small error bar in these plots demonstrates that the ALD-based In_2O_3 transistors are highly uniform. I_{ON} is extracted at $V_{GS} - V_T = 1$ V and $V_{DS} = 1$ V. The maximum g_m is extracted at $V_{DS} = 1$ V. I_{ON} and g_m are found to be improved significantly by EOT scaling. A high average I_{ON} of 1.2 A mm^{-1} is achieved at L_{ch} of 50 nm and at $V_{GS} - V_T = 1$ V and $V_{DS} = 1$ V. A high average g_m of 1.5 S mm^{-1} is achieved at L_{ch} of 50 nm and $V_{DS} = 1$ V. These values are one of the highest among the known reported oxide semiconductor transistors.

Figure 4a,b shows the I_D–V_{GS} and I_D–V_{DS} characteristics of ALD In_2O_3 transistors with L_{ch} of 8.0 nm, T_{ch} of 2.50 nm and EOT of 0.84 nm. One of the highest $I_{D,max}$ of 3.1 A mm^{-1} is achieved due to the scaled device dimension and low contact resistance, where $I_D > 3.0$ A mm^{-1} is achieved on oxide semiconductor transistors. The $I_{D,max}$ and g_m scaling metrics with L_{ch} from 1 μm down to 8 nm of In_2O_3 transistors are shown in Fig. 4c,d. A lower V_{DS} of 0.5 V is used for the shorter channel length to avoid the self-heating effect due to the high power density in the ultrascaled device area. The corresponding V_{DS} at different L_{ch} values is marked in the figure. Considering V_{DS} of 0.5 V and I_D of 3.1 A mm^{-1}, contact resistance (R_C) can be estimated to be less than 0.08 Ω mm.

Device performance benchmarking

The performance of scaled ALD In_2O_3 transistors in this work is benchmarked with state-of-the-art high-performance transistors with an ultrathin channel, such as 2D transistors and oxide semiconductor transistors, using figures of merit of I_{ON}, g_m, R_C and mobility versus channel thickness (Supplementary Table 1). ALD In_2O_3 transistors exhibit the largest $I_{D,max}$ in the range of 1.0–3.5 nm and the largest g_m below 3.5 nm, among all the known semiconductor thin films to the best of our knowledge (Fig. 5a,b). Such high-performance material and device properties are mainly contributed by the low contact resistance benefiting from the unique CNL alignments in In_2O_3 (Fig. 5c) and the high mobility in the

nanometre scale between 1.0 and 3.5 nm, also benefiting from the atomic thickness control of ALD (Fig. 5d).

Conclusions

We have reported an ALD-based oxide semiconductor transistor technology that shows promising on-state currents—compared with both established and emerging material technologies—when channel thicknesses are fabricated in the range of approximately 1.0–3.5 nm. Our approach takes advantage of the self-limiting growth mechanism of ALD and the unique band structure of In_2O_3. The conformal deposition on 3D structures by ALD also has the potential to create new opportunities for 3D integration, such as BEOL-compatible transistors for monolithic 3D integration and semiconducting channels for 3D vertical NAND.

Methods

Device fabrication. The device fabrication process is similar to previous work[22]. The device fabrication process started with solvent cleaning of the p^+ Si substrate with thermally grown 90 nm SiO_2. A bilayer photoresist lithography process (PMGI SF9 + AZ1518) was then applied for the sharp lift-off of the 40 nm Ni gate metal by e-beam evaporation. This step is critical to avoid sidewall metal coverage such that high-quality ALD gate dielectric can be formed for EOT scaling. HfO_2 with various thicknesses was deposited as the gate insulator by ALD at 200 °C with $[(CH_3)_2N]_4Hf$ and H_2O as the Hf and O precursors, respectively. In_2O_3 thin films with various thicknesses were deposited by ALD at 225 °C using $(CH_3)_3In$ and H_2O as the In and O precursors, respectively. N_2 is used as the carrier gas at a flow rate of 40 s.c.c.m. The base pressure at the N_2 flow rate of 0 s.c.c.m. is 169 mtorr, whereas the base pressure at the N_2 flow rate of 40 s.c.c.m. is 437 mtorr. Concentrated HCl was employed for channel isolation. The source/drain ohmic contacts were formed by e-beam evaporation of Ni in two steps to avoid difficulty during the sub-10 nm lift-off process. It is difficult to form a sub-10 nm channel length by one-step e-beam lithography because of the proximity effect that causes electron backscattering into the channel region. Therefore, a two-step e-beam lithography process was adopted by the formation of the source electrode first and then the drain electrode. A wide range of distances between the source and drain electrodes are defined in the masks so that both short and long channel lengths can be achieved. Then, a second step of ICP dry etching using BCl_3/Ar plasma was used to accurately define the channel width. The devices were annealed in O_2 at 250 °C for 4 min to further improve the performance.

Material characterization. The thickness of In_2O_3 was determined together by AFM, TEM and ellipsometry. The AFM measurement was done with a Veeco Dimension 3100 atomic force microscope system. TEM lamella samples were prepared with Helios G4 UX DualBeam scanning electron microscope. FEI Talos F200X operated at 200 kV equipped with Super-X EDX was used for HAADF-STEM imaging.

Device characterization. Electrical characterization was carried out with a Keysight B1500 system and a Cascade Summit probe station in the dark and N_2 environments at room temperature and ambient atmosphere.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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References

1. Loubet, N. et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In *2017 Symposium on VLSI Technology* T230–T231 (IEEE, 2017).
2. Yang, L. et al. High-performance MoS_2 field-effect transistors enabled by chloride doping: record low contact resistance (0.5 kΩ·μm) and record high drain current (460 μA/μm). In *2014 Symposium on VLSI Technology* 1–2 (IEEE, 2014).
3. Krasnozhon, D., Dutta, S., Nyffeler, C., Leblebici, Y. & Kis, A. High-frequency, scaled MoS_2 transistors. In *2015 IEEE International Electron Devices Meeting (IEDM)* 27.4.1–27.4.4 (IEEE, 2015).
4. Liu, Y. et al. Pushing the performance limit of sub-100 nm molybdenum disulfide transistors. *Nano Lett.* **16**, 6337–6342 (2016).
5. Yang, L. M. et al. Few-layer black phosporous PMOSFETs with BN/Al_2O_3 bilayer gate dielectric: achieving I_{on} = 850 μA/μm, g_m = 340 μS/μm, and R_c = 0.58 kΩ·μm. In *2016 IEEE International Electron Devices Meeting (IEDM)* 5.5.1–5.5.4 (IEEE, 2016).
6. Si, M., Yang, L., Du, Y. & Ye, P. D. Black phosphorus field-effect transistor with record drain current exceeding 1 A/mm. In *2017 75th Annual Device Research Conference (DRC)* 1–2 (IEEE, 2017); https://doi.org/10.1109/DRC.2017.7999395
7. Li, X. et al. High-speed black phosphorus field-effect transistors approaching ballistic limit. *Sci. Adv.* **5**, eaau3194 (2019).
8. Chou, A.-S. et al. High on-current 2D nFET of 390 μA/μm at V_{DS} = 1V using monolayer CVD MoS_2 without intentional doping. In *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2020).
9. Shen, P. C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
10. Lin, D. et al. Scaling synthetic WS_2 dual-gate MOS devices towards sub-nm CET. In *2021 Symposium on VLSI Technology* 1–2 (IEEE, 2021).
11. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
12. Nomura, K. et al. Amorphous oxide semiconductors for high-performance flexible thin-film transistors. *Jpn J. Appl. Phys.* **45**, 4303–4308 (2006).
13. Kamiya, T., Nomura, K. & Hosono, H. Present status of amorphous In–Ga–Zn–O thin-film transistors. *Sci. Technol. Adv. Mater.* **11**, 044305 (2010).
14. Matsubayashi, D. et al. 20-nm-node trench-gate-self-aligned crystalline In-Ga-Zn-oxide FET with high frequency and low off-state current. In *2015 IEEE International Electron Devices Meeting (IEDM)* 6.5.1–6.5.4 (IEEE, 2015).
15. Li, S. et al. Nanometre-thin indium tin oxide for advanced high-performance electronics. *Nat. Mater.* **18**, 1091–1097 (2019).
16. Li, S., Gu, C., Li, X., Huang, R. & Wu, Y. 10-nm channel length indium-tin-oxide transistors with I_{on} = 1,860 μA/μm, G_m = 1050 μS/μm at V_{ds} = 1 V with BEOL compatibility. In *IEEE International Electron Devices Meeting (IEDM)* 40.5.1–40.5.4 (IEEE, 2020).
17. Samanta, S. et al. Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: achieving record high $G_{m,max}$ of 125 μS/μm at V_{DS} of 1 V and I_{ON} of 350 μA/μm. In *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2020).
18. Chakraborty, W. et al. BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with I_{on} = 370μA/μm, SS = 73mV/dec and I_{on}/I_{off} ratio > 4×10^9. In *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2020).
19. Si, M. et al. Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating. *ACS Nano* **14**, 11542–11547 (2020).
20. Si, M., Lin, Z., Charnas, A. & Ye, P. D. Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V. *IEEE Electron Device Lett.* **42**, 184–187 (2021).
21. Han, K. et al. First demonstration of oxide semiconductor nanowire transistors: a novel digital etch technique, IGZO channel, nanowire width down to ~20 nm, and I_{on} exceeding 1,300 μA/μm. In *2021 Symposium on VLSI Technology* 1–2 (IEEE, 2021).
22. Si, M., Charnas, A., Lin, Z. & Ye, P. D. Enhancement-mode atomic-layer-deposited In_2O_3 transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment. *IEEE Trans. Electron Devices* **68**, 1075–1080 (2021).
23. Charnas, A., Si, M., Lin, Z. & Ye, P. D. Enhancement-mode atomic-layer thin In_2O_3 transistors with maximum current exceeding 2 A/mm at drain voltage of 0.7 V enabled by oxygen plasma treatment. *Appl. Phys. Lett.* **118**, 052107 (2021).
24. Si, M. et al. Why In_2O_3 can make 0.7 nm atomic layer thin transistors. *Nano Lett.* **21**, 500–506 (2021).
25. Si, M., Lin, Z., Chen, Z. & Ye, P. D. First demonstration of atomic-layer-deposited BEOL-compatible In_2O_3 3D fin transistors and integrated circuits: high mobility of 113 $cm^2/V\cdot s$, maximum drain current of 2.5 mA/μm and maximum voltage gain of 38 V/V in In_2O_3 inverter. In *2021 Symposium on VLSI Technology* 1–2 (IEEE, 2021).
26. Mourey, D. A., Zhao, D. A., Sun, J. & Jackson, T. N. Fast PEALD ZnO thin-film transistor circuits. *IEEE Trans. Electron Devices* **57**, 530–534 (2010).
27. Kim, H. Y. et al. Low-temperature growth of indium oxide thin film by plasma-enhanced atomic layer deposition using liquid dimethyl(*N*-ethoxy-2,2-dimethylpropanamido)indium for high-mobility thin film transistor application. *ACS Appl. Mater. Interfaces* **8**, 26924–26931 (2016).
28. Ma, Q. et al. Atomic-layer-deposition of indium oxide nano-films for thin-film transistors. *Nanoscale Res. Lett.* **13**, 4 (2018).
29. Lee, J. et al. High mobility ultra-thin crystalline indium oxide thin film transistor using atomic layer deposition. *Appl. Phys. Lett.* **113**, 112102 (2018).
30. Robertson, J. & Clark, S. J. Limits to doping in oxides. *Phys. Rev. B* **83**, 075205 (2011).
31. Kamiya, T., Nomura, K. & Hosono, H. Electronic structures above mobility edges in crystalline and amorphous In-Ga-Zn-O: percolation conduction examined by analytical model. *J. Display Technol.* **5**, 462–467 (2009).
32. Schroder, D. K. *Semiconductor Material and Device Characterization* 3rd edn (Wiley, 2006).

33. Hamberg, I. & Granqvist, C. G. Evaporated Sn-doped In_2O_3 films: basic optical properties and applications to energy-efficient windows. *J. Appl. Phys.* **60**, R123–R160 (1986).

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Author contributions

P.D.Y. and M.S. conceived the idea and proposed the ALD In_2O_3 scaling research. M.S. developed the ALD process of In_2O_3 as a high-performance oxide semiconductor. M.S. and Z.L. performed the device fabrication, electrical measurement and analysis on thickness and EOT scaling of ALD In_2O_3 devices. Z.L. and M.S. conducted the channel length scaling of ALD In_2O_3 devices down to 8 nm. Z.C., X.S. and H.W. performed the STEM and EDX measurements. M.S. and P.D.Y. co-wrote the manuscript and all the authors commented on it.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Peide D. Ye.

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