Steep-Slope WSe$_2$ Negative Capacitance Field-Effect Transistor

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Supporting Information

ABSTRACT: P-type two-dimensional steep-slope negative capacitance field-effect transistors are demonstrated for the first time with WSe$_2$ as channel material and ferroelectric hafnium zirconium oxide in gate dielectric stack. F$_4$-TCNQ is used as p-type dopant to suppress electron leakage current and to reduce Schottky barrier width for holes. WSe$_2$ negative capacitance field-effect transistors with and without internal metal gate structures and the internal field-effect transistors are compared and studied. Significant SS reduction is observed in WSe$_2$ negative capacitance field-effect transistors by inserting the ferroelectric hafnium zirconium oxide layer, suggesting the existence of internal amplification ($\sim10$) due to the negative capacitance effect. Subthreshold slope less than 60 mV/dec (as low as 14.4 mV/dec) at room temperature is obtained for both forward and reverse gate voltage sweeps. Negative differential resistance is observed at room temperature on WSe$_2$ negative capacitance field-effect transistors as the result of negative capacitance induced negative drain-induced-barrier-lowering effect.

KEYWORDS: Tungsten diselenide, negative capacitance, ferroelectric oxide, steep slope, internal metal gate

The so-called Boltzmann Tyranny (associated with the Boltzmann distribution of carriers) defines the fundamental thermionic limit of the subthreshold slope (SS) of a metal-oxide-semiconductor field-effect transistor (MOSFET) at 60 mV/dec at room temperature, which prohibits the decrease of the supply voltage and power consumption. Negative capacitance FETs (NC-FETs) have been proposed and attracted much attention to overcome this thermionic limit of SS.$^{1-14}$ In an NC-FET, the insulating ferroelectric material layer served as a negative capacitor so that channel surface potential can be amplified more than the gate voltage, and hence the device can operate with SS less than 60 mV/dec at room temperature. Transition metal dichalcogenides (TMDs) have been intensely explored as two-dimensional (2D) semiconductors for future device technologies because of the atomically ultrathin body for the ideal electrostatic control of the channel. It would be highly desirable to integrate ferroelectric insulator and 2D ultrathin channel materials as 2D NC-FETs to achieve subthermionic SS for low power dissipation and excellent immunity to short channel effects for transistor scaling. Very recently, n-type 2D NC-FETs with molybdenum disulphide (MoS$_2$) as channel material and Si CMOS compatible Hf-based ferroelectric oxide as gate dielectric have been demonstrated with subthermionic SS at room temperature.$^{10-14}$ However, both p-type and n-type FETs are required for complementary metal-oxide-semiconductor (CMOS) device technology but no p-type 2D NC-FETs with sub-60 mV/dec subthreshold slope was reported. Tungsten diselenide (WSe$_2$) is one of the most studied TMDs as a highly promising p-type channel material, because of its balanced conduction and valence band edges and high hole mobility.$^{15-22}$ Intrinsic WSe$_2$ FETs usually exhibit ambipolar transport behavior due to the band alignment of metal to WSe$_2$ near the middle of the bandgap, so that doping technique is required to obtain high performance WSe$_2$ transistors. P-type chemical doping in WSe$_2$ such as NO$_2$ and 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F$_4$-TCNQ) has been studied to enhance the hole transport and reduce the Schottky barrier width.$^{15,20}$

In this Letter, we demonstrate for the first time steep-slope p-type WSe$_2$ NC-FETs by combining ferroelectric hafnium zirconium oxide (HZO) gate stack and F$_4$-TCNQ p-type chemical doping. The effect of internal metal gate (IMG) on the performance of WSe$_2$ NC-FET is also studied by inserting a metal layer between ferroelectric HZO and the positive gate oxide. For WSe$_2$ NC-FET without IMG and after F$_4$-TCNQ doping, minimum SS of 40.2 mV/dec and less than 60 mV/dec are achieved for both forward and reverse gate-to-source voltage ($V_{GS}$) sweeps on the p-type WSe$_2$ NC-FETs with a low hysteresis of less than 0.2 V. For WSe$_2$ NC-FETs without IMG and before F$_4$-TCNQ doping, the transistors exhibit ambipolar transport behavior and a high drain current ($I_D$) is achieved on nFET due to the enhanced electric field from the ferroelectricity in the gate oxide. Negative differential resistance (NDR), correlated to the drain coupled negative capacitance effect, is also observed on both n-type and p-type NC-FETs. For WSe$_2$ NC-FET with IMG and after F$_4$-TCNQ doping, SS$_{FWD} = 41.2$ mV/dec and SS$_{REV} = 14.4$ mV/dec are achieved.
with negative hysteresis due to the ferroelectric switching, while the SS of internal WSe₂ FET is 79.1 mV/dec. The SS of the WSe₂ NC-FET with IMG is much smaller than the SS measured from the internal WSe₂ FET, suggesting the existence of internal amplification by the ferroelectric HZO.

The experimental device schematic of a WSe₂ NC-FET without IMG is shown in Figure 1a, which consists of few-layer WSe₂ as channel, 2 nm amorphous aluminum oxide (Al₂O₃) layer and 20 nm polycrystalline HZO layer as the gate dielectric, heavily doped silicon substrate as the gate electrode and Pt/Au source/drain contacts. The device schematic of a WSe₂ NC-FET with IMG is shown in Figure 1b, which consists of few-layer WSe₂ as channel, 20 nm polycrystalline HZO, 3 nm amorphous Al₂O₃, 20 nm Ni layer as IMG and 10 nm HfO₂ as the gate dielectric of internal FET, heavily doped silicon substrate as the gate electrode and Pt/Au source/drain contacts. HZO was deposited by atomic layer deposition (ALD) as a ferroelectric insulator layer₂³ on a heavily doped silicon substrate after standard solvent clean and hydrogen fluoride passivation. Hf₁₋ₓZrₓO₂ film was deposited at 250°C, using [(CH₃)₂N]₄Hf (TDMAHf), [(CH₃)₂N]₄Zr (TDMAZr), and H₂O as the Hf precursor, Zr precursor, and O precursor, respectively. The Hf₁₋ₓZrₓO₂ film with x = 0.5 was achieved by controlling HfO₂/ZrO₂ cycle ratio to be 1:1. Another 2 or 3 nm Al₂O₃ layer was in situ deposited at 250 °C, using Al(CH₃)₃ as Al precursor and H₂O as oxygen precursor, as an encapsulation layer to prevent the degradation of HZO by the reaction with moisture in air and the amorphous Al₂O₃ layer was also used for capacitance matching and gate leakage current reduction through polycrystalline HZO. A rapid thermal annealing (RTA) in nitrogen ambient was then performed for 1 min at 500 °C to enhance the ferroelectricity, as shown in Figure 1d. Clear dielectric to ferroelectric transition can be seen after annealing on the metal–insulator–metal (MIM, TiN/10 nm HZO/TiN) capacitor. As the working speed of NC-FETs is directly related with the ferroelectric polarization switching speed, the MIM capacitor structure is also used in high-frequency measurement up to 0.5 MHz to study the time response of ferroelectric switching in HZO, as shown in Figure 2 and in Supporting Information (SI) Section 1.
was first carried out on the completed WSe₂ NC-FETs. The measured sample was then soaked in an isopropyl alcohol solution of 0.75 mmol/L F₄-TCNQ for 12 h followed by N₂ drying for p-type doping of the channel. F₄-TCNQ is an organic molecule with a large electron affinity of 5.2 eV. It is widely used as a p-type dopant for graphene, black phosphorus, TMDs and other low dimensional materials. After doping, the WSe₂ NC-FETs were electrically characterized again under ambient condition. All electrical measurements were carried out at room temperature. The I–V measurement was done using a B1500 system with HRSMU and with HR-ADC in AUTO mode. The time in I–V measurement for each data point can be calculated as time = default integration time × factor, where factor = 20 in this work. Default integration time is related with the current level and can be found from the B1500 manual. Estimated time constants for different current levels are listed as following, 1 pA, 25.6 ms; 10 pA, 25.6 ms; 100 pA, 12.8 ms; 1 nA, 6.4 ms; 10 nA, 6.4 ms; 100 nA, 16 ms; 1 μA, 1.6 ms; 10 μA, 3.2 ms; 100 μA, 1.6 ms.

To study the ferroelectric property of the gate stack, especially the ferroelectric switching at high speed, ferroelectric MIM (TiN/10 nm HZO/TiN) capacitors are used as test structure. The polarization versus electric field (P–E) characteristics is measured in two different ways. At low frequency from 50 Hz to 1 kHz, P–E is measured by a Radiant RT66C ferroelectric tester (voltage sweep), as shown in Figure 2a. At high frequency from 10 kHz to 0.5 MHz, P–E is measured (Figure 2b) based on the transient response to square wave voltage signal in RC circuit, which is discussed in detail in SI Section 1. The P–E shows clear ferroelectric switching up to 0.5 MHz. The measurement at high frequency above 0.1 MHz becomes noisier because of the bandwidth of the measurement system. Therefore, the frequency-dependent measurement here confirmed that in ferroelectric HZO, the ferroelectric switching speed can be at least at megahertz level but the upper limit of ferroelectric switching speed has not been detected by current experimental setup.

The electrical performance of WSe₂ NC-FET without IMG is shown in Figure 3. Figure 3a shows the cross-sectional view of a WSe₂ NC-FET without IMG. The I₉–V₃ characteristics of a WSe₂ NC-FET before F₄-TCNQ doping is shown in Figure 3b. This device has a channel length (L₉) of 0.5 μm and channel thickness (Tₑ) of 5.5 nm, measured by atomic force microscopy (AFM). The I₉–V₃ characteristics were measured in bidirectionally (V₃ from high to low) and reversely (V₃ from low to high) in 20 mV V₃ step. SS is extracted for both forward sweep (SS₉) and reverse sweep (SS₉₋) at low V₃. The device exhibits SS₉ = 249.9 mV/dec, SS₉₋ = 176.0 mV/dec for nFET and the device exhibits SS₉ = 297.4 mV/dec for pFET. Figure 3c shows I₉–V₆ characteristics of the same WSe₂ NC-FET as shown in Figure 3b. The gate voltage is stressed up to 10.5 V and maximum gate voltage over EOT in this device is about 2.4 V/nm. A high maximum drain current of 239 μA/μm is achieved. Clear NDR can be observed in both forward and reverse gate voltage sweeps. Clear NDR can be observed in the measurement system. Therefore, the frequency-dependent

Figure 3. (a) Cross-sectional view of WSe₂ NC-FETs without internal metal gate. (b) I₉–V₃ in 20 mV V₃ step and (c) I₉–V₆ characteristics of a WSe₂ NC-FET before F₄-TCNQ doping. This device has a channel length of 0.5 μm and channel thickness of 5.5 nm. A high maximum drain current of 239 μA/μm is achieved. Clear NDR can be observed in both forward and reverse gate voltage sweeps. Clear NDR can be observed in the measurement system. Therefore, the frequency-dependent

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NDR can naturally occur as a result of the negative DIBL charge into the channel. NDR is observed for both WSe₂ n-type voltage. Meanwhile, a low hysteresis (de as shown in Figure 3f. SS of p-type NC-FET below the thermionic limit is the result of the negative capacitance e indicating the e NC-FET and p-type NC-FET, as shown in Figure 3c,e, demonstrating for both forward and reverse gate voltage sweeps, (c) Id−Vs characteristics in 20 mV Vs step of the internal WSe₂ FET of the same device as in Figure 4b. The device exhibits SS = 79.1 mV/dec (d) SS versus Id characteristics of p-type WSe₂ NC-FET with IMG and the internal WSe₂ FET.

Figure 4. (a) Cross-sectional view of WSe₂ NC-FETs with internal metal gate. (b) Id−Vs characteristics in 20 mV Vs step of a representative WSe₂ NC-FET with IMG and after F4-TCNQ doping. This device has a channel length of 1 μm and channel thickness of 9.6 nm. The device exhibits SSB = 14.4 mV/dec, SSB = 41.2 mV/dec at Vs = −0.1 V. SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps. (c) Id−Vs characteristics in 20 mV Vs step of the internal WSe₂ FET of the same device as in Figure 4b. The device exhibits SS = 79.1 mV/dec (d) SS versus Id characteristics of p-type WSe₂ NC-FET with IMG and the internal WSe₂ FET.

Figure 4a shows the cross-sectional view of a WSe₂ NC-FET with IMG. The IMG here is used to enhance the negative capacitance effect for SS reduction. Figure 4b shows the Id−Vs characteristics of a WSe₂ p-type NC-FET with IMG and after F4-TCNQ doping (IMG floating) in 20 mV Vs step. This device has a channel length of 1 μm, and channel thickness of 9.6 nm. The device exhibits SSB = 14.4 mV/dec, SSB = 41.2 mV/dec, and a negative hysteresis of −0.12 V (at Id = 1 pA/μm). Figure 4c shows the Id−Vs characteristics of the internal WSe₂ FET of the same device as in Figure 4b, using IMG as gate electrode in 20 mV Vs step. Figure 4d shows SS versus Id characteristics in the off-state of Id−Vs characteristics in Figure 4bc. SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps, suggesting the existence of internal amplification. The internal amplification, defined as dVout/dVs, is calculated to be 10/1.8 for reverse/forward gate voltage sweep. Note that the positive hysteresis of the internal WSe₂ FET, as shown in Figure 4c, is induced by trapping and detrapping process in the gate oxide or the oxide/semiconductor interface. This positive hysteresis is much larger compared with WSe₂ NC-FET shown in Figure 3d, suggesting the existence of negative capacitance/ferroelectric effect in the gate stack, which leads to the reduction of positive hysteresis.

In conclusion, WSe₂ NC-FETs with ferroelectric HZO gate stack are demonstrated. Chemical doping of F4-TCNQ is applied to suppress the electron current in the off-state of p-type NC-FETs and to reduce the Schottky barrier width for holes. The doped devices exhibit steep-slope switching characteristics with less than 60 mV/dec for bidirectional sweeps. Sub-60 mV/dec SS (as low as 14.4 mV/dec) and negative DIBL effect conclusively confirm the realization of

suppressing the ambipolar effect and reducing the Schottky barriers are the keys to reduce SS in WSe₂ NC-FETs.

F4-TCNQ was applied to WSe₂ to realize p-type channel doping. With p-type dopant in channel, the electron carrier density inside the WSe₂ channel is significantly reduced and electron branch is suppressed. Meanwhile, the Schottky barrier width for hole transport is reduced, which leads to the reduction of contact resistance and the enhancement of hole branch and on-current for pFETs. Figure 3d shows the Id−Vs characteristics of a typical WSe₂ p-type NC-FET with F4-TCNQ doping in 50 mV Vs step. This device has a channel length of 1 μm, and channel thickness of 6.1 nm, measured by AFM. The device exhibits SSB = 40.2 mV/dec, SSB = 57.5 mV/dec SS below 60 mV/dec at room temperature is demonstrated for both forward and reverse gate voltage sweeps, as shown in Figure 3f. SS of p-type NC-FET below the thermionic limit is the result of the negative capacitance effect. Meanwhile, a low hysteresis (defined as Vs difference at 1 pA/μm in Id−Vs characteristics) of 0.18 V is also obtained. Figure 3e shows Id−Vs characteristics of the same WSe₂ NC-FET as shown in Figure 3d. In conventional MOSFETs, the threshold voltage (Vth) shifts toward the negative direction as drain voltage. The drain-induced-bias-lowering (DIBL), defined as DIBL = −ΔVth/ΔVD, is usually positive. With ferroelectric gate stack, the DIBL effect could be reversed in NC-FETs.28,29 The negative DIBL effect originates from the negative capacitance coupling from drain to the interfacial layer between Al₂O₃ and HZO. NDR can naturally occur as a result of the negative DIBL effect because the positive drain voltage can induce negative charge into the channel. NDR is observed for both WSe₂ n-type NC-FET and p-type NC-FET, as shown in Figure 3c,e, indicating the effectiveness of the negative capacitance effect in ferroelectric HZO.

In conclusion, WSe₂ NC-FETs with ferroelectric HZO gate stack are demonstrated. Chemical doping of F4-TCNQ is applied to suppress the electron current in the off-state of p-type NC-FETs and to reduce the Schottky barrier width for holes. The doped devices exhibit steep-slope switching characteristics with less than 60 mV/dec for bidirectional sweeps. Sub-60 mV/dec SS (as low as 14.4 mV/dec) and negative DIBL effect conclusively confirm the realization of

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3685
negative capacitance effect in WSe$_2$ 2D-FETs with HZO as gate dielectric.

**ASSOCIATED CONTENT**

Supporting Information
The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b00816.

Additional details for transient RC measurement of ferroelectric HZO, statistical and cycling measurement of HZO MIM capacitor, gate stack leakage current, detailed numerical simulation, and modeling of enhancement by IMG (PDF)

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Author Contributions
P.D.Y. conceived the idea and supervised the experiments. M.S. did the device fabrication, DC electrical measurement and analysis. M.S. and W.C. did the P–E measurement. C.J. and M.A.A. conducted numerical simulation. M.S. and Y.D. performed the F4-TCNQ doping. M.S. and P.D.Y. cowrote the manuscript and all authors commented on it.

Notes
The authors declare no competing financial interest.

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