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Ultrathin transparent Copper(I) oxide films grown by plasma-enhanced atomic layer deposition for Back-end-of-line p-Type transistors

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Abstract

We demonstrate p-type thin-film transistors (TFTs) on copper(I) oxide (Cu_2O) grown by plasma-enhanced atomic layer deposition (PEALD) with bis(N,N′-di-sec-butylacetami-dinato)dicopper(I) as the Cu precursor and oxygen (O_2) plasma as an oxidant. PEALD provides many if the advantages of other ALD processes, including uniformity and conformality, but with the additional ability to actively generate reactants and to add substantial energy from the plasma which may be important in defect control, low-temperature deposition. In this letter, Cu_2O films were grown on SiO_2/Si substrates under different substrate temperatures (160 ∼ 240 °C) and post-deposition annealing was carried out under various temperatures (300 ∼ 1100 °C) to improve the growth rate and crystallinity of the Cu_2O films. The fabricated p-channel bottom-gate Cu_2O transistors with a controlled thickness of 12 nm have high transparency over 90% and exhibit a subgap density of states ($g(E)$) of 7.2×10^{18} $eV^{-1}\cdot cm^{-3}$ near the valence band (E_V), contact resistivity (R_C) of 14 kΩ·mm, I_{ON}/I_{OFF} ratio of 2×10^3, and field-effect mobility of 0.1 $cm^2/V\cdot s$.

1. Introduction

Cu_2O is regarded as one of the most promising materials for achieving p-type transition metal oxide (TMO) thin-film transistors (TFTs) [1–4]. Furthermore, to enable monolithic three-dimensional (M3D) integration of high performance logic, high mobility n-type and p-type oxide semiconductor thin films that can be utilized for fabrication of back-end-of-line (BEOL) compatible complementary metal oxide semiconductor (CMOS) circuits are strongly demanded [5–8]. Cu_2O is natively p-type owing to the presence of Cu vacancies, which introduce an acceptor level near valence band edge E_V [9]. Cu_2O itself has a cubic structure with a direct bandgap of 2.1 ∼ 2.5 eV [10]. Cu_2O films can formed by a variety of methods such as sputtering [11–13], spray coating [14], solution process [15], pulsed laser deposition [16], chemical vapor deposition [17], and thermal oxidation [18]. Among these deposition techniques, atomic layer deposition (ALD) is particularly suitable for oxide thin-film growth due to its conformal step coverage and accurate thickness control [19]. Although ALD-based Cu_2O studies have been extensively reported [20–24], the fabrication and performance of PEALD-based Cu_2O TFTs has not been demonstrated to date.

Above all, an oxygen plasma or ozone process can play an important role in the improvement of chemical reactivity and film growth rate, which is the limitation for ALD of Cu_2O [25].

In this work, we present p-type TFTs fabricated on Cu_2O ultrathin films grown by PEALD process for the first time. We characterized device electrical performance including R_C, $g(E)$, and μ_{FE} as well as material properties such as phase composition, energy bandgap, and transmittance of the fabricated Cu_2O TFTs, although the quality of the materials and device fabrication process need to be further improved.

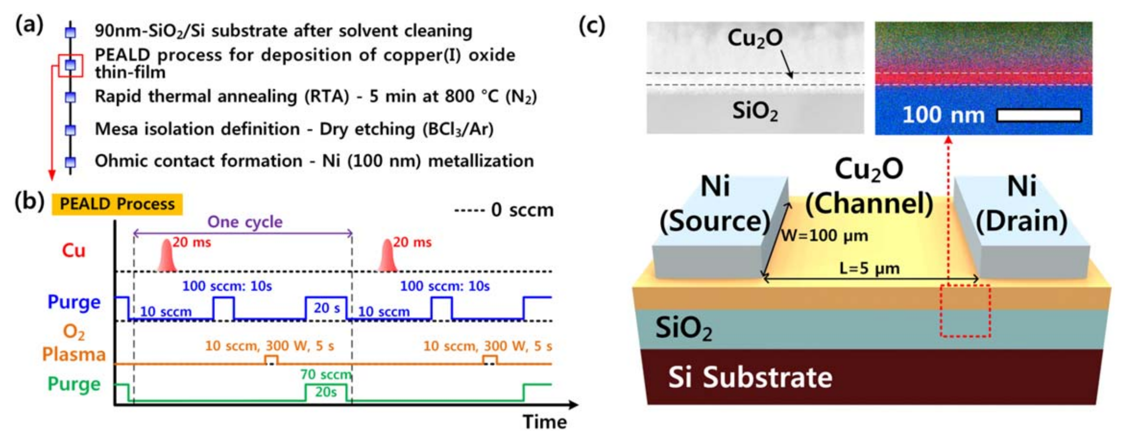

Figure 1. (a) Main fabrication process flow for the bottom-gate p-type Cu_2O TFTs. (b) Schematic diagram of the PEALD deposition cycle of Cu_2O film with bis(N,N′-di-sec- butylacetamidinato)dicopper(I) as the Cu precursor and O_2 plasma as an oxidant (c) STEM and the corresponding EDS images of the ultrathin Cu_2O film on the SiO_2/Si substrate and schematic image of the fabricated device.

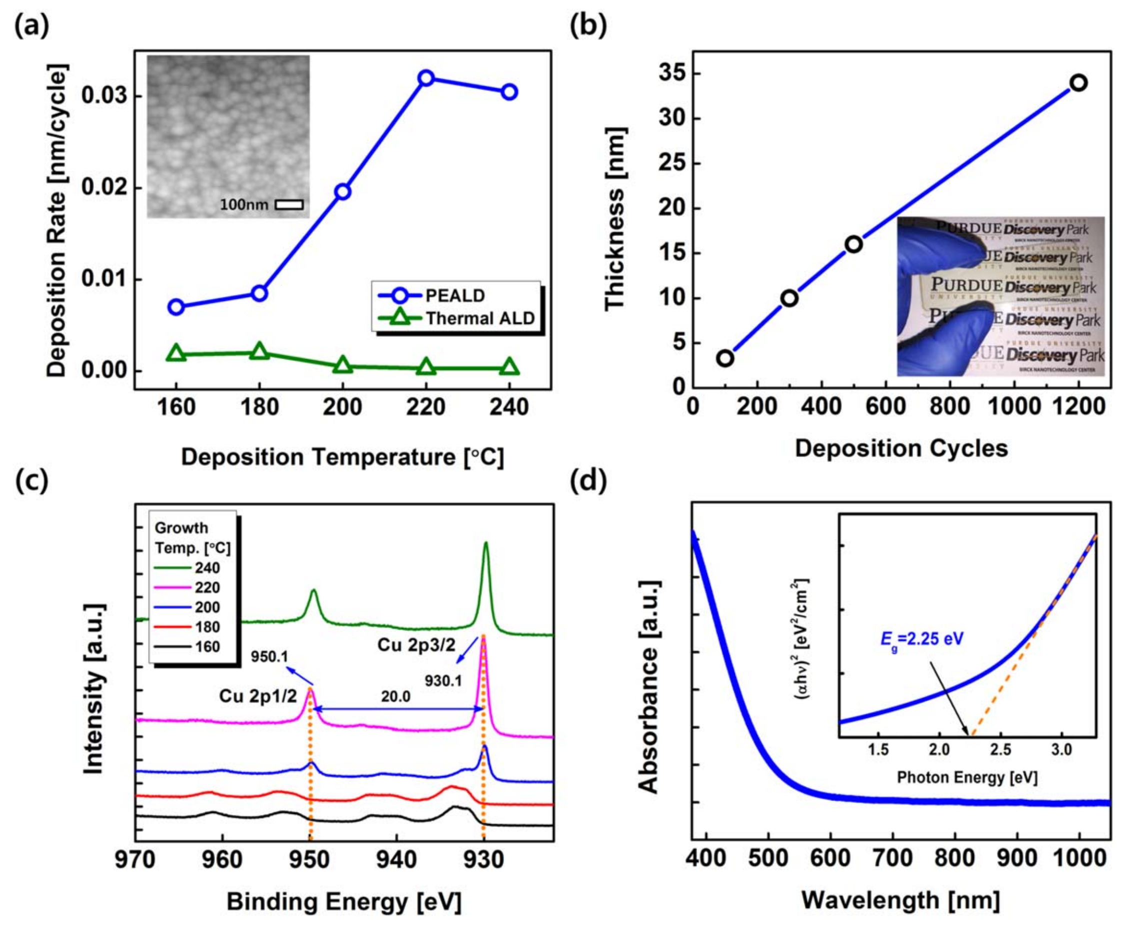

Figure 2. The growth rate per cycle of Cu_2O film by PEALD with (a) substrate temperature (inset: image of as-dep Cu_2O film) and (b) deposition cycles (inset: image of transparent ultrathin Cu_2O film on glass substrate). (c) Cu 2p3/2 and Cu 2p1/2 peaks for the deposited Cu_2O film at various substrate temperatures. (d) The measured absorption spectra and optical bandgap (inset).

2. Experiment

Figure 1(a) shows the key fabrication steps for the bottom-gate p-type Cu_2O TFTs on SiO_2/Si substrates using the newly developed PEALD process. The Cu_2O channel material was deposited by PEALD on SiO_2 (90 nm)/ p + Si wafer, which was functioned as a bottom-gate. In this study, we used bis(N,N′-di-sec-butylacetamidinato)dicopper(I)[Cu(^{5}Bu-Me-amd)]$_2$ as the Cu precursor [20]. The Cu precursor with the solid phase was

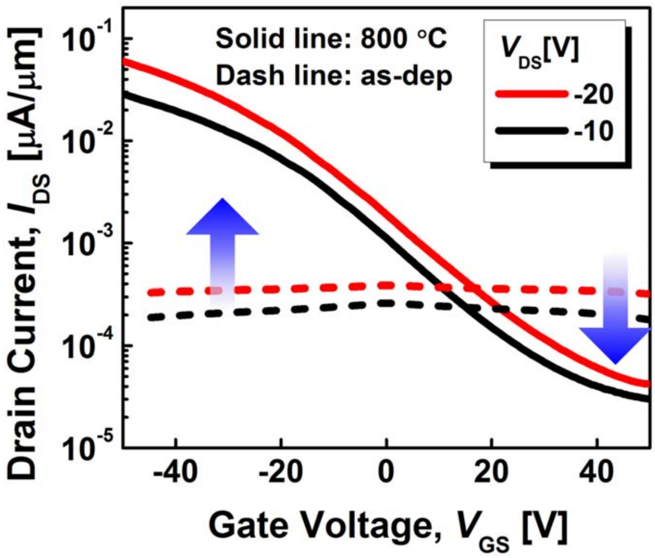

Figure 3. Measured I_{DS}–V_{GS} transfer characteristics of the fabricated bottom-gate Cu_2O TFTs with as-deposited (dashed line) and post-annealed (solid line) Cu_2O film at drain voltage (V_{DS}) = −10 and −20 V.

supplied by STREM, a company that produces a variety of high quality precursors for ALD process. As shown in figure 1(b), the optimized process consists of a Cu-precursor pulse for 20 ms with a 10 sccm N_2 flow, a purge pulse of 10 s with 100 sccm of N_2 flow, an O_2 plasma pulse for 5 s with 10 sccm under a plasma power of 300 W, and a purge pulse of 20 s with both 70 sccm of N_2 flow in main chamber and 100 sccm of N_2 flow in the plasma gas line. Next, rapid thermal annealing (RTA) at 800 °C was carried out under N_2 atmosphere for 5 min.

To define the Cu_2O channel region, we carried out mesa isolation using a BCl_3/Ar gas mixture in an inductively coupled plasma-reactive ion etching (ICP-RIE) system (Panasonic E620 Etcher) for 5 min. The etching rate of Cu_2O film is about 4 nm min^{-1} under the process conditions used: RF power of 100 W; BCl_3 flow of 15 sccm; Ar flow of 60 sccm; pressure of 0.6 Pa. Subsequently, Ni with a thickness of 100 nm was deposited for formation of source (S) and drain (D) contacts via an electron beam evaporator. A schematic view of the p-type Cu_2O TFTs with the bottom-gate structure is shown in figure 1(c). The fabricated device has the channel width (W) of 100 μm and length (L) of 5 μm.

3. Results and discussion

To increase the deposition rate and conductivity of the atomic layer deposited (ALD) Cu_2O film, we employed PEALD process under various conditions. Figure 2(a) shows the dependence of deposition rate on deposition temperature from 160 to 240 °C. The deposition rate rapidly increases with increasing deposition temperature until 220 °C. As shown in figure 2(b), a growth per cycle (GPC) of 0.33 Å was found for a substrate temperature of 220 °C. The inset of figure 2(b) shows a PEALD-grown transparent Cu_2O film with a thickness of 12 nm on a glass substrate. Figure 2(c) shows X-ray photoelectron spectroscopy (XPS) spectra of as-deposited Cu_2O films with various deposition temperatures between 160 to 240 °C. All the samples grown between 200 to 240 °C showed the characteristic Cu 2p3/2 and Cu 2p1/2 peaks at 950.1 and 930.1 eV, respectively. Figure 2(d) shows the high measured absorption spectra of the Cu_2O film, resulting in a high transparency of approximately 90%, corresponding to an optical band gap of 2.25 eV. Figure 3 presents the gate-voltage (V_{GS}) dependent drain-source current (I_{DS}) characteristics of the fabricated bottom-gate Cu_2O TFTs after post-deposition annealing with a temperature of 800 °C, in contrast to those measured from the as-deposited films.

The measured I-V data show that the fabricated devices demonstrate clear p-channel behaviour with an increase of I_{DS} for negative V_{GS}. The I_{ON}/I_{OFF} ratio and $I_{DS,MAX}$ with the as-deposited film and with various annealing temperatures are summarized in table 1. Although I_{OFF} caused by defects and minority carriers (electrons) [26] should be improved, we note that the fabricated device with Cu_2O film annealed at 800 °C exhibits the highest I_{ON}/I_{OFF} ratio and $I_{DS,MAX}$ while the fabricated devices annealed at other temperatures have relatively poor electrical performance. It is noteworthy that high temperature annealing after film deposition gives rise to an improvement in film crystallinity and a reduction of copper vacancies in band tail states near E_V

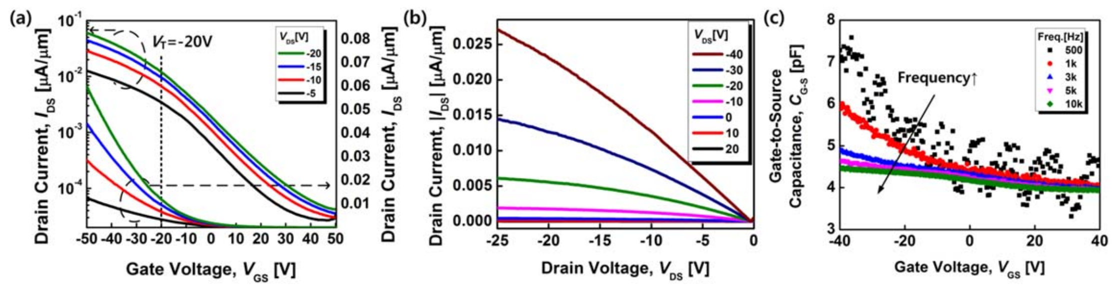

Figure 4. (a) Measured I_{DS}–V_{GS} transfer characteristics at various V_{DS} conditions. (b) V_{GS}-dependent I_{DS}–V_{DS} output characteristics of the fabricated bottom-gate Cu_2O TFTs. (c) The measured C–V curves with various frequencies ($f = 0.5 \sim 10$ kHz).

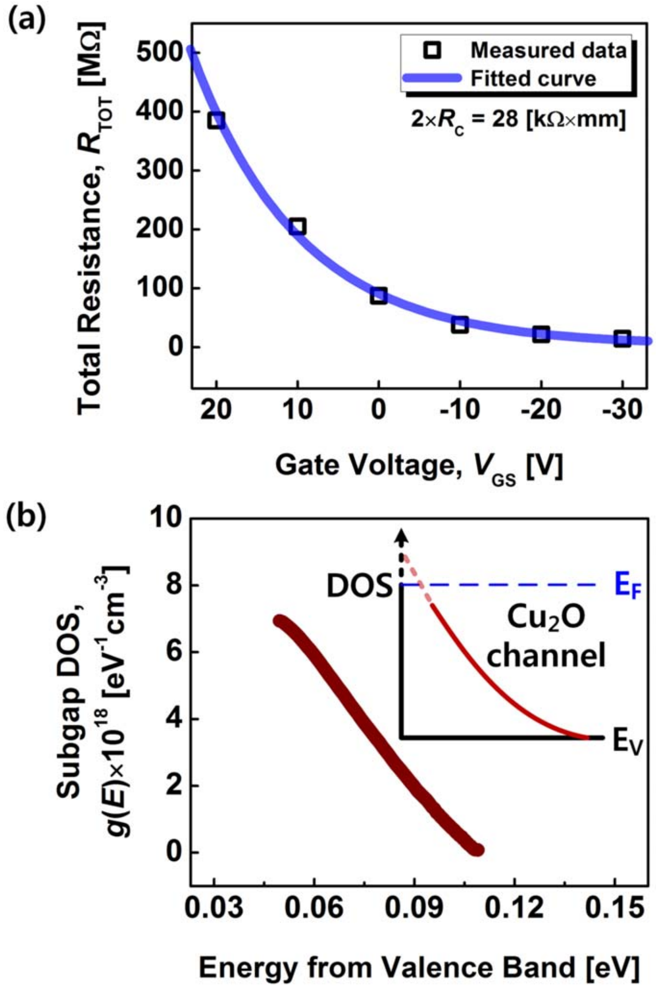

Figure 5. (a) V_{GS}-dependent $R_{TOT}(V_{GS})$ and extrapolated R_C. (b) Energy distribution of extracted subgap DOS ($g(E)$) near E_V.

Table 1. Device parameters with various post-deposition annealing temperatures.

@$V_{DS} = -20$ V	I_{ON}/I_{OFF}	$I_{DS,MAX}$ [μA μm^{-1}]
As-dep	—	2×10^{-4}
700 °C	~9×10^{1}	3×10^{-2}
800 °C	**~2×10^{3}**	**6×10^{-2}**
900 °C	~5×10^{1}	4×10^{-2}

[12]. The measured I_{DS}–V_{GS} transfer and I_{DS}–V_{DS} output characteristics of the fabricated bottom-gate Cu_2O TFTs are shown in figures 4(a) and (b), respectively.

Furthermore, the capacitance between the gate and the short circuited S/D in the p-channel Cu_2O TFT under the accumulation mode was characterized using an Agilent E4980A precision LCR meter. The frequency dependent capacitance-voltage (C-V) characteristics over the frequency range from 500 Hz to 10 kHz for the gate-to-source/drain configuration are shown in figure 4(c). Also, the measured capacitance value increases as V_{GS} increases in the negative direction. The results show the clear evidence for hole accumulation in the Cu_2O film ($V_{GS} < 0$). Especially, large frequency dispersion is attributed to capture-emission events occurring in both oxide bulk and interface with a contribution of large contact resistance (R_C) in S/D regions.

The R_C is obtained from extrapolated V_{GS}-dependent total series resistance ($R_{TOT}(V_{GS})$) as presented in figure 5(a). In the fabricated p-type Cu_2O TFTs, a quantitative analysis of the $g(E)$ over the bandgap is a significant issue when estimating the device instability which can be affected by film quality [27]. As shown in figure 5(b), we obtained $g(E)$ of 7.2×10^{18} eV^{-1} cm^{-3} over the subgap energy ranges using V_{GS}-dependent ideality factor obtained from the subthreshold region of the measured I_{DS}–V_{GS} curve [28]. Although we successfully demonstrated the fabrication and performance of PEALD Cu_2O TFTs, there still remain challenges in achieving higher mobility, better switching behaviors, and lower R_C in ultrathin p-type Cu_2O films. These issues are generally observed in the reported work related to p-type oxide transistors [11–16, 22]. More comprehensive study in particularly related to film growth and further device development are still under way.

4. Conclusion

In this work, we have developed a PEALD process to produce p-type Cu_2O films and demonstrated bottom-gate TFTs. P-type Cu_2O films are an important material building block for TMO-based BEOL transistors and circuits. The deposited Cu_2O thin-films with 12 nm thickness exhibited a high transparency of approximately 90%. Through post-deposition annealing at a temperature of 800 °C, the Cu_2O TFTs have a lower OFF-state current and a larger I_{ON}/I_{OFF} current ratio of 2×10^3. These ultrathin and transparent Cu_2O TFTs fabricated with PEALD process could be a promising candidate for key devices for BEOL transistors in the hyper-scaled transistor era.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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