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Improvement of GaAs metal–semiconductor field-effect transistor drain–source breakdown voltage by oxide surface passivation grown by atomic layer deposition

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Abstract

Oxide surface passivation grown by atomic layer deposition (ALD) has been applied to GaAs metal–semiconductor field-effect transistors (MESFETs). The breakdown characteristic of a MESFET is greatly improved by both Al_2O_3 and HfO_2 passivation. Three-terminal transistor breakdown voltage is improved to a maximum level of 20 V with Al_2O_3 passivation from 11 V without any surface passivation. With the removal of native oxide and passivation on GaAs surface at drain–gate (D–G) and source–gate (S–G) spacings, the device breakdown characteristics are significantly improved.
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1. Introduction

Passivation of the III–V compound semiconductor surface continues to be one of the most difficult problems. The surface imposes many constraints in the design of all types of III–V compound semiconductor photonic and electronic devices. Unlike the electrically passive Si–SiO_2 interface, III–V compound semiconductor passivation technology is still under active development. In general, two types of passivation technologies, chemical surface treatment [1–4] and dielectric deposition [5–9], are widely used in the III–V compound semiconductor field. For examples, the chemical passivation using sulfidation and/or hydrogenation is often applied to InP-based devices [10–12], and the dielectric passivation is critical to the performance of GaN-based power devices [13,14].

Surface passivation of GaAs metal–semiconductor field-effect transistors (MESFETs) attracts much interest to improve the device performance. For example, surface passivation is of great importance to achieve high power and good stability in GaAs power MESFETs. Besides sulfur passivation, deposition of different dielectrics, e.g., PECVD Si_3N_4 and SiO_2, and growth of epitaxial passivation films, e.g., low-temperature-grown GaAs [6] and MBE $Ga_2O_3(Gd_2O_3)$ [8], have been widely studied recently. The improvement of the device performance, e.g., breakdown voltage, has been widely observed in different material systems [4,9,15,16]. But some device simulations and experiments suggest that the breakdown voltage decreases with surface passivation [17–23]. More studies, especially on different passivation materials and approaches, are called for to clarify these contradictory

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results. Inspired by our recent work on GaAs MOSFETs using atomic layer deposition (ALD) grown oxide as gate dielectric [24,25], we apply ALD oxide layer as a new type of dielectric passivation on GaAs MESFETs. In this paper, we study the breakdown voltage of GaAs MESFETs with ALD grown Al_2O_3 and HfO_2 films as passivation layers. 5–10 V improvement of breakdown voltage is widely observed in our passivated devices. The study is applicable to improve the device performance of GaAs power MESFETs. Meanwhile, MESFET is also used as a test vehicle to analyze the effectiveness of different treatments and passivation films on GaAs. It improves our understanding of oxide–semiconductor interface properties.

Al_2O_3 is a widely applied passivation material with a high bandgap of ∼9 eV and a dielectric constant of 8.6–10. HfO_2 is an intensively studied high-k material with a bandgap of ∼5 eV and a dielectric constant as high as 30. Both oxides have a high breakdown field (5–10 MV/cm), high thermal stability, and remain amorphous under typical processing conditions. ALD itself is an ex situ, robust manufacturing process which is already commonly used for high-k gate dielectrics in Si CMOS technology [26].

2. Experiments

Fig. 1 shows the device structure of the fabricated MESFET with ALD grown dielectric passivation. A 1500 Å undoped GaAs buffer layer and a 700 Å Si-doped GaAs layer ($4 \times 10^{17}/cm^3$) were sequentially grown by MBE on a (1 0 0)-oriented semi-insulating 2-in. GaAs substrate. Device isolation was achieved by oxygen implantation. Activation annealing was performed at 450 °C in a helium gas ambient. Ohmic contacts were formed by e-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 435 °C anneal in a forming gas ambient. Finally, Ti/Au metals were e-beam evaporated, followed by lift-off to form the gate electrodes. The gate length varied from 0.65 to 40 μm, while the exposed source-to-gate (S–G) and the drain-to-gate (D–G) spacings were the same (∼0.75 μm) at each device. The sheet resistance of the channel and its contact resistance, measured by the transfer length method (TLM) on the same wafer, were 1.3 $k\Omega/\square$ and 1.5 Ω mm. The whole completed wafer was cleaved into eight pieces to carry out different pre-cleaning and passivation process as listed in Table 1. It includes HCl dip cleaning and/or 10 min ozone plasma cleaning. After pre-cleaning, the samples were transferred immediately to an ASM Pulsar2000™ ALD module. A 200 or 250 Å thick Al_2O_3 or HfO_2 oxide layer was deposited at a temperature of 300 °C. The TEM image illustrates the ALD grown oxide having an abrupt interface with the GaAs substrate as shown in the inset of Fig. 1. The oxide thickness between 100 and 300 Å is essential for balance of passivation stability and being easily pinched through by probes during measurement. In practice, if the oxide thickness is above 500 Å, the Al_2O_3 overlayer can be selectively wet etched by diluted HF solution and HfO_2 overlayer can be dry etched away by BCl_3.

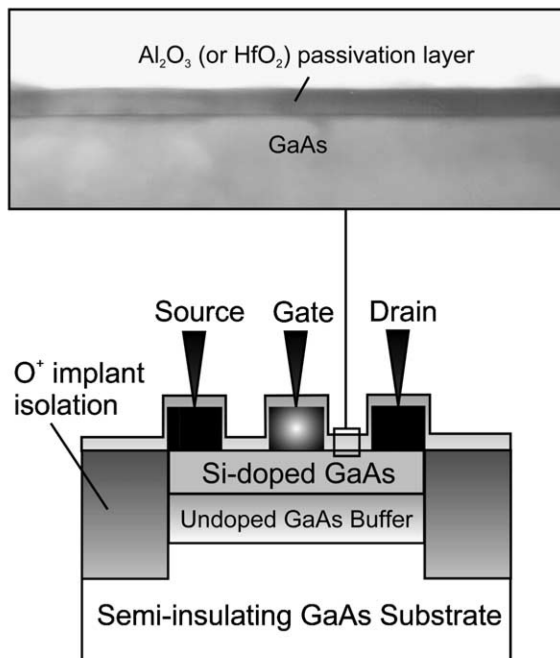

Fig. 1. Schematic view of a GaAs MESFET with ALD-grown oxide as a passivation layer. By measurement, the thin oxide layer covered on the drain, source, gate regions is simply pinched through by probes. Inset: TEM image of Al_2O_3 passivated GaAs surface.

Table 1
Device parameters of GaAs MESFETs on different treatment

		Breakdown voltage V_{br} (V)
#1	200 Å Al_2O_3 passivation	20
#2	10 min ozone clean and Al_2O_3 passivation	15
#3	HCl cleaning and 200 Å Al_2O_3 passivation	13–15
#4	HCl cleaning, 10 min ozone cleaning, and 250 Å Al_2O_3 passivation	13–15
#5	200 Å HfO_2 passivation	15
#6	HCl cleaning and 200 Å HfO_2 passivation	13–15
#7	HCl cleaning unpassivated	10
#8	No cleaning unpassivated	11

3. Results and discussion

Fig. 2(a) shows the I–V curves of Al_2O_3 passivated MESFET with the gate length of 0.75 μm. The gate voltage is varied from −1.0 V to +0.6 V with 0.2 V step. The fabricated device has a pinch-off voltage of −1.0 V. The maximum drain current density I_{dss}, measured at

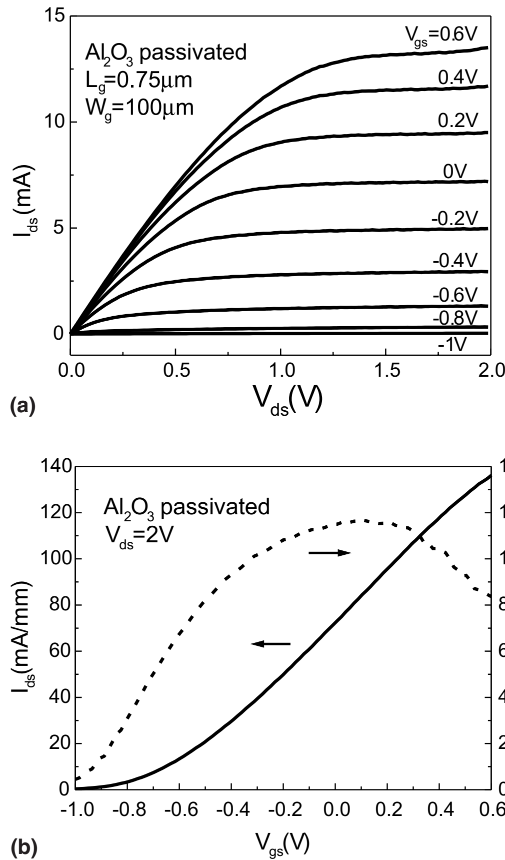

Fig. 2. (a) Drain current vs. drain bias as a function of gate bias of an Al_2O_3 passivated MESFET. (b) Drain current vs. gate bias (solid line) and transconductance vs. gate bias (dashed line) at the saturation region.

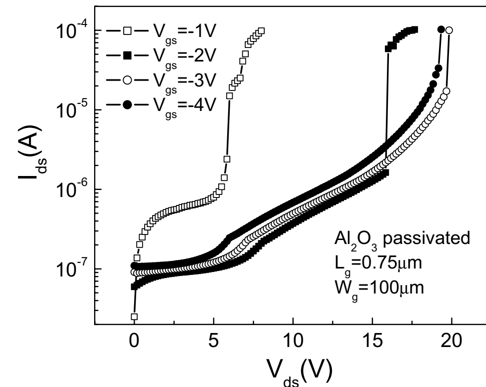

Fig. 3. The drain breakdown characteristics of an Al_2O_3 passivated MESFET as a function of gate biases at a fully pinched-off condition.

V_{gs} = +0.6 V, is ~140 mA/mm. The knee voltage is ~0.85 V at V_{gs} = +0.6 V . Fig. 2(b) illustrates the drain current density as a function of gate bias in the saturation region. The device shows almost linear relation of I_{ds} vs. V_{gs} in the wide bias range. The slope of the drain current shows that the maximum transconductance of this type of MESFETs at L_g = 0.75 μm is typically ~120 mS/mm. The general performances of the devices at low V_{ds} (~3 V) are similar with or without passivation. For example, the variation of I_{dss} is less than 5%. Since the breakdown characteristics between drain and gate is a prerequisite in developing a GaAs power MESFET, in this paper, we focus on just one device parameter, the off-state three-terminal drain–source breakdown voltage V_{br}, as a function of different precleanings and passivations to search for the best passivation approach for a MESFET power device. Here, V_{br} is defined as the value of V_{ds} for a drain current I_{ds} of 1 mA/mm at the pinch-off state.

The drain breakdown characteristics of Al_2O_3 passivated MESFETs as a function of gate bias at fully pinched-off condition are shown in Fig. 3. The curves are taken sequentially from V_{gs} = −1 V to −4 V by setting the maximum I_{ds} = 0.1 mA to avoid catastrophic breakdown of the device. At V_{gs} = −1 V (pinch-off voltage), I_{ds} is lower than 1 μA with V_{ds} < 5 V. I_{ds} dramatically increases once V_{ds} > 5 V. We ascribe this to the source/drain punch-through via the undoped buffer layer (background p^- doping of ~10^{15}/cm^3 in our samples). Once the gate is further biased as −2 to −3 V to deplete the channel, V_{br} increases to 16–20 V and the remnant channel current reduces to 10–100 nA at V_{ds} < 5 V. The more negative gate bias also helps to fix the potential at the p^- buffer layer underneath the gate to prevent the punch-through effect. V_{br} sets back to ~19 V when V_{gs} is further negatively biased to −4 V. This is because of the breakdown of the reverse junction near the drain-edge of the Schottky-contact gate. Using this scheme with smaller steps as ΔV_{gs} = 0.5 V, we can find the gate bias condition for the maximum V_{br}. Here V_{br} is not the highest value reported in MESFETs, because no lightly doped drain or field plate design are incorporated here. Note that in general V_{br} mainly depends on the channel doping and the D–G spacing. The D–G spacing here is only 0.75 μm, much shorter than 2–3 μm, the typical D–G spacing for GaAs power MESFETs. The temperature dependence measurements show that V_{br} drop 20% in average with increased temperatures from 25 °C to 150 °C.

Fig. 4 presents the drain breakdown characteristics on three identical MESFETs with Al_2O_3 passivation, HfO_2 passivation and a reference without passivation. V_{br} is significantly improved from 11 V for MESFET without any treatments and passivations, to ~20 V with Al_2O_3 passivation. The distribution of V_{br} values over 40 devices of three groups is shown in Fig. 5. The three groups of devices are with Al_2O_3, HfO_2 passivations, and without any passivation as a reference. Each group has more than 10 devices. The gate length of all the devices is 0.75 μm. There is no clear evidence that V_{br} is dependent on the gate length in our experiment. It is consistent with the physical picture that the breakdown of the MESFET is the result of a higher electric field

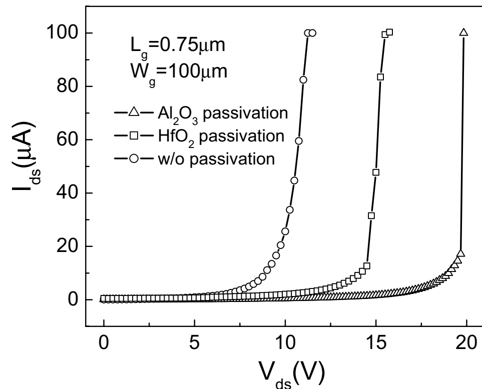

Fig. 4. The drain breakdown characteristics of Al_2O_3 and HfO_2 passivated MESFETs and a MESFET without any passivation or treatment as a reference at a fully pinched-off condition ($V_{gs} = -3$ V).

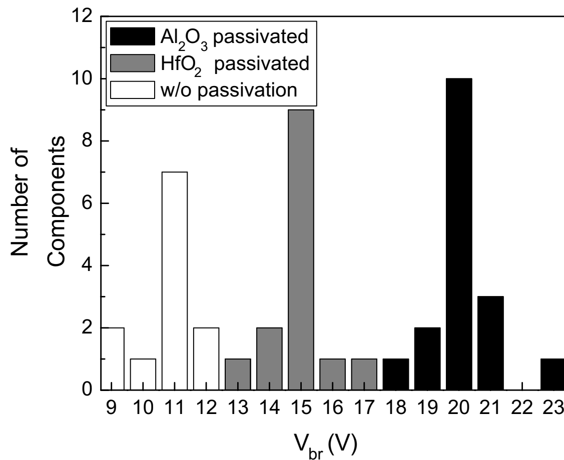

Fig. 5. Average V_{br} for three different types of MESFETs across a 2-in. wafer.

near the drain-edge of the Schottky-contact gate. The data provide decisive conclusion that Al_2O_3 is more suitable for MESFET passivation to improve device breakdown performance. MESFET V_{br} measurements also indicate that Al_2O_3 on GaAs could form a better passivation layer or interface than HfO_2 on GaAs. The naïve understanding is that Al is III-group element and very chemically active, and can replace any Ga vacancies. For examples, AlAs is lattice-matched to GaAs. AlGaAs/GaAs heterojunction is the most widely used material combination in III–V compound semiconductors. It could be related with the fact that Al_2O_3 has superior passivation effect on GaAs than HfO_2. In fact, this point is also verified by our MOS capacitance measurements, which shows the interface of Al_2O_3/GaAs has lower interface trap density than that of HfO_2/GaAs.

Table 1 lists the breakdown voltages of MESFETs for various surface pre-clean treatments and passivations. Sample #1, the finished devices with direct Al_2O_3 passivation, shows the best V_{br} so far. Samples #2–#4, the devices with HCl pre-cleaning and/or ozone plasma cleaning before Al_2O_3 passivation, show inferior breakdown characteristics compared to Sample #1. The same holds for Samples #5–#6 with HfO_2 passivation showing smaller V_{br}. But all of devices with passivation in general show higher breakdown voltages than those without any passivations as reference Samples #7–#8. It is well-known that native oxides exist at normal GaAs surface, which result in various recombination centers and a large number of bound surface charge. After ALD passivation, especially in the Al_2O_3 passivation case, the native oxide and excess As can be removed, resulting in a high quality Al_2O_3/GaAs interface. The surface studies, i.e., medium energy ion scattering (MEIS), high resolution TEM, and atomic level chemical bond analysis [27] confirm the above point. The above experiments demonstrate that the listed straightforward pre-cleaning processes do not further improve the interface quality. To search for a suitable pre-cleaning process is still an open topic. The improved breakdown performance after passivation can be interpreted by the following possible mechanisms. First, the removal of native oxide by ALD process eliminates the weakest source of surface breakdown, thus could improve the device breakdown performance. Second, it is widely recognized that the highest electric field on GaAs MESFET in the breakdown region is near the drain-edge of the Schottky-contact gate. Device simulations *considering passivation materials* [15] shows that the field lines in the passivated MESFET are more widely spread over the gate and are less crowded at the edge of the gate compared to the unpassivated MESFET. This is another possible reason that the breakdown voltage of the passivated MESFET is higher. Third, if the surface or interface traps were donor-type, reduced trap density by passivation would lead to more positive charges existing on the surface, thus increased surface potential and increased breakdown voltage. The surface or oxide trapped charges can also produce the effect to defocusing the electrical field near the drain-edge of the gate, which has the same effect as the widely used field plates in power devices. More studies to determine the interface trap properties could clarify the puzzle of these controversial experimental results [4,9,15–23].

4. Conclusions

In summary, we have demonstrated that both ALD-grown Al_2O_3 and HfO_2 passivation on the S–G and D–G spacings of MESFETs can significantly improve the breakdown characteristics of the devices. The results demonstrate that Al_2O_3 passivation without pre-cleaning yields the best performance and the Al_2O_3/

GaAs interface is of high quality as passivation. These results are particularly critical for power devices.

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References

[1] Sandroff CJ, Nottenburg RN, Bischoff JC, Bhat R. Appl Phys Lett 1987;51(1):33–5.
[2] Yokoi N, Andoh H, Takai M. Appl Phys Lett 1994; 64(19):2578–80.
[3] Fukuda Y, Suzuki Y, Sanada N, Shimomura M, Masuda S. Phys Rev B 1997;56(3):1084–6.
[4] Kang M, Park H, Kim H. Appl Phys Lett 2002;80(14):2499–501.
[5] Charache GW, Akram S, Maby EW, Bhat IB. IEEE Trans Electron Dev 1997;44(11):1837–42.
[6] Chen C-L, Mahoney LJ, Manfra MJ, Smith FW, Temme DH, Calawa AR. IEEE Electron Dev Lett 1992;13(6):335–7.
[7] Wang Q, Yang ES, Li P-W, Lu Z, Osgood RM, Wang WI. IEEE Electron Dev Lett 1992;13(2):83–5.
[8] Hong M, Kwo J, Kortan AR, Mannaerts JP, Sergent AM. Science 1999;283:1897–900.
[9] Dong Y, Ding XM, Hou XY, Li Y, Li XB. Appl Phys Lett 2000; 77(23):3839–41.
[10] Lu ZH, Graham MJ, Feng XH, Yang BX. Appl Phys Lett 1992; 60(23):2773–5.
[11] Maeda F, Watanabe Y, Oshima M. Appl Phys Lett 1993; 62(3):297–9.
[12] Gallet D, Hollinger G. Appl Phys Lett 1993;62(9):982–4.
[13] Green BM, Chu KK, Chumbes EM, Smart JA, Shealy JR, Eastman LF. IEEE Electron Dev Lett 2000;21(6):268–70.
[14] Lu B, Johnson JW, Kim J, Mehandru RM, Ren F, Gila BP, et al. Appl Phys Lett 2001;80(9):1661–3.
[15] Chen CL. IEEE Trans Electron Dev 1996;43(4):535–42.
[16] Chang EY, Cibuzar GT, Pande KP. IEEE Trans Electron Dev 1988;35(9):1412–8.
[17] Mizuta H, Yamaguchi K, Takahashi S. IEEE Trans Electron Dev 1987;ED-34(10):2027–33.
[18] Paccagnella A, Zanoni E, Tedesco C, Lanzieri C, Cetronio A. IEEE Trans Electron Dev 1991;38(12):2682–4.
[19] Barton T, Ladbrooke P. Solid-State Electron 1986;29:807–10.
[20] Trew RJ, Mishra UK. IEEE Electron Dev Lett 1991;12(10):524–6.
[21] Zaitlin MP. IEEE Trans Electron Dev 1986;33(11):1635–9.
[22] Heliodore F, Lefebvre M, Salmer G, El-sayed OL. IEEE Trans Electron Dev 1988;35(7):824–30.
[23] Wada Y, Tomizawa M. IEEE Trans Electron Dev 1988; 35(11):1765–70.
[24] Ye PD, Wilk GD, Kwo J, Yang B, Gossmann H-JL, Frei M, et al. IEEE Electron Dev Lett 2003;24(4):209–11.
[25] Ye PD, Wilk GD, Yang B, Kwo J, Chu SNG, Nakahara S, et al. Appl Phys Lett 2003;83(1):180–2.
[26] Wilk GD, Wallace RM, Anthony JM. J Appl Phys 2001; 89(10):5243–75.
[27] D.A. Muller, private communications.