Ultrathin InGaO Thin Film Transistors by Atomic Layer Deposition

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Abstract—In this letter, we report on scaled ultrathin (~3 nm) InGaO (IGO) thin film transistors (TFTs) by atomic layer deposition (ALD) under a low thermal budget of 250 °C. The ALD-derived IGO channels are In-rich, with In/Ga atomic ratio of ~86:14, providing a high electron mobility of ~28.6 cm²/V·s under a ultrathin thickness of 3 nm. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm channel length (Lch). The IGO TFTs with a Lch of 80 nm show well-behaved electrical characteristics including a high on/off current ratio (Ion/Ioff) of 1010, a low subthreshold swing (SS) of 92 mV/dec under VDS of 0.8 V. The negative- and positive-gate-bias-stress stability (NBS and PBS) of IGO TFTs are studied in both N2 and air ambient, where a remarkably high PBS stability can be observed. The negative Vth shifts during PBS and PBS test in N2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This work presents the first demonstration of high-performance IGO TFTs with a miniatured device dimension, showing the potential for back-end-of-line (BEOL)-compatible monolithic 3D integration.

Index Terms—Atomic layer deposition (ALD), thin film transistor (TFT), indium gallium oxide (IGO), reliability, back-end-of-line (BEOL).

I. INTRODUCTION

INDIUM-BASED oxides have made a great success in traditional back-plane display due to their decent mobility, good uniformity, excellent optical transparency [1], [2], [3], [4], [5]. The high mobility of these In-based oxides could be explained by the isotopically spread In orbits overlap each other, providing an effective electron percolation path [1], [2]. Thus, pure In2O3 provide the highest mobility among oxides but suffer from degenerate carrier concentration and rich oxygen vacancy defects, thereby leading to high off-current (Ioff) and device instability issues [2]. Doping In2O3 with other metal cation having a higher binding energy with oxygen has shown to be an effective method to resolve these issues in display applications [1], [2], [3], [4], [5]. Among these cation dopants, Ga with small radius, high ionic potential, and high bonding energy with oxygen is believed to be a strong oxygen binder and carrier suppressor to In2O3 [6], [7], [8], [9], [10], [11], [12]. In addition, crystalline Ga2O3 has similar edging-sharing octahedral structure as In2O3, thus the introduction of Ga would induce minimal distortions to In2O3 host structure and possibly maintain a high mobility. Some high-performance IGO TFTs has also been demonstrated in previous reports [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. However, these IGO TFTs were mainly aimed at display applications with channel thickness (Tch) larger than 1 μm and process temperature typically above 400 °C. The scaled IGO TFTs with low thermal budget have not yet been demonstrated.

Recently, intensive attention has been garnered on applying oxide semiconductors for back-end-of-line (BEOL)-compatible logic and memory applications towards monolithic 3D integration [21], [22], [23]. High-performance scaled InGaZnO [21], InWO [22], In2O3 [23] TFTs have been demonstrated. Despite their excellent electrical performances, the stability of these scaled TFTs have not been carefully examined yet. It is generally believed that the electron (de)trapping at interface causes the Vth instability during gate-bias-stress test [24]. However, the high-electric field in scaled TFTs may accelerate the defect generation, adding a new mechanism to the Vth instability. Furthermore, H2O and O2 from measurement environments should also be considered [25], [26].

In this work, we report on ultrathin (~3 nm) IGO TFTs by atomic layer deposition (ALD) within 250 °C. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm Lch. The IGO TFTs with a Lch of 80 nm exhibit an Ion/Ioff of 1010, a SS of 92 mV/dec under VDS of 0.8 V. The negative- and positive-gate-bias-stress stability (NBS and PBS) of IGO TFTs are studied in both N2 and air ambient, where a remarkably high PBS stability can be observed in both ambient. The negative Vth shifts during PBS and PBS test in N2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This work presents the first demonstration of IGO TFTs with a miniatured device dimension and high PBS stability, showing a great promise for BEOL monolithic 3D integration.

II. EXPERIMENT

Figure 1(a) illustrates the schematic of the IGO TFTs, where 40 nm Ni, 6 nm HfO2 and 3 nm IGO function as electrodes, dielectric, and semiconductor channel, respectively. The device fabrication process is largely similar to our previous work [23]. Briefly, an 8 nm Al2O3 was first deposited by ALD at 175 °C on the Si/SiO2 substrates to obtain a smooth surface. Then, 40 nm Ni bottom gates were deposited.
by e-beam evaporation, defined by photolithography. Next, 6 nm HfO$_2$ was deposited by ALD at 200 °C, followed by the deposition of 3 nm IGO by ALD at 225 °C. The IGO deposition started with one cycle of Ga$_2$O$_3$ followed by 10 cycles of In$_2$O$_3$, forming one super-cycle of the IGO growth (Fig. 1(b)). A longer pulse time were adopted for In$_2$O$_3$ cycle compared to that of Ga$_2$O$_3$ cycle due to a weaker reactivity of In precursor. The IGO thickness is linearly increased with super-cycle numbers with a growth rate of $\sim 1.25$ Å/super-cycle, confirming the ALD growth nature. Then, IGO mesas were formed by BCl$_3$/Ar dry etching. Finally, 40 nm Ni was deposited as source/drain contacts by e-beam evaporation, defined by electron beam lithography. The fabricated TFTs have a channel width (W$_{ch}$) of 2 μm and channel length ranging from 2 μm to 60 nm. These IGO TFTs were subjected to O$_2$ annealing for 1 min at 250 °C after fabrication. Mild oxidization was adopted to prevent the oxidization of Ni contact, which could still leave some oxygen defects in IGO channel. Figure 1(c) shows the cross-sectional TEM image of IGO TFTs, where the thickness of each layer could be confirmed. Top-view SEM image of a typical IGO TFTs with a L$_{ch}$ of 80 nm could be seen in Fig. 1(d). The high In/Ga atomic ratio of 86:14 was confirmed by XPS in Figs. 1(e)-(g), which is beneficial for achieving a high $\mu$$_{FE}$. Some N and C contamination can also be detected from XPS (not shown), which may come from the precursor ligand during growth.

**III. RESULTS AND DISCUSSION**

Figure 2(a) shows bi-directional transfer characteristics of IGO TFTs with L$_{ch}$ ranging from 2 μm to 60 nm under V$_{DS}$ of 50 mV. All TFTs exhibit similar switching behaviors including high I$_{on}$/I$_{off}$, steep SS, similar V$_{th}$, and negligible hysteresis, indicating its immunity to the short channel effects down to 60 nm, benefiting from the excellent electrostatic control using the ultrathin gate stack. Figure 2(b) presents the statistical results of transconductance (g$_{m}$) and I$_{on}$ of IGO TFTs as a function of L$_{ch}$ under V$_{DS}$ of 0.5 V and under maximum V$_{DS}$. (c) Transfer length method measurements of IGO TFTs. (d) Extracted contact resistance (R$_{C}$). IGO TFTs. The contact resistance (R$_{C}$) can be extracted from TLM analysis (Fig. 2(c)). A low R$_{C}$ value of $\sim 0.1$ Ω·mm can be obtained under a gate overdrive (V$_{GS}$−V$_{th}$) of 2 V in Fig. 2(d).

Figure 3(a) shows the extracted $\mu$$_{FE}$ of 28.6 ± 1.1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ from five TFTs with L$_{ch}$ of 2 μm. The oxide capacitance (C$_{OX}$) of 1.65 μF/cm$^2$ were used for the extraction. Figure 3(b) exhibits transfer curves of a representative IGO TFTs with L$_{ch}$ of 80 nm under various V$_{DS}$. An I$_{on}$/I$_{off}$ of 1.8 × 10$^{10}$ and a steep SS of 92 mV/dec can be observed under V$_{DS}$ of 0.8 V. The V$_{th}$ of $\sim 0.24$ V can be extracted from the linear extrapolation of transfer curve under V$_{DS}$ of 50 mV (not shown).

It is interesting to note that the hysteresis direction transit from clockwise to counterclockwise with increased V$_{DS}$ in Fig. 3(b). The clockwise hysteresis is generally explained by the electron-trapping at the interface while mobile positive ions could lead to a counterclockwise hysteresis [28].
Fig. 4. Evolution of transfer characteristics in log-scale of IGO TFTs with Lch of 80 nm under gate stress voltage (VG,STR) of (a) +2 V; (b) −2 V in N2 ambient; and (c) +2 V; (d) −2 V in air ambient for a stress time of 2000 s. (e) Schematic illustration of the environmental effects on the gate bias stability.

oxides are well known to be rich of oxygen vacancy, which should be the case for our IGO films. These oxygen vacancies could work as shallow donor, where its charge transition levels (neutral to +) should locate at the edge of or in the conduction band of IGO, so called “negative-U” defects [29]. The neutral oxygen vacancy (VN) could function as electron traps [30], explaining the clockwise loop at low VDS. Under high electric field, these VN defects could be ionized, releasing two electrons into conduction band and forming positive charged VO in the channel and at the interface (Fig. 3(b)), which lead to the counterclockwise loop. Negligible hysteresis is observed in bi-directional sweeps on long channel devices since the lateral electric field is much smaller. The corresponding output characteristics of the IGO TFT can be seen in Fig. 3(c), where a high Ion of ~600 μA/μm is achieved under a VDS of 0.8 V and a VGS-Vth of ~2 V, which is among the best values reported for oxide TFTs [21], [22], [23]. Note that the VDS is limited to 0.8 V for a stable device operation.

Gate bias stress stability tests were performed on the IGO TFTs with a Lch of 80 nm under gate stress voltage (VG,STR) of ±2 V in both N2 and air ambient at room temperature (Fig. 4(a)-(d)). During the stress test, the gate was biased at the given voltage while source and drain were grounded. The gate stress was interrupted to collect transfer curves under VDS of 50 mV with a short integration time to avoid recovery and a short delay of 1 ms between measurement and stress. A remarkably high PBS stability can be observed in both ambient, with marginal ∆Vth of ~60 mV in N2 and ~21 mV in air. For NBS test, TFTs show more pronounced negative ∆Vth of ~848 mV in air compared to that of ~398 mV in N2. The differences between air and N2 ambient can be explained by the H2O adsorption/desorption process related to surface contamination such as C and N [31], which could not be removed by resting in N2.

In summary, we report on ultrathin IGO TFTs enabled by ALD under a low temperature of 250 °C. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm. The IGO TFTs with a Lch of 80 nm exhibit Ion/Ioff of 1.8×10^10, SS of 92 mV/dec, and high PBS stability in both N2 and air ambient. The negative Vth shifts during PBS and NBS test in N2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This study demonstrates that ALD IGO TFTs have the potential for BEOL monolithic 3D integration.

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