Few-Layer Black Phosphorus PMOSFETs with BN/Al₂O₃ Bilayer Gate Dielectric: Achieving $I_{on}=850\mu A/\mu m$, $g_m=340\mu S/\mu m$, and $R_c=0.58k\Omega \cdot \mu m$

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Abstract—In this paper, high-performance few-layer black phosphorus (BP) PMOSFETs have been demonstrated by using MOCVD BN and ALD Al₂O₃ as the top-gate dielectric as well as the passivation layer. Highest $I_{on}$ of 850µA/µm ($V_{ds} = -1.8V$) and $g_m$ of 340µS/µm ($V_{ds} = -0.8V$) have been achieved with the 200nm channel length ($L_{ch}$) devices. Record low contact resistance ($R_c$) of 0.88kΩ·µm has been obtained on BP transistors by contact engineering. The gate leakage of the BN/Al₂O₃ bilayer gate dielectric is less than $10^{-12}A/µm^2$ ($V_g = -1V$) with an EOT of 3nm. SS and hysteresis voltage as low as 70mV/dec and 0.1V have been achieved, indicating a high quality interface between BP and BN.

I. INTRODUCTION

BP is an exceptional two-dimensional (2D) material for high-performance transistor applications due to its excellent transport properties: i) intrinsically high electron and hole mobilities, i.e., hole mobility as high as 300-1000cm²/Vs at room temperature [1,2]; ii) direct bandgap semiconductor with the bandgap of 0.35-2.0eV depending on the number of layers, which can find wide applications in electronics and photonics [3,4]. However, the device performance of BP PMOSFETs such as $I_{on}$, $g_m$, EOT, and $R_c$ in literature are still far below what is expected due to the instability of BP in ambient reacting with O₂ and/or H₂O [5,6].

In this work, a bilayer gate dielectric of 1.6nm MOCVD sp²-BN and 1.3nm ALD Al₂O₃ was used to passivate the BP channel from oxidation. Compared with un-passivated devices, the passivated devices showed significant performance improvement. Hysteresis as low as 0.1V and SS as low as 70mV/dec are achieved. Record high $I_{on}$ of 850µA/µm ($V_{ds} = -1.8V$) and $g_m$ of 340µS/µm ($V_{ds} = -0.8V$) have been demonstrated with a 200nm $L_{ch}$ device. The gate leakage is less than $10^{-12}A/µm^2$ ($V_g = -1V$) with an EOT of 3nm. Meanwhile, $R_c$ as low as 0.58 kΩ·µm has also been demonstrated by contact engineering. It is shown that BN/Al₂O₃ is a high quality and scalable gate dielectric as well as an effective passivation layer for BP.

II. EXPERIMENT

Fig. 1 shows the schematic diagram of a BP MOSFET with BN/Al₂O₃ as gate dielectric. A top view SEM image of two connected100nm $L_{ch}$ BP MOSFETs is shown in Fig. 2(a). Fig. 2(b) shows the element analysis along the gate stack direction, namely AA’ in Fig. 1. Fig. 3 illustrates the STM image of 4.5nm by 4.5nm freshly cleaved BP surface with 0.3V scanning bias showing the puckered structures with atomic resolution. The detail of fabrication is shown in Fig. 4. The sp³-BN was grown by MOCVD at 1050°C on 1/4 2'' sapphire wafers. The thickness of BN on sapphire is less than 0.1nm and the film thickness is ~1.6nm measured by AFM, as shown in Fig. 5(a) and (b). Bulk BP was synthesized from red phosphorus using SnI₄/Sn as catalyst in sealed ampoules. Firstly, PMMA A10 and PDMS were coated on BN/sapphire wafers. The sapphire substrate was peeled after a few hours’ soak in BOE. BP flakes (thickness of 4-12 nm) were exfoliated onto a 90nm SiO₂/p⁺⁺ Si substrate. The PDMS/PMMA/BN film was transferred to the substrate after baking at 120°C for 30 minutes. The processes of BP exfoliation and BN transfer were all performed in a glovebox with H₂O and O₂ concentration less than 0.5ppm. The sample was baked at 100°C for 30 minutes to improve the adhesion between BP and BN. PMMA and PDMS was removed by solvent cleaning followed by N₂ annealing at 180°C. After Source/Drain pattern, an optional low power O₂/Ar plasma etching was used to open the BN windows at the S/D regions. The samples were immediately loaded into a metallization chamber after etching. 5nm Pt/ 8nm Ni/ 30nm Al or 12nm Ni/ 30nm Al was deposited as the contact metals. Fig. 6 shows a cross-sectional TEM image of the S/D region with BN etched. After metal lift-off, 1.3nm Al₂O₃ was deposited with ALD at 200°C. Finally, 10nm Ti/50nm Au was deposited as the top gate metal.

All patterns were defined with a VISTEC VB6 UHR e-beam lithography. Dry etching was performed with a Panasonic E620 high density plasma etcher. A HORIBA LabRAM HR800 Raman spectrometer was used for the Raman measurement with a 632.8nm wavelength He-Ne laser. All the devices were measured with a Keithley 4200 semiconductor parameters analyzer at room temperature.

III. RESULTS AND DISCUSSION

BP has anisotropic hole mobilities as the hole effective mass of armchair direction is 6-8 times larger than that of zigzag direction from DFT calculation [1]. Consequently, the armchair direction is identified with polarized Raman spectra and used as the channel direction for all devices, as shown in Fig. 7(a). Fig. 7(b) shows the time dependence of integrated intensity of A₁g Raman mode of BP samples without BN, with BN, and with
BN/Al$_2$O$_3$, respectively. Laser illumination is used to accelerate the degradation of BP [7]. Exposed in air, the normalized A$^{1g}_g$ Raman intensity of the freshly cleaved BP flake decreases exponentially within one hour, indicating its fast degradation in ambient. The degradation speed slows down when it is covered by BN only. Interestingly, no sign of degradation is observed when BP is covered by BN and Al$_2$O$_3$ with EOT of 3nm thick. It is shown that BN/Al$_2$O$_3$ bilayer dielectric can effectively suppress the degradation of BP in ambient.

Fig. 8 (a) shows the C-V characteristics of 1.6nm BN and 6nm Al$_2$O$_3$. The extracted relative dielectric constant of the MOCVD BN is about 3.0, which is in agreement with the reported dielectric constant of CVD BN [8]. In Fig. 8 (b), the leakage current density of the 1.6nm BN/1.3nm Al$_2$O$_3$ gate dielectric is less than 10$^{-12}$A/μm$^2$ at $V_g$ = -1V, which is comparable to SiO$_2$ with the same EOT.

Typical transfer curves of a back-gate (7.5nm HfO$_2$) BP transistor without any passivation techniques are shown in Fig. 9. The I-V hysteresis is as large as 2.5V [Δ$V_{th}$] and comparable to SiO$_2$-12 transistor without any passivation techniques are shown in Fig. 10. The extracted relative dielectric constant of the MOCVD BN is about 3.0, which is in agreement with the reported dielectric constant of CVD BN [8]. In Fig. 8 (b), the leakage current density of the 1.6nm BN/1.3nm Al$_2$O$_3$ gate dielectric is less than 10$^{-12}$A/μm$^2$ at $V_g$ = -1V, which is comparable to SiO$_2$ with the same EOT.

Record high $I_{on}$, $g_m$, $R_c$, and $I_{off}$/EOT have also been demonstrated. Finally, Table 2 benchmarks the device metrics such as EOT, $I_{on}$, $g_m$, $R_c$, $I_{off}$/EOT of this work with other BP transistor results in literature [12-15].

### IV. CONCLUSION

High-performance BP MOSFETs with $I_{on}$ = 850μA/μm, $g_m$ of 340μS/μm, EOT = 3nm, and $R_c$ = 0.58kΩμm have been successfully demonstrated in this work. The significant performance improvement is attributed to the BN/Al$_2$O$_3$ bilayer dielectric, which served as a top gate dielectric and a passivation layer. I-V hysteresis and SS as low as 0.1V and 70mV/dec have also been demonstrated.

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### REFERENCES

Fig. 1. Schematic diagram of a BP PMOSFET with BN/Al2O3 gate dielectric.

Fig. 2. (a) Top-view SEM image of two BP MOSFETs with BN/Al2O3 top gate dielectric. (b) EDS element analysis along the AA’ gate direction.

Fig. 3. STM image of a freshly cleaved BP surface showing atomic puckered structures.

Fig. 4. Fabrication process flow for the BP MOSFET. Key steps include: (i) MOCVD BN; (ii) bulk BP growth; (iii) BP exfoliation; (iv) BN transfer; (v) BN dry etching; (vi) ALD Al2O3. BP exfoliation and BN transfer were performed in glovebox filled with high purity Ar.

Fig. 5. AFM image of (a) BN on sapphire with RMS = 0.096 nm and (b) BN after dry etching. The thickness of BN is 1.6 nm.

Fig. 6. Cross-sectional TEM image of the Pt/BP contact after BN etching.

Fig. 7. (a) BP anisotropic Raman. (b) Time dependence of A1g Raman intensity of BP w/o BN, w/ BN, and w/ BN and Al2O3.

Fig. 8. (a) C-V of a BN/Al2O3 capacitor; (b) gate leakage vs. Vg of 1.6nm BN/1.3nm Al2O3.

Fig. 9. Typical I-V of a 200nm Lch BP MOSFET with 7.5nm HfO2 as back gate oxide. No passivation technique is used.

Fig. 10. I-V of a 500nm Lch BP FET with BN/Al2O3 as gate dielectric without source/drain BN etching.

Fig. 11. I-V of a 200nm Lch BP MOSFET with BN/Al2O3 as gate dielectric. The source/drain BN was etched. Hysteresis is as low as 0.1V.
Table 1. Comparison of BP passivation techniques: 1) no passivation; 2) ALD Al₂O₃ as top gate; 3) vacuum annealing; 4) sandwiched with top and bottom BN and annealing; 5) this work.

Table 2. Benchmark of device metrics of this work with other results in literature [12-15].