Multi-probe Interface Characterization of In0.65Ga0.35As/Al2O3 MOSFET

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Abstract
Through a combination of measurement techniques, we study the interface properties of In0.65Ga0.35As transistor with ALD deposited Al2O3 gate dielectric. We show that the interface trap density at In0.65Ga0.35As/Al2O3 interface can be relatively high, but the transistor still exhibits inversion characteristics. A detailed profiling of the interface traps shows that majority of the interface traps are donor-like, and explains the absence of Fermi level pinning in spite of the high interface trap density.

Introduction
With aggressive scaling of device dimensions, it is expected that the widely successful silicon CMOS technology will approach its fundamental limits within the next few technology nodes. Substrate material based on III-V compound semiconductor like InGaAs is an attractive choice for replacing silicon NMOS transistors due to their higher electron mobility [1-5]. However, the interface properties of transistors based on III-V substrate materials are not well understood, and are often a topic of significant debate. In this paper we use a wide range of measurement techniques to characterize the In0.65Ga0.35As/Al2O3 interface so as to obtain the trap density, type and location in position and energy. We show that the interface trap densities are high, but remarkably/counter-intuitively, it is still possible to attain large inversion current since majority of the traps are donor-like.

Interface trap characterization
Fig. 1 shows the device structure used in the study, the fabrication steps of which are discussed in [1-2]. The I_D-V_D characteristics of the device are shown in Fig. 2, and drain current exceeding 1A/mm is obtained. Capacitance-voltage (CV) measurements are carried out at various frequencies (Fig. 3) to study the interface properties of the transistor. The inversion capacitance increases at lower frequencies, suggesting the formation of inversion channel. The interface trap density (D_IT) within the semiconductor bandgap is measured using the Hi-Lo CV method [6], and trap densities above 4.8x10^12/cm^2 eV are obtained (see Fig. 9). Similar values of D_IT in the order of 2-3x10^12/cm^2 eV were also obtained using conductance (G-V) method [7].

Fig. 4a shows the transistor I_D-V_G characteristics. The sub-threshold slopes (SS) of the transistors are found to be high, indicating large interface trap density. Fig. 4b shows the SS and corresponding D_IT which is in the order of 1-2x10^13/cm^2 eV. It is interesting to note that although
D_{IT} shows variation close to factor of 2, the V_T shows a smaller variation, suggesting predominantly donor-like traps within the InGaAs band gap.

Charge pumping (CP) currents measured on various channel length devices are shown in Fig. 5a. A high offset CP current is obtained as the channel length is extrapolated to zero, which has been identified as contribution from substrate region under the gate pad (see Fig. 6). The slope of I_{CP} vs. L is used to obtain D_{IT} \sim 1.5 \times 10^{13}/cm^2 eV. Note that the energy window scanned by CP vary within the oxide (see Fig. 13a), and hence a weighted average \Delta E is used. Full CP sweep on device with gate pad partly removed (Fig. 5b), and multiple rise/fall time CP measurement carried out on devices with different gate areas (Fig. 7) also give similar D_{IT}.

The low frequency CV (LF-CV) has been simulated in presence of D_{IT} and matched with measurement (see Fig. 8). The D_{IT} profile that has been used to match the simulated CV curve with measurement is shown in Fig. 9a. Fig. 9b explains the algorithm used to...
model the impact of interface traps into the simulated CV curve. Full numerical simulation also gives identical results [8]. Donor-like traps with density $\sim 1 \times 10^{13}/cm^2$ eV within the energy bandgap of InGaAs is required to match the experimental CV characteristics.

Fig. 10 provides a summary of interface trap profile from various characterization techniques. Different interface characterization techniques, depending on the region probed, provide a range $D_{IT}$ from $2 \times 10^{12}$- $3 \times 10^{13}/cm^2$ eV. For Si/SiO$_2$ systems, the CP in general provides most accurate/reliable estimates of $D_{IT}$; however since various methods probe different spatial/energy extends into the dielectric and since consistency of assumptions in various techniques cannot be guaranteed a-priori, additional work is needed for quantitative measure of $D_{IT}$ at high-k/III-V interface. However it is interesting that the inversion-mode InGaAs MOSFET still works well with the relatively high $D_{IT}$, and we will address this question in the next section.

### Simulation Results

The relatively high $D_{IT}$ obtained from various characterization techniques have often been linked to Fermi level pinning, which in turn will prevent transistor inversion. However, $I_D$-$V_G$ and CV characteristics clearly show inversion operation. This puzzle is resolved by noting that if the interface states are due to donor-like traps as suggested by $I_D$-$V_G$ (Fig. 4) and LF-CV techniques (Fig. 8, 9), the $V_T$ and ON-current of the transistor remain unaffected. This is also proven by the $I_D$-$V_G$ characteristics obtained from detailed MEDICI simulation for various donor-like trap densities (Fig. 11a). Note that the SS values alone cannot distinguish between acceptor/donor-like traps (Fig. 11c), and hence cannot be used as a signature of Fermi level pinning. However, $I_D$-$V_G$ characteristics for acceptor-like traps show an increase in $V_T$ which makes inversion operation difficult (Fig. 11b), while full inversion – consistent with observed results in Fig. 4 is possible with donor-like traps. We emphasize that this key

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**Table:**

<table>
<thead>
<tr>
<th>Method</th>
<th>$D_{IT}$ (E)</th>
<th>Trap type</th>
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<tbody>
<tr>
<td>G-V</td>
<td>$2 \times 10^{12}$</td>
<td>$2 \times 10^{12}$</td>
</tr>
<tr>
<td>Hi-Lo CV</td>
<td>$6.7 \times 10^{12}$</td>
<td>$8.4 \times 10^{12}$</td>
</tr>
<tr>
<td>LF-CV</td>
<td>$5.6 \times 10^{12}$</td>
<td>$1 \times 10^{13}$</td>
</tr>
<tr>
<td>SS/V_T</td>
<td>$1-2 \times 10^{13}$</td>
<td>$1.5-3.5 \times 10^{13}$</td>
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</tbody>
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**Figure 9:** (a) $D_{IT}$ profile used to match measured and simulated LF-CV characteristic. A good match is obtained by using donor-like traps below the InGaAs conduction band. The trap density within InGaAs band gap agrees well with that measured using Hi-Lo CV technique. (b) Algorithm used to obtain LF CV characteristic in the presence of interface traps from the ideal CV.

**Figure 10:** Summary of $D_{IT}$ profile obtained from various techniques. Note that the sensitivity of the G-V method is lower at high interface trap densities ($qD_{IT}$$/C_{ox}$) [9], and might explain the slightly lower $D_{IT}$ values compared to other techniques. SS/V_T and LF-CV techniques suggest significant contribution from donor-like traps. *Cannot distinguish between donor/acceptor traps.

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**Figure 11:** MEDICI simulation of InGaAs MOSFET with (a) donor-like and (b) acceptor-like interface traps. Donor-like traps change the SS and OFF-current of the device, keeping the $V_T$ and ON-current unchanged. Acceptor-like traps degrade SS, $V_T$ and ON-current. (c) SS from simulated $I_D$-$V_G$ for various acceptor/donor-like trap densities. SS is independent of the nature of the traps and depends only on the trap density.
distinction has been absent in all debates regarding the influence of interface traps at the III-V/high-k interface.

It is interesting to note a couple of things from the above analysis. The concept of charge neutrality level (CNL) is often linked with Fermi level pinning at metal-semiconductor interface, in which the Fermi level is assumed to be pinned close to the CNL [10]. Similarly, the closer the CNL at semiconductor/dielectric interface is to the conduction band, the easier it is to attain inversion. A dominant contribution from donor-like traps moves the CNL closer to the conduction band, and is therefore consistent with the previous reports [11] that suggested CNL in In₀.₆₅Ga₀.₃₅As might be close to the conduction band edge.

Secondly, significant contribution of donor-like traps in the semiconductor bandgap makes it difficult to move the Fermi level towards the valence band edge, in order to turn off the transistor. Therefore, the SS and OFF currents of such transistors can be relatively high, as shown in Fig. 11a. Also, a similar interface trap profile in PMOS transistors might result in Fermi level pinning for the same reason explained above, thereby lowering the drive currents.

**Bulk trap characterization**

In addition to interface trap characterization, the multi-frequency CP (MFCP) measurement [12] (Fig. 12) is used to profile the trap densities into the bulk of Al₂O₃. The spatial and energy extends scanned by MFCP are obtained through a numerical solution of carrier capture and emission between substrate and the trap level, with charge pumping pulse applied at the gate. Simulation results in Fig. 13a indicate that CP scans non-uniform energy extends into the bulk, which can be as large as 0.8eV at the region where differential CP current is to be computed. A non-uniform bulk trap profile is extracted and is shown in Fig. 13b. Bulk trap densities in the order of 7-20x10¹⁹/cm³ eV are obtained, which is a reasonable value for deposited high-k dielectrics [13-14].

**Conclusions**

Based on a combination of measurement techniques and simulation we show that the nature of the trap – and not the number alone – determines Fermi level pinning and surface inversion. The InGaAs/Al₂O₃ based transistors are shown to exhibit strong inversion characteristics in spite of the relatively high trap densities as majority of the traps are donor-like. And thereby, our work addresses a long-standing controversy in the field and provides a new approach to understand high-k/III-V interface properties and their effect on device performance.

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