Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs

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***Abstract*— High-performance InGaAs gate-all-around (GAA) nanowire MOSFETs with channel length (L_{ch}) down to 20 nm are fabricated by integrating a higher k $LaAlO_3$-based gate-stack with an equivalent oxide thickness of 1.2 nm. It is found that inserting an ultrathin (0.5 nm) Al_2O_3 interfacial layer between the higher k $LaAlO_3$ and InGaAs can significantly improve the interface quality and reduce device variation. As a result, a record low subthreshold swing of 63 mV/dec is demonstrated at sub-80-nm L_{ch} for the first time, making InGaAs GAA nanowire devices a strong candidate for future low-power transistors.**

***Index Terms*— InGaAs, MOSFET, nanowire, variability.**

I. Introduction

III–V COMPOUND semiconductors have recently been explored as alternative channel materials for future CMOS technologies [1]. In_x Ga_{1-x} As gate-all-around (GAA) nanowire MOSFETs fabricated using either bottom-up [2], [3] or top-down technology [4]–[6] are of particular interest due to their excellent electrostatic control. Although the improvement of on-state and off-state device metrics has been enabled by nanowire width (W_{NW}) scaling, the scalability of the devices in [4] is greatly limited by the large equivalent oxide thickness (EOT) of 4.5 nm. Aggressive EOT scaling is needed to meet the stringent requirements on electrostatic control [5], [7], [8]. It was shown recently that sub-1-nm EOT with good interface quality can be achieved by Al_2O_3 passivation on planar InGaAs devices [9]. Considering the inherent 3-D nature of the nanowire structure, whether such a gate-stack technology can be successfully integrated in the InGaAs nanowire MOSFET fabrication process remains to be shown. In addition, the electron transport in the devices [4] can be enhanced by increasing the indium concentration in the InGaAs nanowire channel, which promises further on-state metrics improvements such as on-current (I_{ON}) and transconductance (g_m).

Manuscript received December 4, 2012; revised February 5, 2013; accepted February 16, 2013. This work was supported in part by the Air Force Office of Scientific Research monitored by Prof. J. C. M. Hwang and the Semiconductor Research Corporation Focus Center Research Program Materials, Structures, and Devices Focus Center. The review of this letter was arranged by Editor S. J. Koester.

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Digital Object Identifier 10.1109/LED.2013.2248114

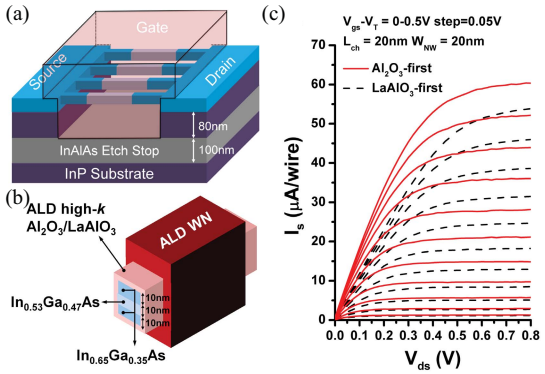

Fig. 1. (a) Schematic diagram and (b) cross sectional view of InGaAs GAA nanowire MOSFETs with ALD $Al_2O_3/LaAlO_3$ gate-stack. (c) Output characteristics (source current) of InGaAs GAA nanowire MOSFETs (L_{ch} = 20 nm) with Al_2O_3-first (solid line) and $LaAlO_3$-first (dashed line) gate-stack.

In this letter, we report the fabrication of $In_{0.65}Ga_{0.35}As$ GAA nanowire MOSFETs with atomic-layer-deposited (ALD) $LaAlO_3$-based gate-stack (EOT = 1.2 nm). ALD $LaAlO_3$ is a promising gate dielectric for future 3-D transistors because of its high dielectric constant (k = 16), precise thickness control, excellent uniformity, and conformality [10]. The effect of ultrathin Al_2O_3 insertion on the device on-state and off-state characteristics has been systematically studied. It is shown that Al_2O_3 insertion effectively passivates the $LaAlO_3$/InGaAs interface, leading to the improvement in both device scalability and variability. Record low subthreshold swing (SS) of 63 mV/dec has been achieved at sub-80-nm L_{ch}, indicating excellent interface quality and gate electrostatic control. Detailed device variation analysis has been presented for the first time for InGaAs MOSFETs, which helps in identifying new manufacturing challenges for future logic devices with high-mobility channels.

II. Experiment

Fig. 1(a) and (b) shows the schematic diagram and cross-sectional view of InGaAs GAA nanowire MOSFETs fabricated. The fabrication process is similar to that described in [4]. A HCl-based wet etch process was used to release the InGaAs nanowires with minimum W_{NW} of 20 nm. Each device had four nanowires in parallel as shown in Fig. 1(a). Because of the relatively high etch selectivity between InAlAs and InP, an additional 100-nm InAlAs etch stop layer was added under the 80-nm InP sacrificial layer to improve the control of

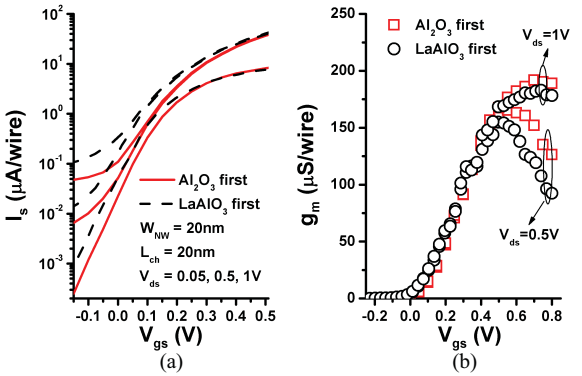

Fig. 2. (a) Transfer characteristics (source current) at $V_{ds} = 0.05$, 0.5, and 1 V and (b) g_m-V_{gs} of Al_2O_3-first and $LaAlO_3$-first InGaAs GAA nanowire MOSFETs with $L_{ch} = 20$ nm.

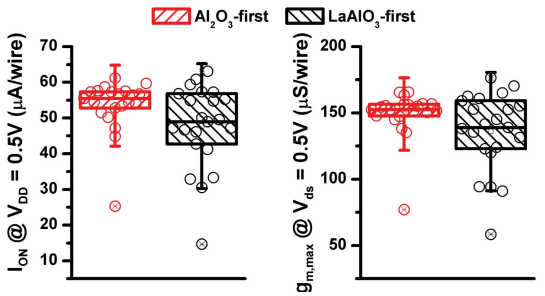

Fig. 3. I_{ON} and peak g_m box plots of Al_2O_3-first and $LaAlO_3$-first devices with $L_{ch} = 20$ nm and $W_{NW} = 20$ nm at $V_{DD} = 0.5$ V.

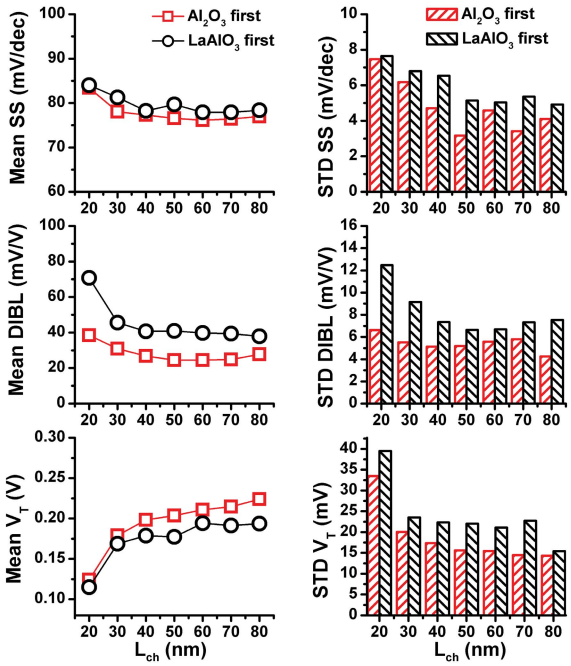

Fig. 4. Scaling metrics of SS, DIBL, and V_T and their standard deviations (STDs) for Al_2O_3-first and $LaAlO_3$-first InGaAs GAA nanowire MOSFETs with $W_{NW} = 20$ nm.

the nanowire release process. The InGaAs nanowire channel consists of one 10-nm $In_{0.53}Ga_{0.47}As$ layer sandwiched between two 10-nm $In_{0.65}Ga_{0.35}As$ layers, as shown in Fig. 1(b), yielding a total nanowire height (H_{NW}) of 30 nm. Here, the heterostructure design ensures the high quality of epitaxial layers grown by molecular beam epitaxy while maximizing the indium concentration in the nanowire. A 0.5-nm Al_2O_3, 4-nm $LaAlO_3$, and 40-nm WN high-k/metal gate-stack were grown by ALD surrounding all facets of the nanowires. Two samples were fabricated in parallel with only the sequence of the Al_2O_3 and $LaAlO_3$ growth deliberately switched. Both samples were treated with 10% $(NH_4)_2S$, and then transferred into the ALD chamber within 1 min of air break. Since the Al_2O_3-first and $LaAlO_3$-first samples had the same EOT of 1.2 nm and underwent the same process flow, the difference of device performance can be ascribed to the effect of the Al_2O_3 passivation. All other fabrication details can be found in [4]. In this letter, the channel length (L_{ch}) is defined as the width of the electron beam resist in the source/drain implantation process and has been verified by scanning electron microscopy.

III. Results and Discussion

Fig. 1(c) shows the output characteristics of two representative Al_2O_3-first and $LaAlO_3$-first InGaAs GAA nanowire MOSFETs with $L_{ch} = 20$ nm. Fig. 2(a) and (b) shows the transfer characteristics and transconductance of the same devices. Because of the large junction leakage current in the drain, the source current I_s is shown in the current–voltage characteristics and used to calculate I_{ON} and g_m. The Al_2O_3-first device shows higher $I_{ON} = 57$ μA/wire at $V_{DD} = V_{ds} = V_{gs} - V_T = 0.5$ V and peak transconductance $g_{m,max} = 165$ μS/wire at $V_{ds} = 0.5$ V, compared to 48 μA/wire and 155 μS/wire for the $LaAlO_3$-first device. Both devices operate in the enhancement mode, with a linearly extrapolated V_T of 0.14 and 0.11 V, respectively. For the off-state performance, the Al_2O_3-first device shows an SS of 75 mV/dec and DIBL of 40 mV/V, while the $LaAlO_3$-first device shows a higher SS of 80 mV/dec and a higher DIBL of 73 mV/V. To study the statistical distribution of the on-state metrics, the box plots for I_{ON} and $g_{m,max}$ at $V_{DD} = 0.5$ V are shown in Fig. 3. The box plots include measurements from all 50 devices with L_{ch} of 20 nm and W_{NW} of 20 nm. Although only a 12% (10%) increase in mean I_{ON} ($g_{m,max}$) is observed for the devices with Al_2O_3 insertion, a 54% (64%) reduction in standard deviation of I_{ON} ($g_{m,max}$) is obtained on the Al_2O_3-first devices, indicating a significant improvement in device variation by effective passivation of interface traps. The I_{ON} variation is impacted by several variation sources including parasitic resistance, effective mobility, and V_T variation [11], all of which are sensitive to the interface quality of the high-k/InGaAs nanowire surface.

To further investigate the scalability and off-state performance variability, the averages and standard deviations of SS, DIBL, and V_T as a function of L_{ch} are shown in Fig. 4 for Al_2O_3-first and $LaAlO_3$-first devices with $W_{NW} = 20$ nm. The SS and DIBL remain almost constant with L_{ch} scaling down to 50 nm for both samples. This indicates that the current GAA structure with 1.2-nm EOT has yielded a very small geometric screening length and the devices show excellent

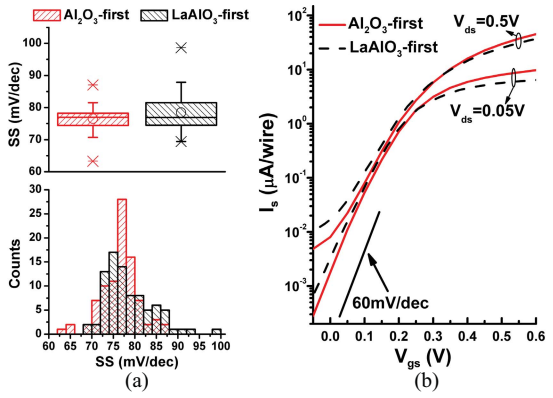

Fig. 5. (a) SS box plot and histogram for all Al_2O_3-first and $LaAlO_3$-first devices with L_{ch} between 50 and 80 nm and W_{NW} of 20 nm. (b) Transfer characteristic (source current) of an Al_2O_3-first and a $LaAlO_3$-first InGaAs GAA nanowire MOSFET with lowest SS of 63 and 69 mV/dec, respectively.

resistance to short-channel effects. Average SS = 76 mV/dec and DIBL = 25 mV/V are obtained for Al_2O_3-first devices with L_{ch} between 50 and 80 nm, compared to 79 mV/dec and 39 mV/V for the $LaAlO_3$-first devices, indicating a reduction of interface trap density (D_{it}) with Al_2O_3 passivation. A small increase in V_T is also observed for the Al_2O_3-first sample, which is ascribed to the reduction in negative donor-type charges at the interface. Furthermore, larger standard deviations of SS, DIBL, and V_T are observed for devices without Al_2O_3 insertion at all L_{ch}, indicating that the relatively low interface quality of the $LaAlO_3$-first devices introduced additional device variation. It is also shown that the off-state performance variation increases as L_{ch} scales below 50 nm, which is ascribed to the reduction in electrostatic control.

Fig. 5(a) shows the box plot and histogram of SS measured from all the Al_2O_3-first and $LaAlO_3$-first devices with L_{ch} between 50 and 80 nm and W_{NW} of 20 nm. Although the average SS for Al_2O_3-first devices is only 1.9 mV/dec lower than that of $LaAlO_3$-first devices, 25% and 46% reduction in standard deviation and interquartile range has been obtained on Al_2O_3-first devices, indicating the effectiveness of Al_2O_3 passivation. Since these devices are immune to short-channel effects, SS is dominated by D_{it}. Therefore, D_{it} can be estimated from SS using the equation

$$\mathrm{SS} = \frac{60}{300} T \left(1 + \left(\frac{q D_{\mathrm{it}}}{C_{\mathrm{ox}}}\right)\right) [\mathrm{mV/dec}] \qquad (1)$$

where T is the temperature in kelvin, q is the electronic charge, and C_{ox} is the oxide capacitance. Ninety percent of the devices with Al_2O_3 insertion show SS between 66.0 and 83.3 mV/dec, corresponding to a D_{it} between 1.80×10^{12} and $6.98 \times 10^{12}/\mathrm{cm}^2/\mathrm{eV}$. Fig. 5(b) shows the transfer characteristics of an 80-nm L_{ch} hero Al_2O_3-first device and a 60-nm L_{ch} hero $LaAlO_3$-first device with the lowest $SS = 63$ and 69 mV/dec, respectively. The estimated D_{it} for these two devices are 8.98×10^{11} and $2.69 \times 10^{12}/\mathrm{cm}^2 \cdot \mathrm{eV}$. The near-ideal SS is achieved because of the very small surface area of the nanowires, aggressive EOT scaling, and effective interface passivation.

IV. Conclusion

InGaAs GAA nanowire MOSFETs with L_{ch} down to 20 nm and EOT down to 1.2 nm were demonstrated, showing excellent gate electrostatic control. The insertion of an ultrathin 0.5-nm Al_2O_3 layer in the $LaAlO_3$/InGaAs interface was shown to effectively improve the scalability and variability of the devices. SS of near 60 mV/dec was achieved on InGaAs nanowires with scaled EOT and effective interface passivation. The InGaAs GAA nanowire MOSFET is a promising candidate for low-power logic applications beyond 10 nm.

Acknowledgment

The authors would like to thank A. T. Neal, M. S. Lundstrom, D. A. Antoniadis, and J. A. del Alamo for valuable discussions.

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