Al₂O₃/β-Ga₂O₃(-201) Interface Improvement
Through Piranha Pretreatment
and Postdeposition Annealing

Hong Zhou, Sami Alghmadi, Mengwei Si, Gang Qiu, and Peide D. Ye, Fellow, IEEE

Abstract—In this letter, we report on the improvement of atomic layer deposited (ALD) Al₂O₃/β-Ga₂O₃ (-201) interface quality through piranha pretreatment and postdeposition annealing (PDA). The high quality interface is verified via the temperature dependent capacitance–voltage (C–V) and photo-assisted (deep UV) C–V measurements, considering its ultra wide bandgap of 4.8 eV for β-Ga₂O₃. A low C–V hysteresis of 0.1 V from the measurement frequency of 1 kHz to 1 MHz is obtained, compared with the hysteresis of 0.45 V without piranha optimization. An average interface trap density (Dit) of 2.3 × 10¹¹ cm⁻²·eV⁻¹ is extracted from the photo C–V measurements. Piranha pretreatments and PDA turn out to be an effective way to improve the ALD Al₂O₃/β-Ga₂O₃ (-201) interface for future high quality Ga₂O₃ metal–oxide–semiconductor field-effect transistors.

Index Terms—β-Ga₂O₃, interface, Dit, hysteresis, ALD Al₂O₃, piranha, annealing.

I. INTRODUCTION

VERY recently, β-Ga₂O₃ has been considered as a promising candidate for the next generation power electronics due to its ultra wide bandgap (Eg) of 4.8 eV compared with SiC and GaN with bandgap of 3.2 and 3.4 eV, respectively [1]–[8]. Its 4.8 eV bandgap enables the β-Ga₂O₃ to have a theoretical breakdown field (Eₜ) of 8 MV/cm. Even at such early development stage, a high Eₜ of 3.8 MV/cm has already been achieved, which exceeds the Eₜ of GaN and SiC [9]. Combined with the 100 cm²/V·s room temperature electron mobility (μ), β-Ga₂O₃ possesses a high Baliga’s figure of merit of 3444, defined as εμEₜ² [10]. In addition to its excellent material property, potential cost effective large size substrate can be realized through Czochralski method [11], [12]. However, unlike the GaN HEMT and MOSHEMT with buried channels, β-Ga₂O₃ can only form a depletion-mode MOSFET so far. Therefore, gate dielectric/oxide interface plays an important role in forming high performance MOSFETs. In general, high-k dielectric, high conduction band offset, and high oxide/β-Ga₂O₃ interface quality are major concerns in terms of obtaining high performance device characteristics [13], [14].

There are several methods to determine the MOS interface trap densities (Dit), such as Terman method, hi/lo frequency (f) method and AC conductance method [15], [16]. However, some inherent limitations exist when applying those methods to β-Ga₂O₃ with 4.8 eV bandgap [17]. For instance, inaccurate estimation of the doping concentration and oxide capacitance and the negligence of deep energy level traps lead to underestimation of Dit by comparing the ideal C-V curve with high f C-V curve. Hi/lo f method leads to significantly under-estimate the Dit also since it takes an extremely long time to generate holes in n-Ga₂O₃ so that low f criteria is not satisfied. AC conductance method can only detect shallow energy level (0.2-0.6 eV) Dit due to the limited f and temperature (T) ranges to detect the traps deeply inside the bandgap. In addition, the Ga₂O₃ trap capture cross-section σ is still undetermined yet, which makes the trap energy level in the bandgap less accurate. Photo-assisted C-V takes advantage of the ultraviolet (UV) illumination to generate electron-hole pairs in the wide bandgap materials, ensuring that all the traps in the bandgap can respond during the measurement [18], [19]. By comparing the dark high f C-V curve with the post-UV C-V curve, an overall average Dit can be obtained from the shift of the two curves.

II. DEVICE FABRICATION AND MEASUREMENT

As received 2 inch Sn-doped β-Ga₂O₃ (-201) was first diced into 6 mm by 6 mm small pieces. The diced samples have been treated with acetone, methanol and isopropanol solvent clean for 30 minutes. Before loading into ASM F-120 ALD chamber, 6 pieces of samples were first pretreated by piranha (98% H₂SO₄: 30% H₂O₂ = 3 : 1) for 1 min. and DI water rinse. 15 nm of Al₂O₃ was then deposited by ALD at 250 °C with tri-methyl-aluminum (TMA) and H₂O as precursors. 2 pieces were then annealed in Jepelec rapid thermal annealing (RTA) furnace for 2 minutes under O₂ and N₂ atmosphere at 500 °C. 3 samples were annealed for 1 minute under O₂ atmosphere at elevated temperatures of 600, 700 and 800 °C, respectively. As a comparison purpose, 3 samples without piranha pretreatment were also deposited with 15 nm of Al₂O₃ at 250 °C, and 2 of them were annealed under the same conditions as the 2 samples with piranha pretreatment above. Serial MOS capacitors (MOSCAPs) were then fabricated with photo
lithography followed by Ti/Au (30/70 nm) lift-off process. A high precision HP4284 LCR meter was used for the capacitance measurement. Deep UV light with wavelength of 300 nm was used as the light source of the photo-assisted C-V measurements. The fabricated MOSCAPs were shown in Fig.1 (a), and the doping concentration \( N_d \) of the \( \beta \)-Ga\(_2\)O\(_3\) is extracted to be \( 2.7 \times 10^{18} \) cm\(^{-3}\) from the slope of \( 1/C^2 \) [20]:

\[
N_d = \frac{2}{q\varepsilon_0\varepsilon_s A^2} \frac{d}{dV} \left( \frac{1}{C^2} \right)
\]

where the gate electrode area \( A \) is \( 1.96 \times 10^{-5} \) cm\(^2\), and \( \varepsilon_0 \) and \( \varepsilon_s \) of 9.5 are vacuum permittivity and relative dielectric constant of \( \beta \)-Ga\(_2\)O\(_3\).

### III. Results and Discussion

Fig. 2 shows the \( f \)-dependent C-V hysteresis measurements of two optimized samples with and without piranha pretreatments, respectively. The measurements start from depletion to accumulation and then sweep back to depletion. The existence of the interface and bulk traps leads to a shift of the flat-band voltage \( V_{FB} \) due to the trapping and de-trapping at the bi-directional sweeps. The sweep rate for the C-V hysteresis measurement is 1.0 second per 0.1 V step and the forward to reverse sweep hold time is 10 seconds. With piranha pretreatment, the hysteresis is 0.1 V, while on the other hand the hysteresis is 0.45 V without piranha pretreatment.

The trapped electrons or detectable interface trap quantity \( Q_{it} \) can be roughly estimated through the \( V_{FB} \) shift by using the equation: \( Q_{it} = C_{ox} \times \Delta V/q \), where \( C_{ox} = 0.5 \) \( \mu \)F/cm\(^2\) and \( \Delta V \) are the oxide capacitance and \( V_{FB} \) difference, respectively. The \( Q_{it} \) is reduced from \( 1.4 \times 10^{12} \) cm\(^{-2}\) without piranha treatment to \( 3.2 \times 10^{11} \) cm\(^{-2}\) after treatment. The piranha pretreatment is found to be useful in smoothing the sample surface and removing carbon-based organic contamination [21].

The root mean square (RMS) surface roughness after piranha is 0.17 nm, while the sample without piranha pretreatment is 0.26 nm, as shown in Fig.2 (c) and (d).

Fig. 3 summarizes the post deposition annealing (PDA) influences on the piranha pretreated samples. Both room temperature and high temperature (\( T = 150 \) °C) C-V curves are presented. Deep depletion behavior is observed due to the wide bandgap of Ga\(_2\)O\(_3\) so that inversion layer is not formed at 3 kHz-2 MHz. At room temperature, there is no significant difference between unannealed and annealed samples with no obvious stretch out near depletion and slight frequency
At temperatures in our experiment, since Ga2O3 has a wide normalized conductance, the depletion of the MOSCAP is limited to the depletion of the MOSCAP. No obvious dispersion at accumulation. Compared with room temperature C-V curves, there is a right shift of high temperature C-V curves, showing the existence of negative charge at the Al2O3/Ga2O3 interface. Similar right shift at high temperatures is also observed by Wong [2]. Room temperature C-V measurement at accumulation region allow border traps capturing electrons and represent themselves as “negative” fixed charges, which leads the flatband voltage shifted to left compared to the ones measured at high temperatures [14]. One big issue for β-Ga2O3 is its low thermal conductivity from room temperature to elevated temperatures, which degrades the device performances, such as electron mobility. The large flatband or VFB shifts are observed at elevated temperatures. At high temperatures, unannealed MOSCAP has higher frequency dispersion compared with annealed ones, as highlighted by the red rectangles, indicating that PDA can help to further increase the interface quality. Moreover, AC conductance method is also used to extract the Dit of the MOSCAP. The VG is limited to the depletion of the MOSCAP. No obvious normalized conductance (G_D/Aqo) peaks are observed even at T= 175 °C. It is likely that even at this high temperature of 175 °C, the conductance method cannot detect deep trap energy levels in our experiment, since Ga2O3 has a wide bandgap of 4.8 eV.

Because of the wide bandgap of Ga2O3, photo-assisted C-V method becomes a reliable approach to evaluate the MOS interface and extract the average Dit. The measurements started with biasing VG at accumulation for 10 s to make sure traps are filled with electrons, and then sweeping VG from deep depletion to accumulation at high f= 1 MHz in dark. Then, VG is kept biased at deep depletion with VG = -10 V and deep UV light is on for 10 minutes to generate electron-hole pairs and forcing generated holes to move to the Al2O3/Ga2O3 interface. After turning off the UV light and then sweeping the C-V from depletion to accumulation again in dark, a UV off C-V curve is obtained. UV generated holes recombine with those trapped electrons so that after UV exposure the interface is “donors” dominated compared to “acceptors” dominated interface without UV illumination. Therefore, a left shift of the C-V curves is observed and this VFB shift can be translated into the average Dit by the equation:

\[ D_{it} = \frac{C_{ox} \times \Delta V}{V_{FB} - V_{FB}} \]

The VFB is determined through the extrapolated line of the C-V curves at C2/C2 = 0, as shown in Fig. 4 (a) [22]. Fig.4 (a)-(c) describes the originally measured photo-assisted C-V comparisons with dark high frequency C-V curves. The gate leakage currents at both sweeps are limited to 10 μA/cm². Both the 500 °C N2 and O2 PDA can help to minimize the average Dit, which confirms that PDA is needed to optimize the Al2O3/β-Ga2O3 interface. The improved interface quality after O2 annealing is related to the compensation of oxygen vacancies [23]. The achieved minimal average Dit is 2.3 x 10⁻¹¹ cm⁻² eV⁻¹ with 0.35 V VFB shift. Increased annealing temperature at 600, 700 and 800 °C starts to degrade the interface in our experiments. Both our work and the work from Zeng et al. [13] show a decent interface trap density less than 10⁻¹² cm⁻² eV⁻¹, which is favorable for device applications. Compared to Ref.[13], we have taken a further step to optimize the interface through piranha pretreatment and PDA, which might be useful to further improve β-Ga2O3 MOS interface for device applications.

IV. CONCLUSION

We have investigated the piranha pretreatment and PDA effects on Al2O3/β-Ga2O3 (-201) interface through frequency and temperature-dependent and photo-assisted C-V measurements. Low C-V hysteresis of 0.1 V, reduced high-temperature frequency dispersion and reduced VFB shifts are benefited from the improved interface quality. Finally, a low average Dit of 2.3 x 10⁻¹¹ cm⁻² eV⁻¹ is achieved through photo-assisted C-V measurements. Piranha pretreatment and PDA process are demonstrated to effectively improve the Al2O3/β-Ga2O3 interface, making the Al2O3/β-Ga2O3 (-201) MOS structure possible for future power electronics.

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REFERENCES


