# Distinguishing the Different $V_{th}$ shift Mechanisms in $In_2O_3$ TFTs Using Ultrafast On-the-Fly Reliability Measurements

Chien-Hung Yeh, Chang Niu, Jian-Yu Lin, Zehao Lin, Chang Liu, Juanjuan Lu, Sumi Lee, Haiyan Wang, Ting-Chang Chang, Peide D. Ye, *Fellow*, *IEEE*

***Abstract*— This study presents a comprehensive investigation of the threshold voltage ($V_{th}$) shift mechanisms in atomic-layer-deposited (ALD) $In_2O_3$ thin-film transistors (TFTs), utilizing ultrafast On-the-Fly (UF-OTF) measurements. Two distinct degradation mechanisms are identified: electron trapping and donor trap generation at the $HfO_2/In_2O_3$ interface under positive bias stress (PBS), which conventional measure-stress-measure (MSM) techniques fail to effectively separate due to the inability to perform short-time measurements. Donor trap generation exhibits a strong dependence on measurement temperature, and stress degradation time, indicating a thermally activated process. Optimized oxygen annealing effectively passivates these defects, significantly reducing their impact on device instability. Temperature-dependent measurements reveal shallow electron trapping with an activation energy ($E_{\tau,e}$) of 0.12 eV, whereas donor trap generation is characterized by an activation energy ($E_{\tau,d}$) of 0.57 eV. These results emphasize the importance of oxygen annealing optimization, defect passivation, and self-heating mitigation to enhance the electrical performance, long-term stability, and overall reliability of high-performance $In_2O_3$ TFTs for advanced electronic applications.**

***Index Terms*— atomic layer deposition (ALD), indium oxide, ultrafast On-the-Fly, positive bias stress**

## I. Introduction

Amorphous oxide semiconductor-based FETs have garnered significant attention in recent years due to their potential applications as back-end-of-line (BEOL) compatible transistors in monolithic 3D integration [1], [2], [3], [4], [5], [6]. ALD $In_2O_3$ TFTs offer several key advantages, including excellent conformity on complex structures and high electron mobility [2], remarkable on-state current and trans-conductance [3], outstanding reliability [4], and negative Schottky barrier height-induced ultralow contact resistance reaching Landuaer's limit [5].

Despite these advantages, long-term threshold voltage ($V_{th}$) stability and overall reliability of $In_2O_3$ TFTs remain major concerns. $V_{th}$ shifts, often induced by charge trapping and defect creation, can significantly impact device performance and reliability. A comprehensive understanding of the mechanisms driving $V_{th}$ instability is essential to further improve device reliability [7]. The widely used MSM method cannot capture the fast and dynamic nature of these trapping-detrapping processes [8], [9], especially during electrical stress and relaxation cycles. UF-OTF method, with its ability to achieve microsecond-level temporal resolution, provides a unique approach to distinguish the different contributions of these mechanisms in time domain [10], [11], [12], [13], [14].

By employing the UF-OTF technique, this study conclusively identifies two primary mechanisms contributing to $V_{th}$ instability in nanoscale $In_2O_3$ TFTs: the rapid electron trapping in dielectric and the slow generation of donor traps in oxide channel both near the interface.

## II. Experiments

Fig.1 (a) illustrates the schematic cross-sectional view of a

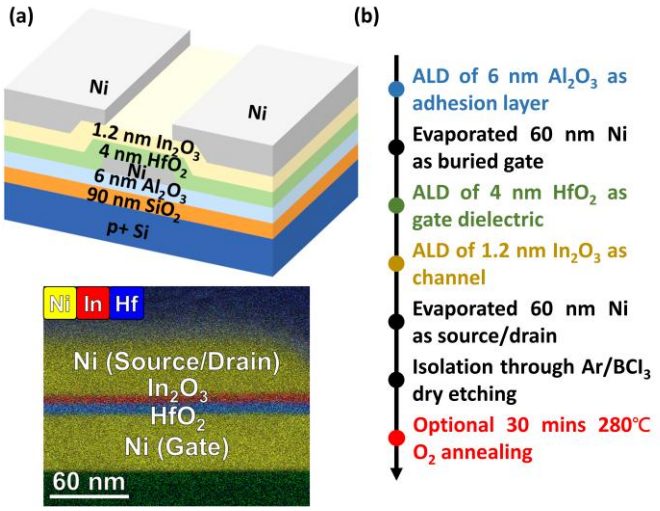


Figure 1. (a) 3D schematic of a bottom gate $In_2O_3$ FETs and STEM cross-section image with energy dispersive X-ray spectroscopy elemental mapping (In, Hf, and Ni) of a similar device structure (b) Fabrication process flow of ALD $In_2O_3$ FETs.

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C-H Yeh, is with the Department of Photonics, National Sun Yat-Sen University, Kaohsiung, 80424, Taiwan and also with the Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA.

Chang Niu, Jian-Yu Lin, Zehao Lin, Chang Liu, and Peide D. Ye are with the Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Chang Liu, Juanjuan Lu, and Haiyan Wang are with the School of Material Engineering, Purdue University, West Lafayette, IN 47907 USA.

Ting-Chang Chang is with the Department of Physics and also with College of Semiconductor and Advanced Technology Research, National Sun Yat-sen University, Kaohsiung, 804, Taiwan

fabricated $In_2O_3$ TFT. The fabrication process flow is presented in Fig. 1(b). First, a 6 nm $Al_2O_3$ layer was deposited by ALD as an adhesion layer. A 60 nm Ni layer was evaporated to form the buried gate, followed by the deposition of a 4 nm $HfO_2$ layer by ALD as the back gate dielectric. The 1.2 nm $In_2O_3$ channel layer was deposited also by ALD, and another 60 nm Ni layer was evaporated to form the source and drain contacts. Isolation of the device was achieved through an $Ar/BCl_3$ dry etching process. An optional annealing process in $O_2$ at 280°C for 30 minutes was performed to enhance the device performance and reliability [15].

## III. Result and Discussion

Fig. 2 (a) illustrates the transfer characteristics of well-behaved annealed long-channel ($L_{ch}$=600nm) devices measured at $V_{DS}$ = 0.1 V and 1 V, showing good subthreshold swing (SS) and high on/off ratio of $10^8$-$10^9$. The SS was extracted based on a constant-current $V_{th}$ definition, using the subthreshold region between drain currents of $10^{-13}$ and $10^{-11}$ A. Fig. 2 (b) shows the output characteristic of the annealed device, showing $I_{on}$ of 197 μA/μm at $V_{DS}$ =4V. The evolution of the transfer curves and the time evolution of $\Delta V_{th}$ and SS under 1000s PBS at $V_{GS}$ = 3V for both annealed and unannealed devices are shown in Fig. 2 (c) and Fig. 2 (d). It is evident that an appropriate $O_2$ annealing process effectively reduces oxygen vacancies and defects, thereby significantly mitigating the negative $V_{th}$ shift under PBS. As shown in Fig. 3, where both annealed and unannealed devices exhibit negligible variation in SS over time. Since the subthreshold swing can be used to evaluate interface trap densities [16], this result indicates that the degradation does not occur at the channel interface.

To further investigate these mechanisms, we first examine unannealed devices, which exhibit a significant $V_{th}$ shift to investigate the different mechanisms utilizing UF-OTF method [17]. The UF-OTF waveform is shown in Fig. 4(a). The measurement process is divided into two phases: the stress phase and the relaxation phase. The drain current at the beginning of the stress phase is defined as $I_{D0,stress}$, while the drain current at the start of the relaxation phase—immediately after completing 10,000 seconds of stress—is defined as $I_{D0,Relax}$. Both $I_{D0,stress}$ and $I_{D0,relax}$ were extracted in the linear regime of device operation, with gate and drain voltages set to $V_G$ =3V $V_D$ = 0.1V and $V_G$ =0V $V_D$ = 0.1V, respectively. The drain current change, $\Delta I_D$, is calculated as $I_D(t) - I_{D0}$, where $I_{D0}$ refers to the initial current of the respective phase. The threshold voltage, before stress is applied, is denoted as $V_{th0}$, representing the pre-stressed $V_{th}$. Using the formula in Fig. 4 (a), The drain current variation ($\Delta I_D$) can be translated into a threshold voltage shift ($\Delta V_{th}$) shown in Fig. 4 (b) and Fig. 4 (c).

As the stress and degradation time progress, the threshold voltage shift ($\Delta V_{th}$) reveals three clearly distinguishable phases: initial leveling, gradual rising, and subsequent falling. In the initial stage, occurring at a very short time scale, $\Delta V_{th}$ remains relatively constant, indicating a temporary equilibrium between competing mechanisms. This plateau behavior is attributed to the dynamic balance between fast electron trapping and slower donor-type trap generation processes. As the stress continues, a rising trend in $\Delta V_{th}$ becomes evident, which is predominantly governed by electron trapping at the $HfO_2/In_2O_3$ interface.

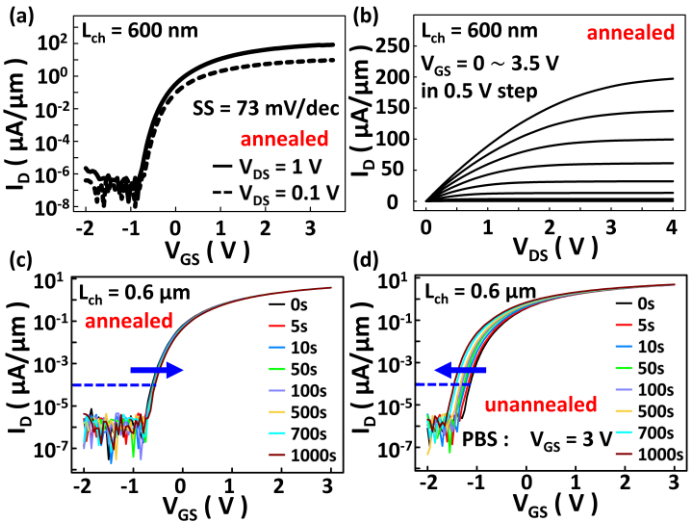


Figure 2. (a) $I_D - V_{GS}$ and (b) output characteristics of the $In_2O_3$ FETswith channel length ($L_{ch}$) = 600 nm. (c) Evolution of transfer curves of annealed $In_2O_3$ FETs under PBS of 3 V. (d) Evolution of transfer curves of unannealed $In_2O_3$ FETs under PBS of 3 V.

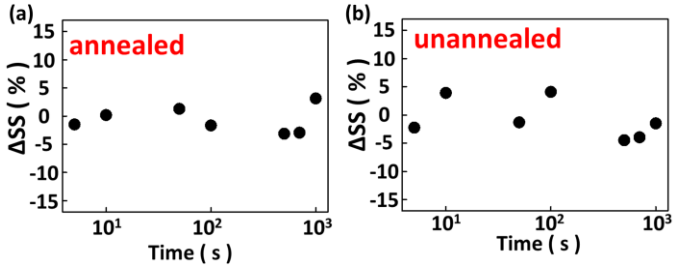


Figure 3. (a) ΔSS of anneal $In_2O_3$ FETs under PBS of 3 V. (b) ΔSS of unannealed $In_2O_3$ FETs under PBS of 3 V.

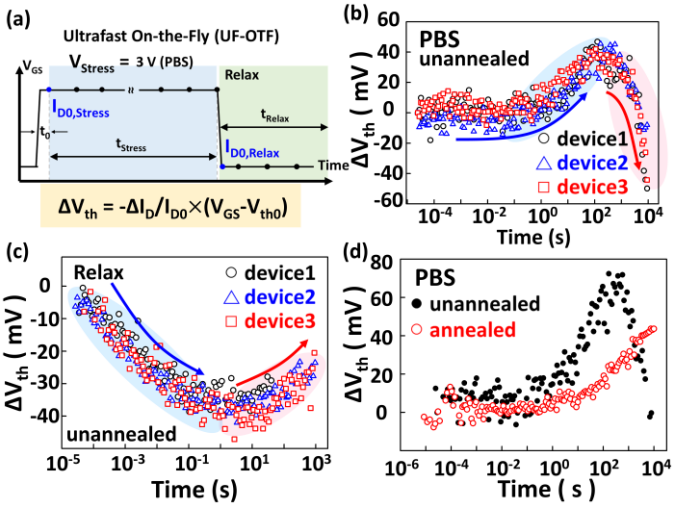


Figure 4. (a) Schematic of UF-OTF waveform. $ID_{0,Stress}$ represents the first current data point during the PBS process, while $ID_{0,Relax}$ represents the first current data point during the relaxation. (b) $\Delta V_{th}$ of unannealed devices induced by PBS degradation, extracted from UF-OTF measurements. (c) Time evolution of $\Delta V_{th}$ observed during the relax phase for unannealed devices. (d) Time evolution of $\Delta V_{th}$ of unannealed and annealed devices during PBS phase.

These trapped electrons accumulate near the dielectric/semiconductor boundary, leading to a positive shift in the threshold voltage.

As shown in Fig. 4(c), the recovery time of electron trapping is less than 1 millisecond. However, the MSM measurement process involves a module-switching delay on the order of

milliseconds. As a result, the Vth shift caused by electron trapping cannot be observed in MSM measurements, since the trapped electrons have already recovered during this delay. In contrast, the UF-OTF method enables real-time measurement without module-switching delays, successfully capturing the effects of electron trapping.

However, at longer stress durations, $\Delta V_{th}$ begins to decrease, marking the onset of a falling phase, which is primarily driven by the generation of donor-like traps located below the charge neutrality level (CNL) within the conduction band of $In_2O_3$ near the interface [18]. These donor-type traps act as electron sources, effectively increasing the free carrier concentration and thus reducing the threshold voltage.

These observations highlight two competing mechanisms with opposite impacts on $V_{th}$ shift across different time scales. Notably, the ultrafast On-the-Fly (UF-OTF) technique applied in this study provides, for the first time, the temporal resolution required to distinguish these effects clearly. Unlike conventional measure-stress-measure (MSM) methods, the UF-OTF approach enables real-time tracking of $V_{th}$ evolution, offering deeper insight into the coexisting but temporally distinct degradation mechanisms.

Additionally, the relaxation behavior observed after stress and degradation, as shown in Fig. 4 (c), exhibits a decrease in $\Delta V_{th}$ attributed to electron detrapping, followed by an increase in $\Delta V_{th}$ associated with the partial recovery of donor-type trap generation over a different time scale [19].

Comparing $\Delta V_{th}$ of PBS and relaxation between the unannealed and annealed devices, Fig. 4 (d) reveals a significant reduction in variations for the annealed device, indicating that the annealing process effectively passivates donor traps in $In_2O_3$. Moreover, the pronounced suppression of $\Delta V_{th}$ variations in the annealed device further confirms that the annealing process effectively passivates donor-type traps in $In_2O_3$, thereby improving device stability and mitigating long-term degradation under positive bias stress.

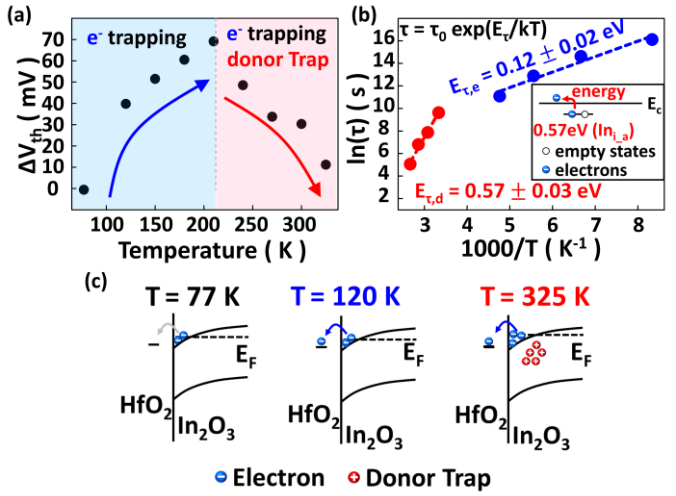


Figure 5. (a) Temperature evolution of $\Delta V_{th}$. Electron trapping dominates at lower temperatures, while donor trap becomes the dominant mechanism at higher temperatures. (b) Plot of ln(τ) versus 1000/T yields $E_{\tau,e}$ = 0.12 eV for electron trapping and $E_{\tau,d}$ = 0.57 eV for donor traps, attributed to interstitial indium at the a-site ($In_{i\_a}$), consistent with theoretical predictions [19]. (c) The corresponding schematic energy band diagrams at various temperatures.

To further investigate the defect nature responsible for the observed $V_{th}$ shift, temperature-dependent reliability measurements were conducted. As shown in Fig. 5(a), the temperature evolution of $V_{th}$ reveals that donor-type trap generation becomes the dominant degradation mechanism at elevated temperatures. Measurements from 120 K to 375 K, using the equation :

$$\Delta V_{th} = \Delta V_{th\infty,e}\left\{1 - exp\left[-\left(t/\tau_e\right)^{n_e}\right]\right\} - \Delta V_{th\infty,h}\left\{1 - exp\left[-\left(t/\tau_d\right)^{n_d}\right]\right\} \quad (1)$$

where $\Delta V_{th\infty,e}$ and $\Delta V_{th\infty,h}$ denote the maximum threshold voltage shifts caused by electron trapping and donor-type trap generation, respectively. $\tau_e$ and $\tau_d$ are the corresponding characteristic time constants. $n_e$ and $n_d$ are the stretched-exponential exponents for each mechanism [20]. The extracted $\tau$ values at different temperatures were further fitted using the following equation:

$$\tau(T) = \tau_0 exp\left(E_\tau/kT\right) \quad (2)$$

where $\tau(T)$ represents the extracted time constant at different temperature, $\tau_0$ is the pre-exponential factor, $E_\tau$ is the activation energy associated with the process, $k$ is the Boltzmann constant, and $T$ is the absolute temperature. The fitting results in Fig. 5(b) yield activation energies for electron trapping ($E_{\tau,e}$) and donor trap generation ($E_{\tau,d}$) of 0.12 eV and 0.57 eV, respectively. These values are in excellent agreement with theoretical studies on native donor defect energy levels responsible for n-type conductivity in $In_2O_3$ [21].

## IV. CONCLUSION

This study employs the UF-OTF technique in the time domain to differentiate the two main mechanisms of $V_{th}$ instability in $In_2O_3$ TFTs: electron trapping and donor-type trap generation. At low temperatures and short times, electron trapping dominates, linked to shallow defects $E_{\tau,e}$ = 0.12 eV. In contrast, higher temperatures and longer stress promote donor trap generation, associated with deeper, thermally activated states $E_{\tau,d}$ = 0.57 eV. $O_2$ annealing effectively suppresses donor trap formation, reducing $\Delta V_{th}$ shifts under PBS. These results clarify the time- and temperature-dependent degradation mechanisms and highlight oxygen annealing as a practical method for enhancing device reliability.

## REFERENCES

[1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa and H. Ye, "Back-End-of-Line Compatible Transistors for Monolithic 3-D Integration," in IEEE Micro, vol. 39, no. 6, pp. 8-15, 1 Nov.-Dec. 2019, doi: 10.1109/MM.2019.2942978.

[2] Z. Lin, C. Niu, H. Jang, T. Kim, Y. Zhang, H. Wang, C. Jeong and P. D. Ye, "Enhancement of $In_2O_3$ Field-Effect Mobility Up To 152 $cm^2 \cdot V^{-1} \cdot s^{-1}$Using HZO-Based Higher-k Linear Dielectric," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2, doi: 10.1109/VLSITechnologyandCir46783.2024.10631497.

[3] Z. Zhang, Z. Lin, P. Y. Liao, V. Askarpour, H. Dou, Z. Shang, A. Charnas , M. Si, S. Alajlouni , A. Shakouri, H. Wang, M. Lundstrom, J. Maassen , and P. D. Ye "A Gate-All-Around $In_2O_3$ Nanoribbon FET With Near 20 mA/μm Drain Current," in IEEE Electron Device Letters, vol. 43, no. 11, pp. 1905-1908, Nov. 2022, doi: 10.1109/LED.2022.3210005.

[4] Z. Zhang, Z. Lin, C. Niu, M. Si, M. A. Alam and P. D. Ye, "Ultrahigh Bias Stability of ALD $In_2O_3$ FETs Enabled by High Temperature $O_2$ Annealing," 2023 IEEE Symposium on VLSI Technology and Circuits

(VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185292.

[5] C. Niu, Z. Lin, Z. Zhang, P. Tan, M. Si, Z. Shang, Y. Zhang, H. Wang and P. D. Ye., "Record-Low Metal to Semiconductor Contact Resistance in Atomic-Layer-Deposited $In_2O_3$ TFTs Reaching the Quantum Limit," 2023 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2023, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413708.

[6] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," Nature Electron., vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: 10.1038/s41928-022-00718-w.

[7] A. Charnas, Z. Zhang, Z. Lin, D. Zheng, J. Zhang, M. Si, P. D. Ye, " Review—Extremely Thin Amorphous Indium Oxide Transistors," Advanced Materials, vol. 36, no. 9, pp. 2304044, March 2024, doi: 10.1002/adma.202304044.

[8] N. Kimizuka et al., "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-/spl mu/m gate CMOS generation," 2000 Symposium on VLSI Technology. Digest of Technical Papers, Honolulu, HI, USA, 2000, pp. 92-93, doi: 10.1109/VLSIT.2000.852782.

[9] V. Huard, M. Denais, F. Perrier, N. Revil, C. Parthasarathy, A. Bravaix, E. Vincent, " A thorough investigation of MOSFETs NBTI degradation," Microelectronics Reliability, vol. 45, no. 1, pp. 83-98, January 2005, doi: 10.1016/j.microrel.2004.04.027.

[10] T. Seo, C. Jin and Y. Chung, "First Observation of Time Exponent Variations under Positive bias Stress on a-IGZO Transistors Utilizing Ultrafast On-the-Fly Technique with 1 μs Delay," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2, doi: 10.1109/VLSITechnologyandCir46783.2024.10631423.

[11] A. E. Islam, E. N. Kumar, H. Das, S. Purawat, V. Maheta, H. Aono, E. Murakami, S. Mahapatra, and M.A. Alam, "Theory and Practice of On-the-fly and Ultra-fast VT Measurements for NBTI Degradation: Challenges and Opportunities," 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 2007, pp. 805-808, doi: 10.1109/IEDM.2007.4419070.

[12] E. N. Kumar, E. N. Kumar, V. D. Maheta, S. Purawat, A. E. Islam, C. Olsen, K. Ahmed, M. A. Alam and S. Mahapatra, "Material Dependence of NBTI Physical Mechanism in Silicon Oxynitride (SiON) p-MOSFETs: A Comprehensive Study by Ultra-Fast On-The-Fly (UF-OTF) IDLIN Technique," 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 2007, pp. 809-812, doi: 10.1109/IEDM.2007.4419071.

[13] M. S. Rahman, A. Sarkar, D. R DeSilva, A. T. Harrison, Y. H. Kuo, J. Chen, A. I. Khan, and T. Roy, "Accurate Bias Stress Instability Measurements in High-Performance ITO FETs using Modified On-the-Fly Technique," in IEEE Electron Device Letters, doi: 10.1109/LED.2025.3554214.

[14] G. Liu, Z. Zhang, D. H. Trinh, H. Li, Q. Kong, C. Sun, Z. Zhou, D. Zhang, X. Wang, K. Han, Y. Kang, B. Y. Nguyen, K. Ni, G. Liang, and X. Gong, "Revealing the Impact of Hydrogen (H) on NBTI/PBTI of IGZTO FETs Under DC and AC Stress: Deep Dive into H Dynamics and Advanced Modeling," 2024 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4, doi: 10.1109/IEDM50854.2024.10873553.

[15] S. Wahid, A. Daus, J. Kwon, S. Qin, J.-S. Ko, H.-S. P. Wong, and E. Pop, "Effect of top-gate dielectric deposition on the performance of indium tin oxide transistors," IEEE Electron Device Lett., vol. 44, no. 6, pp. 951–954, Jun. 2023, doi: 10.1109/LED.2023.3265316.

[16] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed. New York, NY, USA : Wiley, 2006, p. 337, doi: 10.1002/0470068329.

[17] S. Mahapatra, N. Goel, A. Chaudhary, K. Joshi, and S. Mukhopadhyay, "Characterization methods for BTI degradation and associated gate insulator defects," in Fundamentals of Bias Temperature Instability, Springer Series in Advanced Microelectronics, vol 52. New Delhi, india: Springer, 2016, pp. 43–92. doi: 10.1007/978-81-322-2508-9_2.

[18] C. Niu , Z. Lin , V. Askarpour , Z. Zhang , P. Tan, M. Si, Z. Shang, Y. Zhang, H. Wang, M. S. Lundstrom, J. Maassen , and P. D. Ye, "Surface Accumulation Induced Negative Schottky Barrier and Ultralow Contact Resistance in Atomic-Layer-Deposited $In_2O_3$ Thin-Film Transistors," in IEEE Transactions on Electron Devices, vol. 71, no. 5, pp. 3403-3410, May 2024, doi: 10.1109/TED.2024.3367312.

[19] C.-A. Shih, M. M. F. Islam, S. Lee, P. D. Ye and M. A. Alam, "Asymmetric Reliability and Universality of Defect Formation in Oxide-Gated Ultra-Thin $In_2O_3$ Vertical FETs for Monolithic 3-D Integration," 2025 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2025, pp. 1-6, doi: 10.1109/IRPS48204.2025.10982725.

[20] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretchedexponential time dependence of charge injection and trapping in amorphous thin-film transistors," Applied Physics Letters, vol. 62, no. 11, pp. 1286–1288, 1993, doi: 10.1063/1.108709.

[21] T. Tomita, K. Yamashita, Y. Hayafuji, H. Adachi, "The origin of n-type conductivity in undoped $In_2O_3$," Applied Physics Letters, vol. 87, no. 5, pp. 051911, August 2005, doi: 10.1063/1.2001741.