Exploration of Interplay between Charge Trapping Dynamics and Polarization Switching in α-In_2Se_3 Ferroelectric Semiconductor FETs

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***Abstract*—The trap behavior in a two-dimensional (2D) ferroelectric semiconductor (FeS) field-effect transistors (FETs) that can overcome the device scaling limit of conventional ferroelectric FETs was analyzed. The conventional ferroelectric FETs exhibit a counterclockwise hysteresis loop, whereas ferroelectric channel-based FETs with high effective oxide thickness exhibit a clockwise hysteresis loop. Therefore, it is challenging to determine the contribution of ferroelectric polarization switching and trap states to the current conduction of FeS-FETs and to quantify their respective impacts, owing to their complex interaction. The modified conductance method with a four-element equivalent circuit model was employed to analyze the behavior of intrinsic trap states, with parasitic capacitance de-embedded, depending on the FeS polarization switching states. As a result, we confirmed that over the full energy range trap density can be extracted by unique characteristics of FeS-FETs. The retention characteristic was maintained at over 70 % of the initial memory on/off ratio when extrapolated to 10^4 s. Based on these results, guidelines for undefined trap state behavior of 2D α-In_2Se_3 FeS-FETs were presented.**

***Index Terms*—Alpha-indium selenide (α-In_2Se_3), ferroelectric semiconductor field-effect transistors (FeS-FETs), intrinsic trap states (D_{trap}), modified conductance method (MCM), nonvolatile memory device.**

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I. Introduction

In_2Se_3 exhibits ferroelectricity in the α-/β-phase. In particular, α-In_2Se_3 demonstrates interlocking between out-of-plane (OOP) and in-plane (IP) polarization at room temperature, resulting in strong spontaneous polarization [1], [2], [3], [4], [5]. OOP and IP polarizations can be controlled by both planar and vertical electric fields, making α-In_2Se_3 suitable for multiterminal device applications, unlike other ferroelectrics that only have controllable OOP polarization [6], [7], [8]. In addition, α-In_2Se_3 is a two-dimensional (2D) material with a bandgap energy of 1.46 eV, characterized by its ultrathin geometry, free dangling bonds across the interface, easy manipulation for integration with other materials, and no limit of critical thickness, which is the primary problem in conventional ferroelectric films [9], [10], [11], [12]. α-In_2Se_3 is expected to provide a solution to nonvolatile memory applications currently facing scaling limitations. However, unlike conventional ferroelectric field-effect transistors (FETs), which have a counterclockwise hysteresis loop, ferroelectric-semiconductor (FeS)-FETs with high effective oxide thickness (EOT) have a clockwise hysteresis loop [13]; thus, the hysteresis direction in FeS-FETs reflects the combined influence of both trap states and ferroelectric polarization switching. Therefore, accurate analysis of trap states is necessary to address the performance degradation and confusion in the device's operation, for example, threshold voltage instability, memory window reduction, and on/off ratio lowering [14], [15]. Nevertheless, α-In_2Se_3 is still in the early stages of research, hence, the specific characterization of the device's properties is yet to be fully established. In this work, for the first time, we quantitatively analyzed the intrinsic trap density of α-In_2Se_3 FeS-FETs after de-embedding parasitic capacitance based on the modified conductance method (MCM), in consideration of the unique operation mechanism of α-In_2Se_3 FeS-FETs.

II. Experiments

Fig. 1(a) depicts a schematic of the device, which indicates both the down and up states of ferroelectric polarization. The optical microscopy (OM) image of fabricated α-In_2Se_3 FeS-FETs can be shown in the inset image. α-In_2Se_3 flakes were transferred by using a mechanical exfoliation method on a 100 nm-SiO_2/p^+-Si substrate. The channel width (W) and length

(L) of the α-In_2Se_3 FeS-FETs were 6 μm and 4 μm, respectively. The thickness of the transferred flake was confirmed to be 40 nm by using the atomic force microscopy (AFM) line profile, as shown in Fig. 1(b). Subsequently, Ti/Ni (10/70 nm) was deposited via e-beam evaporation as source (S) and drain (D) contacts, patterned by the photolithography process. The current–voltage (I–V) and capacitance–voltage (C–V) characteristics of the fabricated α-In_2Se_3 FeS-FETs were measured by a semiconductor parameter analyzer (Keithley 4200A-SCS) and Agilent E4980A LCR meter, respectively.

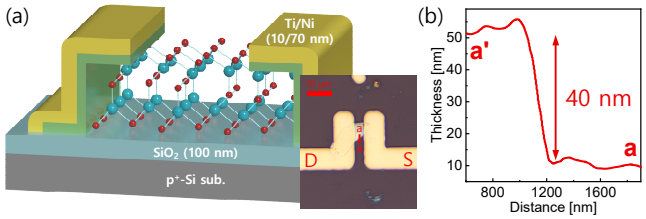

Fig. 1. (a) Device schematic reflecting polarization-down and -up states of the ferroelectric channel material with inset OM image and (b) AFM line profile of α-In_2Se_3 flake.

III. Results and Discussion

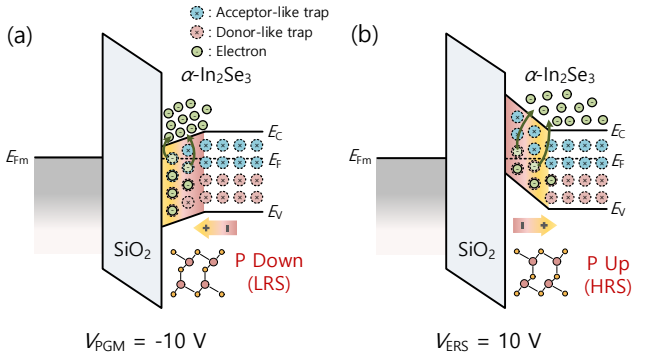

Fig. 2. Energy band diagram of α-In_2Se_3 FeS-FETs at ferroelectric (a) polarization-down state and (b) polarization-up state, which indicates the behavior of trap state.

Figs. 2(a) and (b) show the energy band diagram of α-In_2Se_3 FeS-FETs at ferroelectric polarization-down and -up states, respectively. In the partially polarization-down state induced by a negative gate bias (V_{GS}), band bending due to the polarization charge increases the density of free carriers near the insulator/channel interface, inducing a low resistance state (LRS) in FeS-FETs with high EOT gate oxide. Concurrently, band bending caused by an internal electric field due to the polarization charge enhances the predominance of acceptor-like trap behavior. Conversely, when positive V_{GS} was applied, the polarization was partially switched to upstate. Owing to the band bending by the internal electric field caused by the polarization charge, the free carrier near the insulator/channel interface is depleted and also donor-like trap behavior is dominated. In addition, free carriers could not be accumulated on the top side of the channel by the high EOT, resulting in a high resistance state (HRS).

Fig. 3(a) shows the transfer characteristics of the α-In_2Se_3 FeS-FETs, which indicate a clockwise gate hysteresis loop, reflecting the unique operation mechanism mentioned above. The multifrequency C–V curve is shown in Fig. 3(b). Free carriers were excited from the channel trap states by the frequency and V_{GS}, enabling the quantitative extraction of trap states according to the frequency dispersion. The parallel mode capacitance-conductance (C_m–G_m) was obtained from the measured capacitance-dissipation factor (C_m–D_m) using the following equation:

$$D_m = 1/\omega C_m R_m \quad (1)$$

$$G_m = 1/R_m \quad (2)$$

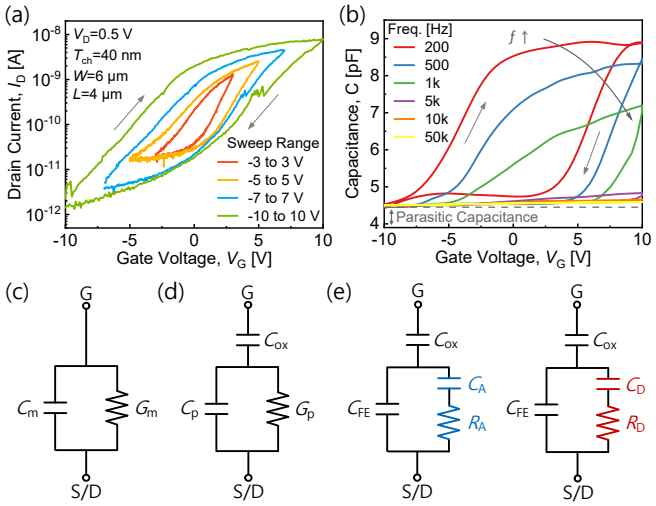

Fig. 3. (a) Transfer characteristics and (b) frequency-dispersive C–V curve of fabricated α-In_2Se_3 FeS-FETs. Equivalent circuit model of (c) a two-element model for the parallel mode C_m–G_m, (d) a three-element model for the C_{ox} including parallel mode C_p–G_p, and (e) a four-element model for the C_{ox} including parallel mode C_{FE}–C_A/R_A or –C_D/R_D according to polarization switching states.

As presented in Figs. 3(c) and (d), C_m–G_m was converted into oxide capacitance (C_{ox}) and parallel capacitance–conductance (C_p–G_p). Subsequently, depending on the polarization switching states, C_p–G_p was converted into frequency-dependent acceptor- or donor-like trap capacitance (C_A or C_D)/resistance (R_A or R_D), which are physical parameters related to the capture and emission of free carriers, in parallel with the α-In_2Se_3 ferroelectric channel capacitance (C_{FE}), shown in Fig. 3(e). The intrinsic capacitance ($C_{m,int}$) without parasitic capacitance (C_{par}), which is inevitably included because of the S/D metal overlap region, was calculated from the measured C–V curves [16]. G_p/ω was calculated as the following equation:

$$C_{m,int} = C_m - C_{par}\ [\mathrm{F}] \quad (3)$$

$$\frac{G_p}{\omega} = \frac{\omega G_{m,int} C_{ox}^2}{G_{m,int}^2 + \omega^2 (C_{ox} - C_{m,int})^2} = \frac{q\omega\tau_{trap} D_{trap}}{1 + (\omega\tau_{trap})^2}\ [\mathrm{S \cdot s}] \quad (4)$$

Here, $G_{m,int}$ is the intrinsic conductance; D_{trap} is the intrinsic trap density, which represents either acceptor-like trap density ($D_A(E)$) or donor-like trap density ($D_D(E)$), depending on the polarization switching state; τ_{trap} ($=R_{trap} \cdot C_{trap}$) is the time constant; and ω ($=2\pi f$) is the angular frequency. The obtained G_p/ω was plotted as a function of ω, shown in Figs. 4(a) and 4(b) at polarization-down and -up states, respectively. D_{trap} is obtained from the maximum value of G_p/ω at $\omega = 1/\tau_{trap}$ as follows:

$$C_{trap} = \frac{2 \times G_{p,max}}{\omega} \quad (5)$$

$$D_{\text{trap}} = \frac{(dQ_{\text{trap}}(E)/dE)}{W \times L \times T_{\text{ch}}} = \frac{(dQ_{\text{trap}}(E)/dV_{\text{G}})}{W \times L \times T_{\text{ch}} \times q}$$
$$= \frac{C_{\text{trap}}}{W \times L \times T_{\text{ch}} \times q} \ [\text{cm}^{-3} \cdot \text{eV}^{-1}] \quad (6)$$

The extracted and characterized by energy distribution D_{trap} profiles, with the frequency- and V_{GS}-dependent trapped charge (Q_{trap}) inside the energy bandgap, are shown in Fig. 4(c) as a function of surface potential ($\psi_{\text{S,A}}$ and $\psi_{\text{S,D}}$) as expressed in (7) and (8), respectively:

$$\psi_{\text{S,A}} = \int_{V_{\text{FB}}}^{V_{\text{on}}} (1 - \frac{C_{\text{m,int}}}{C_{\text{ox}}}) dV_{\text{G}} \ [\text{eV}] \quad (7)$$

$$\psi_{\text{S,D}} = \int_{V_{\text{FB}}}^{V_{\text{off}}} (1 - \frac{C_{\text{m,int}}}{C_{\text{ox}}}) dV_{\text{G}} \ [\text{eV}] \quad (8)$$

Herein, the $\psi_{\text{S,A}}$ and $\psi_{\text{S,D}}$ was calculated from the flat band voltage to the voltage representing the on and off states in both LRS and HRS. In LRS, integration proceeded in a positive direction, while in HRS, it proceeded in the negative direction, mapping to the energy levels near the conduction and valence band, respectively. The ψ_{S} corresponding to the voltage range, where the effective G_{p}/ω peak appears, was used to represent D_{trap} within the subgap energy region. $D_{\text{A}}(E)$ and $D_{\text{D}}(E)$ were extracted from 2.79×10^{19} $\text{cm}^{-3}\text{eV}^{-1}$ to 2.94×10^{19} $\text{cm}^{-3}\text{eV}^{-1}$ and from 1.57×10^{16} $\text{cm}^{-3}\text{eV}^{-1}$ to 2.04×10^{16} $\text{cm}^{-3}\text{eV}^{-1}$ at polarization-down and -up states, respectively, within the subgap energy range. We note that the interface and bulk traps have a high density near the conduction band (E_{C}) and valence band (E_{V}) rather than near the midgap energy [17], resulting in the order of magnitude difference between $D_{\text{A}}(E)$ and $D_{\text{D}}(E)$.

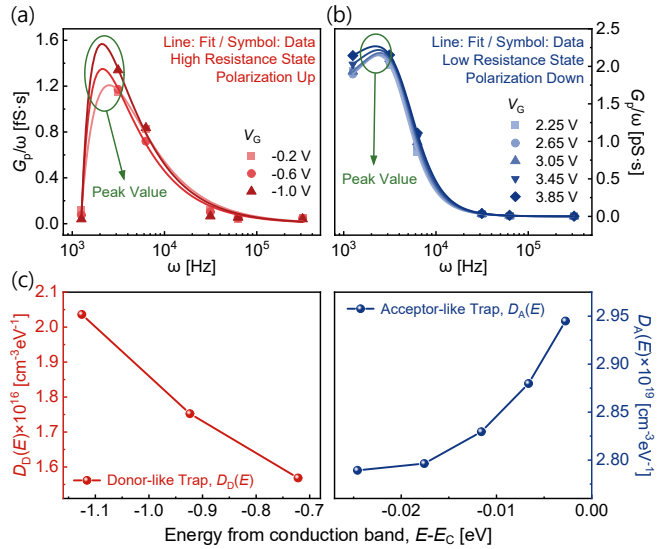

Fig. 4. The obtained G_{p}/ω from the MCM with a four-element model at (a) polarization-up and (b) -down states, respectively. (c) The D_{trap} was extracted separately for donor-like traps near the E_{V} and acceptor-like traps near the E_{C}, considering polarization switching states.

The retention and endurance characteristics for investigating the ferroelectric memory device reliability of the α-In_2Se_3 FeS-FETs were measured and shown in Fig. 5. In the retention characteristics, when linearly extrapolated to 10^4 s, the LRS and HRS states remained over 70 % compared to the initial data. The endurance characteristics were measured with the program and erase repeated at -10 V and 10 V, respectively. The LRS and HRS states of fabricated FeS-FETs were maintained over the 10^3 program/erase cycles under various operation temperatures of 65 ℃, 85 ℃, and 105 ℃.

It's noteworthy that band bending caused by ferroelectric polarization charge determines the types of trap states, which affect the transfer characteristics of FeS-FETs. Hence, trap states were extracted at polarization-down and -up states using the frequency-dispersive conductance method excluding parasitic capacitance. The energy profile of trap states can be extracted using C–V characteristics that precisely measure the time constant by examining the trapping/de-trapping speed of traps through frequency-dependent behaviors. Thus, C–V-based trap analysis techniques are suitable for an intuitive, quantitative, and accurate evaluation of the spatial distribution of trap states compared to the I–V-based analysis method. Therefore, the proposed technique in this study is expected to be extensively utilized for analyzing trap states in FeS-FETs. While this study provides critical insight into the role of electrically active traps associated with polarization switching, further studies are required to clarify the correlation between the physical mechanisms and electrical characteristics, considering device geometry and polarization switching behavior.

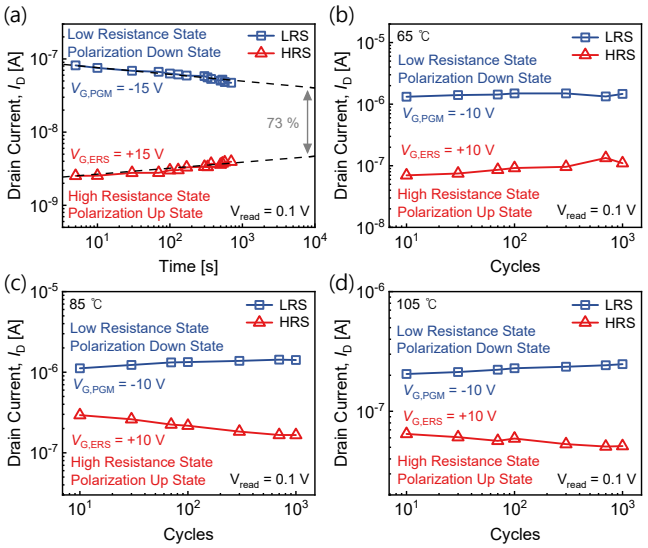

Fig. 5. (a) Extrapolated retention time up to 10^4 s and endurance characteristics for 10^3 cycles under (b) 65 °C, (c) 85 °C, and (d) 105 °C for investigating the reliability of ferroelectric memory device.

IV. Conclusion

In this work, for the first time, the trap states behavior of 2D ferroelectric α-In_2Se_3 FeS-FETs was investigated through the frequency-dispersive C–V characteristics de-embedding the C_{par}. The acceptor- and donor-like trap density in the polarization-down and -up states were extracted over the full range of subgap energy levels in high EOT α-In_2Se_3 FeS-FETs. We expect that the proposed technique will become an effective tool for analyzing the unique behavior of trap density in FeS-FETs, which have not yet been fully understood.

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