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# Positive Bias Temperature Instability and Hot Carrier Degradation of Back-End-of-Line, nm-Thick, $In_2O_3$ Thin-Film Transistors

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***Abstract*— Recently, back-end-of-line (BEOL) compatible indium oxide ($In_2O_3$) thin-film transistors (TFTs), grown by atomic layer deposition (ALD) with channel thickness of ~1 nm and channel length down to 40 nm, have achieved a record high drain current of 2.2 A/mm at $V_{DS}$ of 0.7 V. A systematic characterization of the reliability issues, such as positive bias temperature stress (PBTS) and hot carrier degradation (HCD), would allow its immediate integration into innovative ICs, such as 3D-stacked SRAM or on-chip bridge for mixed-voltage systems. Surprisingly, PBTS and HCD are both characterized by a universal two-stage threshold voltage shift ($\Delta V_{th}$, a positive shift followed by a temperature-activated negative shift). This is attributed respectively to electron trapping/trap-generation and hydrogen-assisted formation of positive donor-traps. These competing mechanisms of $\Delta V_{th}$ depend on the stress voltages and stress temperature. Unlike traditional logic transistors, HCD in BEOL-TFTs is strongly correlated to PBTS, caused by the much stronger vertical field in an ultra-thin device. Overall, this high-performance BEOL-transistor is remarkably reliable, with a relatively small $\Delta V_{th}$ under PBTS/HCD stress conditions at room temperature (RT). However, self- and mutual heating of BEOL levels and the resultant threshold voltage variability must be mitigated/managed for its successful integration in various neuromorphic circuits.**

***Index Terms*— Thin-film transistors (TFTs), atomic layer deposition (ALD), hot carrier degradation (HCD), positive bias temperature stress (PBTS), oxide semiconductors**

## I. Introduction

There has been a surging interest in integrating thin-film transistors (TFTs), resistors, and memory elements within the metal-insulator back-end-of-line (BEOL) stack such as 3D DRAM [1], 3D one transistor-one resistor (1T-1R) RRAM array [2], 3D field-programmable gate array (FPGA) [3] for applications in traditional and in-memory computing. Amorphous oxide semiconductor (AOS) TFTs are of great interest for advanced display applications because of their transparency, higher mobility, and steeper subthreshold slope (SS) compared to amorphous-Si (a-Si) TFTs [4]. Among those AOSs, amorphous In-Ga-Zn-O (a-IGZO) TFTs, which can be deposited by sputtering [5] or atomic layer deposition (ALD) [6], are widely adopted in display circuits. The use of compositionally simpler $In_2O_3$ TFTs was hindered by the unstable electrical properties of the films deposited by sputtering (because it forms poly-crystalline films) and the difficulty in operating the transistor in enhancement mode (oxygen-deficiency makes the film intrinsically n-type) [7].

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Fortunately, these persistent challenges have recently been addressed by Si et al. with ALD-grown amorphous $In_2O_3$ TFT with the channel thickness of 1.5-0.7 nm and the channel length scaled down to 40 nm [8]. These ALD-grown transistors demonstrate excellent mobility (> 100 $cm^2V^{-1}s^{-1}$) [9], low subthreshold slope (65 mV/dec) [10], and tunable threshold voltage ($V_{th}$) between $-4$ and 5 V [11]. As an enhancement mode TFT, the record high current density of 2.2 A/mm at $V_{DS}$ of 0.7 V was reported [10]. These performance metrics establish $In_2O_3$ TFT as a promising technology for BEOL integration. It remains to be seen, however, if the technology is sufficiently reliable to make this integration practical.

In this letter, we characterize the $V_{th}$ instability of these transistors under positive bias temperature stress (PBTS) and hot carrier degradation (HCD). It is well known that PBTS and HCD are the two dominant reliability challenges of this class of TFTs. Given its sub-nm ultra-thin channel, we expect the degradation physics to be substantially different compared to traditional front-end logic transistors (e.g., FinFET) or other thin-film technologies (e.g., a-IGZO TFTs).

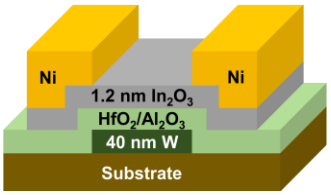


Fig. 1. The schematic of the bottom-gate $In_2O_3$ TFT under study.

## II. Experimental Observations

### A. Experiment Setup

As depicted in Fig. 1, the bottom-gate TFTs have 10 nm of $HfO_2$, 1 nm of $Al_2O_3$ as the gate dielectric, and 1.2-nm-thick $In_2O_3$ as the channel material. The channel width ($W$) is 11.1 μm, and the channel length ($L_{ch}$) of 10 μm are examined throughout this paper. The detailed fabrication process can be found in Ref. [11]. The stress voltages range from $V_G$ = 4-6 V, and $V_D$ = 8-9 V, for a temperature range of 20-80 °C, a typical range of temperatures in self-heated BEOL interconnects [12]. PBTS tests are conducted with source and drain grounded, and the gate contact is positively biased. The PBTS (HCD) stress is intermittently interrupted by $I_D$-$V_G$ sweeps at $V_{DS}$ = 0.05 V (1

V). $\Delta V_{th}$ is obtained by the constant current method at 1 nA $\times (W/L)$.

### B. Experimental Observations

Fig. 2 summarizes $V_{th}$ shift ($\Delta V_{th}$) results of temperature- and field-dependent PBTS [first row, Fig. 2(a)(b)] and HCD [second row, Fig. 2(c)(d)]. It is noteworthy that, in traditional silicon transistors, $\Delta V_{th}$ due to PBTS is always positive due to electron trapping [13]. However, Fig. 2(a) shows that under low-stress PBTS ($V_G = 4$, 5 V), the TFTs are characterized by an anomalous negative-to-positive turn-over in $\Delta V_{th}$, while the high-stress case ($V_G = 6$ V) shows a fast positive $\Delta V_{th}$, characterized by a logarithmic time-dependent degradation. A similar trend has been reported for a-IGZO transistors [14]. For a given stress voltage (e.g., $V_G = 6$ V), the temperature-dependent PBTS shown in Fig. 2(b) are also characterized by an anomalous positive-to-negative $\Delta V_{th}$ with increasing temperature. To summarize, PBTS-induced $\Delta V_{th}$ in $In_2O_3$ TFTs can be characterized by a two-stage (negative to positive or positive to negative) degradation. This two-stage degradation have also been reported for other TFTs [14]–[17].

Fig. 2(c) shows $\Delta V_{th}(t)$ in a log-log scale for HCD as the transistors are stressed with different $V_G/V_D$ combinations. It is clear that higher $V_G$ stress (6 V) shows a distinct behavior with a higher degradation level at an early stage compared to lower $V_G$ stress (4 and 5 V). This abrupt transition at higher $V_G$ stress is similar to the PBTS transition at similar gate voltage, as in Fig. 2(a). Fig. 2(d) reveals that temperature-dependent HCD shows a positive to negative $\Delta V_{th}$ with increasing temperature, similar to that of PBTS. As an aside, this is the first report of HCD in BEOL-integrated transistors and its correlation to PBTS degradation. The similarity of PBTS and HCD in terms of voltage and temperature dependence suggests that similar mechanisms may be driving this phenomenon.

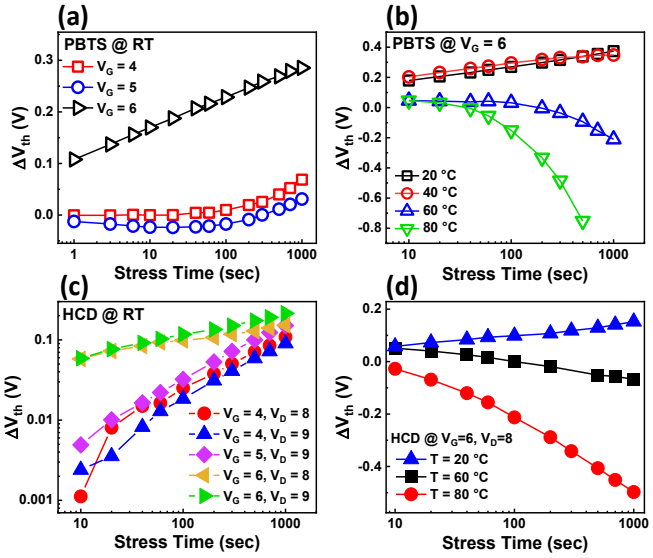


Fig. 2. $\Delta V_{th}(t)$ in various PBTS conditions in semi-log scale at (a) room temperature (RT) and (b) elevated temperatures. And $\Delta V_{th}(t)$ in various HCD conditions in log-log scale at (c) RT and (d) elevated temperatures.

## III. Theory and Modeling

It has been suggested that the two-stage $\Delta V_{th}$ of a-IGZO TFTs may be interpreted by a two-component degradation: a positive $\Delta V_{th}$ is attributed to electron trapping at the channel/oxide interface ($N_{it}$) and/or into oxide ($N_{ot}$) [18], [19], and a negative $\Delta V_{th}$ variously correlated to accumulation of positive ions at the semiconductor/oxide interface [20] or formation the donor-like traps through the interaction with hydrogen (H) [15], [16], oxygen ($O_2$) [21], or water ($H_2O$) molecule [14], [17]. Our analysis below shows that the consistent interpretation of the dataset in Fig. 2 is only possible if $\Delta V_{th}$ involves a correlated sum of of *three components*, i.e.,

$$\Delta V_{th}(t) \equiv V_{it}^{+}(t) + V_{tr}^{+}(t) - V_{dt}^{-}(t) = \left[A_{it}t^{n} + B_{tr}\log\left(\frac{t}{\tau_{\mathrm{tr}}}\right)\right] - C_{dt}\left(1 - e^{-\left(\frac{t}{\tau_{dt}}\right)^{\beta}}\right), \quad (1)$$

where $A_{it}$, $B_{tr}$, $C_{dt}$ are voltage- and temperature-dependent prefactors of interface trap generation, electron trapping in existing states, and donor-trap formation, respectively. The corresponding characteristic time-scale factors, $\tau_{tr}$ and $\tau_{dt}$, also depend on voltage and temperature, but power exponent $n$ and $\beta$ must not. The stretched exponential functional form for donor-trap formation is empirical, but the general form and the exponent $\beta$ can be justified physically. We exclude $H_2O$ or $O_2$ as potential sources of degradation because passivated and unpassivated samples show similar degradation. As proposed in Ref [15], hydrogen can be released from $Al_2O_3$ and react with $O_2^-$ (in $In_2O_3$), producing $OH^-$ and $e^-$ and creating shallow donor levels at the oxide/semiconductor interface.

Next, we use Eq. (1) to fit the experimental data shown in Fig. 2 to decouple the components due to interface trap generation, electron trapping in existing states, and donor-trap formation. Fig. 3(a) shows that for high-voltage PBTS ($V_G$ =6 V) at 40 °C, $\Delta V_{th}(t, \mathrm{high}) \sim V_{tr}^{+(t)} - V_{dt}^{-}(t)$. Here, $V_{tr}^{+} \equiv B_{tr}\log\left(\frac{t}{\tau_{\mathrm{tr}}}\right)$, which increases rapidly when the increasing vertical electric field exponentially increases the (weakly temperature-dependent) tunneling current into the oxide. Similar results have been reported in Ref. [18] for a-IGZO TFTs. The negative (donor-trap) contribution, $V_{dt}^{-}(t)$, is relatively small at RT (Fig. 3(a), dashed line) but it enhances rapidly (Fig. 3(b), dashed line) as the temperature rises from 40 to 80 °C. This indicates a *strong field and temperature activation of the donor-trap formation*, i.e., $\tau_{dt}(T) = \tau_0 \exp\left(\frac{E_\tau}{kT}\right)$ [19] ($\tau_0$ =47.2 μs and $E_\tau$ =0.48 eV are determined by fitting, which is close to 0.52 and 0.63 eV reported in Ref. [16]). One possible explanation is the enhanced release of hydrogen atoms from $Al_2O_3$ at a higher $V_G$, given the high hydrogen concentration in low-temperature ALD $Al_2O_3$ [22]. And the elevated temperature accelerates the chemical reaction of creating shallow donor levels. At lower stress voltage ($V_G = 4, 5$ V), however, reduced vertical field exponentially suppresses $V_{tr}^{+}(t)$, and the interface trap generation $V_{it}^{+}(t)$ dominates the long term degradation. In other words, $\Delta V_{th}(t; low) \sim V_{it}^{+}(t) - V_{dt}^{-}(t)$.

Fig. 3(c)(d) show that HCD at various $V_G$ and $V_D$ combinations can likewise be interpreted in terms of Eq. (1).

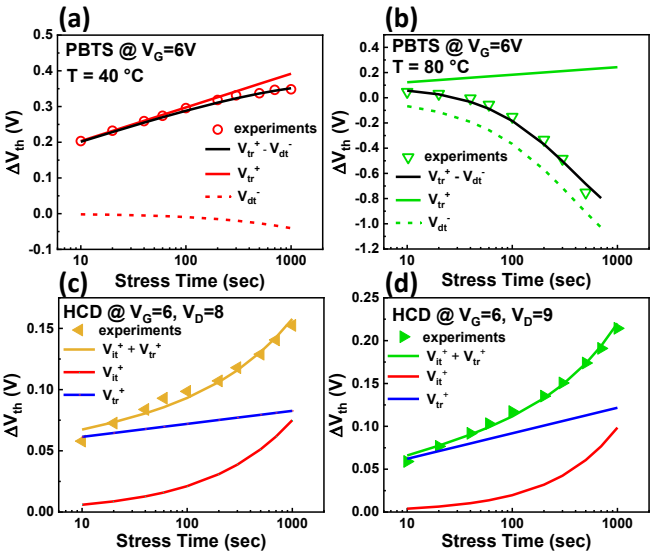


Fig. 3. The decomposition of $\Delta V_{th}(t)$ of PBTS with $V_G$ =6 (a) at 40 °C and (b) 80 °C. Also, $\Delta V_{th}(t)$ of HCD at RT with (c) $V_G$ =6, $V_D$ = 8 and (d) $V_G$ =6, $V_D$ = 9, showing the dominance of PBTS during HCD at RT.

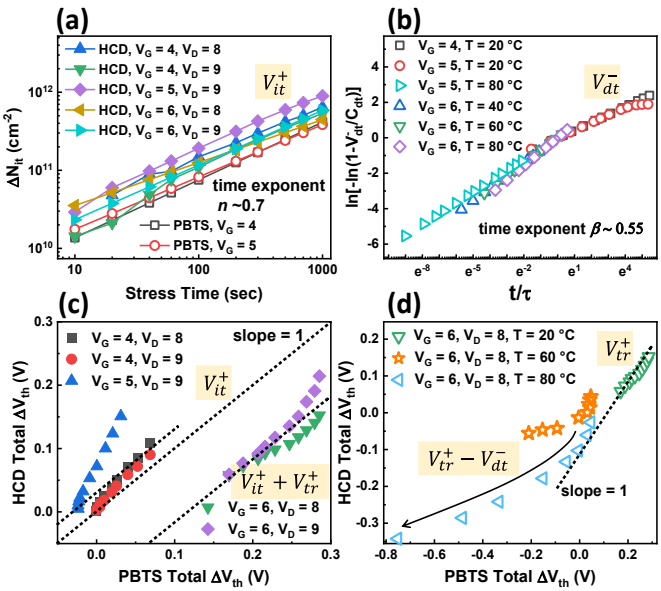


Fig. 4. (a) $\Delta N_{it}$ calculated from decoupled $V_{it}^+$ from both PBTS and HCD tests. (b) Decoupled $V_{dt}^-$ in the Weibull plot. The comparison of total $\Delta V_{th}$ under PBTS and HCD at (c) RT and (d) elevated temperatures. The corresponding components are annotated.

Specifically, $\Delta V_{th}(t, \text{low}) \sim V_{it}^+(t)$ as is typical for traditional MOSFETs [23], [24]. However, at high enough $V_G$ stress, PBTS-assisted $V_{tr}^+(t)$ dominates. The $V_{dt}^-(t)$ component must be present due to the PBTS-like stress, but is overwhelmed by $V_{it}^+(t)$ and $V_{tr}^+(t)$ components at RT. In brief, the decompositions demonstrate that Eq. (1) describes both PBTS and HCD as various combinations of the three degradation components.

Fig. 4(a) shows that the interface trap generation ($\Delta N_{it}$) calculated from decomposed $V_{it}^+$ terms ($V_{it}^+ = q\Delta N_{it}/C_{ox}$) can be characterized by a voltage- and temperature-*independent* time exponent, $n \sim 0.7$. The universality of the time-exponent suggests that although the magnitude of the contribution ($A_{it}$) may be differently accelerated by PBTS vs. HCD, $\Delta N_{it}$ is governed by the same physical mechanism. Equally remarkable, $V_{dt}^-(t)$ component is given by a universal function, characterized by the voltage- and temperature-independent exponent ($\beta \sim 0.55$), as demonstrated by the Weibull plot in Fig. 4(b). In other words, the mechanics of donor-trap formation, regardless of the microscopic detail, are also universal. Interestingly, other types of TFTs fabricated with very different processes (e.g., sputtering vs. ALD, and top gate vs. bottom gate) are also characterized by $\beta = 0.44$ [14], $\beta = 0.66$ [15], and, $\beta = 0.59$ [17], suggesting an identical mechanism.

Despite the similarity of the underlying mechanisms, $V_{it}^+$, $V_{tr}^+$, and $V_{dt}^-$ contribute differently to PBTS and HCD tests. By comparing the total $\Delta V_{th}$ under HCD and PBTS at RT in Fig. 4(c), we find that at low voltage and RT, $\Delta V_{th}^{\text{HCD}} \gg \Delta V_{th}^{\text{PBTS}}$. However, at higher $V_G$, the dominance of electron trapping erases the gap, i.e., $\Delta V_{th}^{\text{HCD}} \sim \Delta V_{th}^{\text{PBTS}}$. Consequently, it defines the upper limit of the accelerated HCD tests for these TFTs. Finally, Fig. 4(d) shows a similar plot at higher temperatures, with a strong non-classical negative shift for both HCD and PBTS. Interestingly, PBTS induces a significantly more negative shift compared to HCD, making it deviate from the line of slope = 1. This is attributed to the higher and uniform vertical field ($E_y \gg E_x$) by strong PBTS, stemming from the ultra-thin channel relatively to its length: a critical distinction to the classical devices.

## CONCLUSIONS

We examined the reliability of 1.2-nm-thick ALD-grown $In_2O_3$ TFT as a promising BEOL-integrated transistor. We found that the two-stage $\Delta V_{th}$ under PBTS and HCD are correlated. They can be described by the combinations of three-component degradation (interface trap generation, oxide electron trapping, and donor-trap formation), as described in Eq. (1). The time-evolution of the degradation functions are essentially identical, defined by power exponents ($n \sim 0.7$, $\beta \sim 0.55$). Compared to other IGZO TFTs, such as [14]–[16], [25], our TFTs demonstrate an excellent $V_{th}$ stability at RT under 1000 seconds of PBTS ($\Delta V_{th} < 0.4$ V) and HCD ($\Delta V_{th} < 0.3$ V). Their strong/anomalous temperature-activated $\Delta V_{th}$, related to donor-trap formation, is a critical concern, especially when integrated with traditional transistors with substantial self-heating. Depending on the interconnect level, the temperature difference will reflect a rapid $V_{th}$ divergence. Overcoming the temperature sensitivity by suppressing the hydrogen-assisted donor-trap formation is the key challenge for future adoptions in modern integrated circuits.

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