

Capacitance-voltage Characterization of Atomic-Layer-Deposited Al₂O₃/InGaAs and Al₂O₃/GaAs Metal–Oxide-Semiconductor Structures

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ALD Al₂O₃/GaAs and Al₂O₃/In_{0.2}Ga_{0.8}As MOS and source-drain implanted MOSFET structure were fabricated and characterized by capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements. It is shown that, after high-temperature anneal, the MOS leakage current density of the thinner (16nm) film is much higher than that of the thicker (30nm) film. The high-quality Al₂O₃ (30nm)/In_{0.2}Ga_{0.8}As interface after high temperature anneal is verified by *C-V* curves showing sharp transition from depletion to accumulation with “zero” hysteresis, 1% frequency dispersion per decade at accumulation capacitance and strong inversion under split *C-V* measurement. However, Al₂O₃(16nm)/GaAs shows larger hysteresis and frequency dispersion with no inversion layer formed under split *C-V* measurement. Photo-assisted *C-V* measurement shows the inversion layer easily formed on In_{0.2}Ga_{0.8}As interface but not on GaAs interface, indicating higher surface recombination rate at GaAs interface. The estimated interface trap density (D_{it}) by split *C-V* method shows $2.9 \times 10^{11}/\text{cm}^2\text{-eV}$ for Al₂O₃/In_{0.2}Ga_{0.8}As. Minority-carrier response of Al₂O₃/In_{0.2}Ga_{0.8}As and Al₂O₃/GaAs is systematically studied by high-temperature *C-V* measurements which reveal the activation energy (E_A) of the minority-carrier recombination to be about 0.62 ± 0.03 eV for InGaAs and 0.71 ± 0.01 eV for GaAs, respectively.

Introduction

Silicon technology has already entered the regime of nanotechnology (<100 nm), and SiO₂ gate oxide has reached its physical limit. In order to continuously sustain Moore’s law in the future, it requires not only shrinking the device size but also the introduction of high-k gate dielectric, high mobility channel and new device structures for high-speed, high-performance and low power applications. Recently, there has been tremendous progress in the research of semiconductor-nanowire field-effect-transistors (FETs), carbon nanotube (CNT) FETs and III-V FETs devices because of their significantly higher intrinsic mobilities. Among them, both nanowires and CNTs are formed using “bottom-up” chemical synthesis. They are difficult to be placed reliably on the desired device positions. On the other hand, III-V

materials can be patterned into desirable device structure using conventional “top-down” technology [1]. III-V compound semiconductor industry has been existing for nearly three decades.

For more than four decades, the research community has been searching for suitable gate dielectrics or passivation layers on III-V compound semiconductors. There are tremendous efforts and many literatures in this field [2-14]. The main obstacle is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO₂ on Si, e.g., a mid-bandgap interface-trap density (D_{it}) of $\sim 10^{10}/\text{cm}^2\text{-eV}$. Unpinning the III-V surface Fermi level with low D_{it} is the key to the realization of high-performance III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs) with commercial values. Atomic-layer-deposited (ALD) high-k dielectrics on III-V are of particular interest, since the Si industry has already been familiar with ALD Hf-based dielectrics and this approach is becoming a viable production technology. Compared to the conventional methods of forming thin Al₂O₃ films, i.e., by sputtering, electron beam evaporation, chemical vapor deposition or oxidation of pure Al films, the ALD Al₂O₃ is of much higher quality. ALD is an ultra-thin-film deposition technique based on sequences of self-limiting surface reactions enabling thickness control on atomic scale. The ALD high-k materials are the leading candidates to substitute SiO₂ for 45 nm Si complimentary MOSFET applications. ALD also provides unique opportunity to high-quality gate dielectrics integration on non-Si semiconductor materials such as Ge, the leading high mobility channel material for future p-type MOSFETs [15].

Al₂O₃ is a widely used insulating material for gate dielectric, tunneling barrier and protection coating due to its excellent dielectric properties, strong adhesion to dissimilar materials, and its thermal and chemical stability. Al₂O₃ has a high bandgap (~ 9 eV), a high breakdown electric field (5-30 MV/cm),¹⁶ a high permittivity (8.6-10) and high thermal stability (up to at least 1000 °C) and remains amorphous under typical processing conditions such as implant activation.

In our previous work, we have succeeded in integrating ALD high-k dielectric Al₂O₃ on GaAs, InGaAs and GaN, and demonstrated high performance depletion-mode III-V MOSFETs [9,17-19] We have also demonstrated enhancement-mode (E-mode) inversion-type ALD Al₂O₃/InGaAs MOSFETs [20], which is of particular interests for very large scale integrated (VLSI) circuits or high-speed digital applications. In this paper, we report room-temperature capacitance-voltage ($C-V$), split $C-V$, photo-assisted $C-V$ and high-temperature $C-V$ measurements on high temperature annealed ALD Al₂O₃ dielectrics on InGaAs and GaAs.

Experiment

Figure 1 shows the cross-sectional view of the fabricated E-mode n-channel Al₂O₃/ In_{0.2}Ga_{0.8}As/GaAs (or GaAs) MOSFET and the capacitor to characterize the Al₂O₃ / InGaAs (or GaAs) interface. A 150 nm p-doped $4 \times 10^{17} / \text{cm}^3$ buffer layer, a 285 nm p-doped $1 \times 10^{17} / \text{cm}^3$ intermediate layer and a 13.5 nm p-doped $1 \times 10^{17} / \text{cm}^3$ In_{0.2}Ga_{0.8}As channel layer (or 300 nm p-doped $1 \times 10^{17} / \text{cm}^3$ GaAs channel layer) were sequentially grown by MOCVD

on a 2-inch GaAs p+ substrate. After appropriate surface pretreatment, 16 nm – 30nm ALD Al₂O₃ films were deposited at 300 °C using an ASM Pulsar2000™ ALD module. Trimethyl aluminum (Al(CH₃)₃) and water (H₂O) were used as precursors. The ALD Al₂O₃ is served not only as a gate dielectric but also as an encapsulation layer due to its high thermal and chemical stability. A 1.8 μm thick AZ1518 photoresist was used as a mask for the selective area Si-implantation for the source and drain contact regions and as protection layer for MOS capacitor region. After silicon implant the photoresist became hardened and in some cases difficult to strip. The implant-hardened photoresist was removed using Ar/O₂ plasma ashing followed by acetone and ethanol treatment. During the plasma ashing process, chamber pressure, plasma power and ashing time are optimized since plasma damage and impurities can be induced in the oxide film. The Si-dopant activation was carried out at 750 – 850 °C by rapid thermal annealing (RTA) in N₂ ambient for 10s-30s. Dopant activation/annealing is a very critical step which not only activates the dopant but also must preserve the smoothness of the interface at atomic level. After dopant activation, the oxide on the source and drain regions was removed using wet etch in diluted HF, while the gate area was protected by photoresist. Ohmic contacts were formed by electron-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 400 °C anneal in N₂ ambient. Finally, conventional Ti/Au metals were e-beam evaporated, followed by lift-off to form the gate electrodes. The process requires 4 levels of lithography (alignment, source and drain implantation, ohmic and gate), all done using a contact printer. The sheet resistance of the implanted source/drain region and its contact resistance are measured by transfer length method (TLM) to be ~ 300 Ω/sq. and ~ 1.0 Ω·mm, which demonstrates good process on implantation and activation. The designed gate lengths of the measured devices are 0.65, 0.85, 1, 2, 4, 8, 20 and 40 μm. The overlap length between gate and source/drain is estimated around ~ 0.5 μm or less. The diameter of the measured MOS capacitors is 75 μm. Capacitance-voltage measurements were carried out on an HP 4284A precision low capacitance resonance (LCR) meter and the Al₂O₃ film thickness was estimated by ellipsometry.

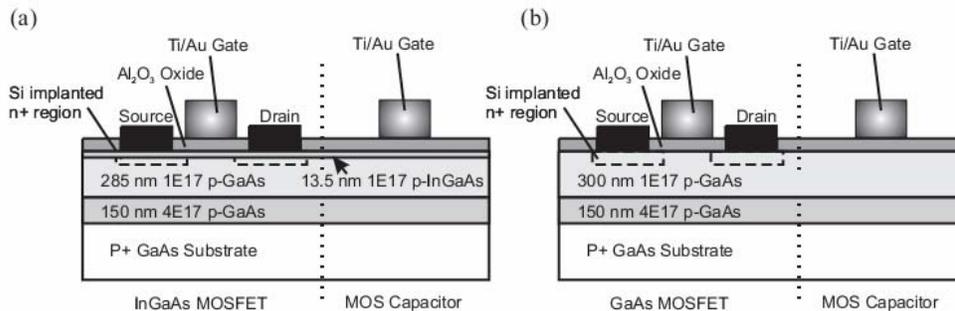


Fig. 1(a) Cross sections of an E-mode Al₂O₃/InGaAs MOSFET and MOS capacitor fabricated by the same process. (b) Cross sections of a similar Al₂O₃/GaAs MOSFET and MOS capacitor.

Results and Discussion

C-V Measurements of Al₂O₃/InGaAs and Al₂O₃/GaAs MOS Capacitor

The *C-V* measurements are widely used to quantitatively study the MOS structures. There are three important parameters in evaluating high-k dielectrics on novel channel materials. The first is the amount of *C-V* hysteresis when the MOS capacitor is biased well into accumulation and inversion region. The second is the interface trap density D_{it} showing the quality of surface passivation and dielectric formation. The third is the frequency dispersion on accumulation capacitances and the subsequent flat-band shifts.

We focus on the *C-V* characterization of ALD Al₂O₃ on InGaAs (and GaAs) after high temperature annealing between 750 °C –850 °C required to activate Si dopants in InGaAs (and GaAs). Note that better *C-V* curves or D_{it} might exhibit under annealing temperature between 450°C –600 °C under certain ambient or complicated annealing process. But it is not directly relevant to the MOS interface needed for realizing inversion-channel E-mode GaAs MOSFET using conventional self-aligned (gate-first) implanted process. The frequency dependence of the *C-V* curves for 30 nm ALD Al₂O₃ on InGaAs and 16 nm ALD Al₂O₃ on GaAs MOS capacitor are shown in Fig. 2(a) and Fig. 2(b), respectively. I-V characteristics of each MOS capacitors are also shown in Fig. 2(c) and Fig. 2(d), respectively. These capacitors went through all fabrication process and were annealed by RTA at 800 °C for 10 s in nitrogen ambient. The annealed 30nm Al₂O₃ films (Fig. 2(c)) shows very low leakage current density of about 10^{-8} A/cm² at 5MV/cm and the breakdown electrical field (E_{BR}) is 8.3 MV/cm, which is close to the reported bulk E_{BR} of (7-8 MV/cm). [16] It exhibits almost “zero” hysteresis in this *C-V* loop with maximum shift less than 20 mV from Figure 2(a). The typical hysteresis observed in this type of MOS devices is between 20 mV to 50 mV, corresponding to a slow trap density of about 5.0×10^{10} /cm²-eV to 1.25×10^{11} /cm²-eV. The extremely low hysteresis demonstrates the high quality of bulk properties of ALD Al₂O₃ on InGaAs even after high temperature annealing. However, the hysteresis of 16 nm Al₂O₃ on GaAs are larger, at about 100-200 mV from Figure 2(b), showing slow trap density of about 2.5×10^{11} /cm²-eV to 5.0×10^{11} /cm²-eV. There are two possible explanations for the larger hysteresis in the 16 nm Al₂O₃ on GaAs. The first is that the ashing process, in which longer ashing time was applied for photoresist removal on this specific sample, introduced plasma damage that results in the increase of hysteresis. The hysteresis of 16 nm Al₂O₃ on GaAs could be decreased to <100 mV after optimizing the ashing process (data not shown). The second is the degradation of Al₂O₃ film quality in thinner film (16nm) during 800 °C anneal. Fig. 2(d) shows the leakage current density of the 800 °C annealed 16nm Al₂O₃ films is about 4×10^{-4} A/cm² at 5MV/cm, which is 10^4 times higher than that of 30 nm Al₂O₃ on InGaAs. The breakdown electrical field (E_{BR}) is 4.4 MV/cm, about half of that of the 30 nm sample. The 16 nm Al₂O₃ film on both InGaAs and GaAs appears same order of leakage current density under 800 °C annealing indicate the possible Arsenic diffusion through thinner (16 nm) Al₂O₃ and degraded the insulator. The effects of the annealing step on chemical and structural properties of the interface are very complex and difficult to quantify in details. The general

observation of hysteresis on ALD Al_2O_3 on InGaAs (or GaAs) is following: (1) The unannealed (as-deposited) ALD Al_2O_3 usually exhibits a hysteresis of ~ 200 mV to 500 mV depending on n-type or p-type surfaces, surface pretreatment, ALD growth temperature and others. Slow traps dominate on unannealed MOS structures. (2) The RTA step improves the bulk and interface characteristics and reduces both slow and fast traps significantly. The most efficient annealing temperature is between 450°C – 600°C , depending on different channel materials and ambient conditions. (3) The bulk and interface properties start to degrade drastically after the RTA step with the annealing temperature higher than 800°C due to the inter-diffusion between Al_2O_3 and GaAs or InGaAs and As out-gasing from GaAs. The bulk properties of thinner Al_2O_3 degrade faster than thicker ones.

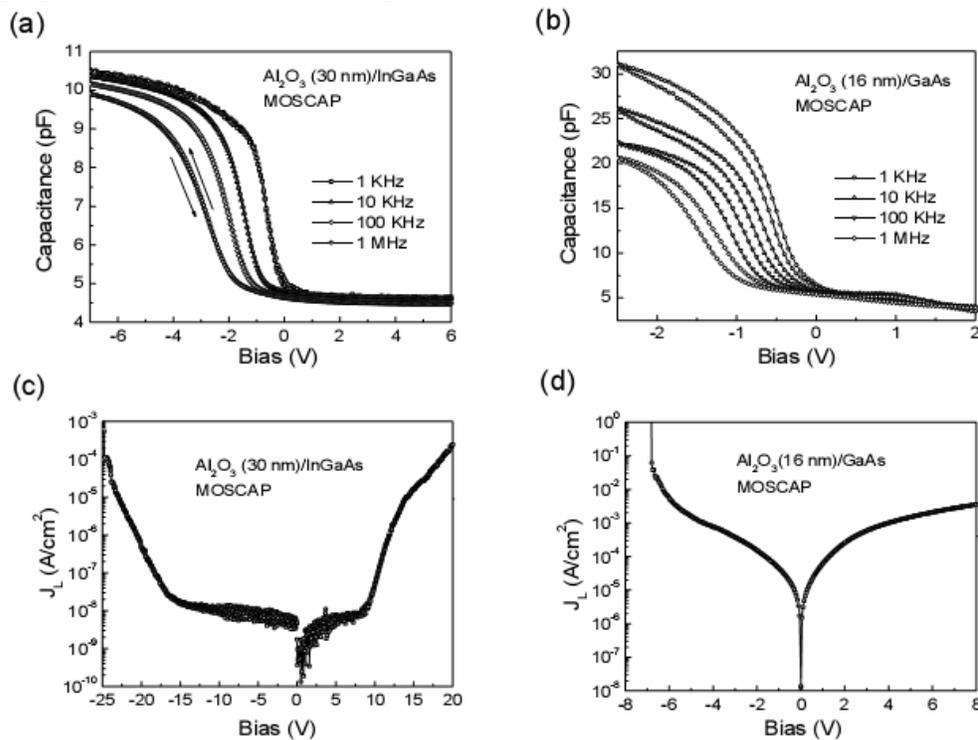


Fig. 2(a) Capacitance-voltage curve for ALD Al_2O_3 (30nm)/InGaAs MOS capacitor subjected to a RTA step of 800°C , 10 s in nitrogen. The hysteresis is negligible. (b) Capacitance-voltage curve for ALD Al_2O_3 (16nm)/GaAs MOS capacitor subjected to the same RTA treatment. Larger hysteresis is observed. (c) Leakage current density J_L (A/cm^2) versus gate bias V_g (V) from a finished Al_2O_3 (30nm)/InGaAs MOS capacitor subjected to a RTA step of 800°C , 10 s in nitrogen. (d) J_L versus V_g from a Al_2O_3 (16nm)/GaAs MOS capacitor subjected to the same RTA process step. The diameter of MOS capacitor is $75\ \mu\text{m}$.

The frequency dispersion on accumulation capacitance C_{max} is another issue for high-k dielectrics on III-V materials. This dispersion could be as large as 50% or more in the frequency range of 1 kHz to 1 MHz, which stymies all efforts to estimate D_{it} using high-low frequency capacitance method. As can be seen in Fig. 2(a), the accumulation capacitance C_{max} was measured on 800°C annealed capacitors in wide frequency range from 1 kHz

up to 1 MHz. The frequency dispersion is only 1% per decade at this frequency range. This experiment unambiguously demonstrates that the major part of frequency dispersion on non-ideal oxide/III-V material interface does relate to the interface properties instead of simple parasite effect, which can be corrected by two-frequency correction or multi circuit element models.[21-22] The dielectric constant is ~ 8.1 deduced from the measured C_{\max} , the area of the capacitor and the film thickness. For annealed 16nm $\text{Al}_2\text{O}_3/\text{GaAs}$, the average frequency dispersion of accumulation capacitance is 8% per decade due to mentioned ashing process and bulk property degradation. The measured accumulation capacitance for 16nm $\text{Al}_2\text{O}_3/\text{GaAs}$ is higher than the expected value. We ascribe it to the fact that the thin amorphous Al_2O_3 film becomes much compact or thinner after 800 °C high temperature annealing.

The flat band shift is also an issue at the beginning of alternative dielectrics research on Si. Here we focus on the observed frequency dependent flat band shift of 800 °C annealed capacitors. The work function of Ti is 4.3 eV, and the band gap of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ is 1.15 eV. The ideal flat band voltage for $\text{Au/Ti/Al}_2\text{O}_3/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and $\text{Au/Ti/Al}_2\text{O}_3/\text{GaAs}$ MOS structure is -0.98 eV and -1.08 eV, respectively. There is almost no flat band voltage shift at 1 KHz frequency. However, the flat band voltages shift toward negative side as frequency increases in Fig. 2(a). The frequency dependent flat band shift is much less on medium temperature (450 °C – 600 °C) annealed capacitors. The phenomenon is less significant on 16 nm thick film compared to 30 nm thick one. It's also roughly scaled with the film thickness and linearly dependent on $\log(f)$. [20] The real origin of this frequency dependent flat band shift is still unknown, and the film thickness dependence of this flat band shift is under systematic investigation.

Split C - V Measurement of $\text{Al}_2\text{O}_3/\text{InGaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET

Split C - V is widely used for mobility calculation [23]. To determine the gate-channel capacitance experimentally, one has to measure the capacitance between the gate and the source/drain region of a MOSFET with grounded substrate. Clear n-channel inversion on p-type InGaAs is observed at $\text{Al}_2\text{O}_3/\text{InGaAs}$ interface on InGaAs MOSFET as shown in Fig.3 (a). The C - V curve is taken on a MOSFET with 40 μm gate length and 100 μm gate width at frequency as low as 1 kHz. At the conventional MOS configuration as measured in Fig. 2(a), no n-channel inversion is observed at frequency as low as 1 KHz. It is understood that the minority carriers (electrons) are supplied by the source and drain regions and not by thermal generation in the depletion region. In split C - V or MOSFET configuration with source and drain grounded at the same time, majority (holes) and minority (electrons) carrier capacitances can be measured independently at the same frequency. Using low-frequency (1 KHz) capacitance $C_{\text{LF}} = 5.5$ pF, high-frequency (1 MHz) capacitance $C_{\text{HF}} = 5.0$ pF and oxide capacitance $C_{\text{ox}} = 11.0$ pF, the middle gap interface trap density D_{it} is determined to be $2.9 \times 10^{11} / \text{cm}^2\text{-eV}$. The actual D_{it} could be higher because 1 KHz frequency is not sufficiently low and slow interface traps could not respond. In the case of $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET in Fig. 3(b), there is no inversion layer formed at interface even at frequency as low as 100 Hz. In addition, there's almost no drain current observed in fabricated

GaAs MOSFET. For InGaAs MOSFET, the drain current of InGaAs is also only 0.12 mA/mm, indicating lower free electron density in the source region. In order to boost the drain current, the implant dose, energy and activation temperature have to be optimized. More work is needed to further improve the interface quality and device process, including activation.

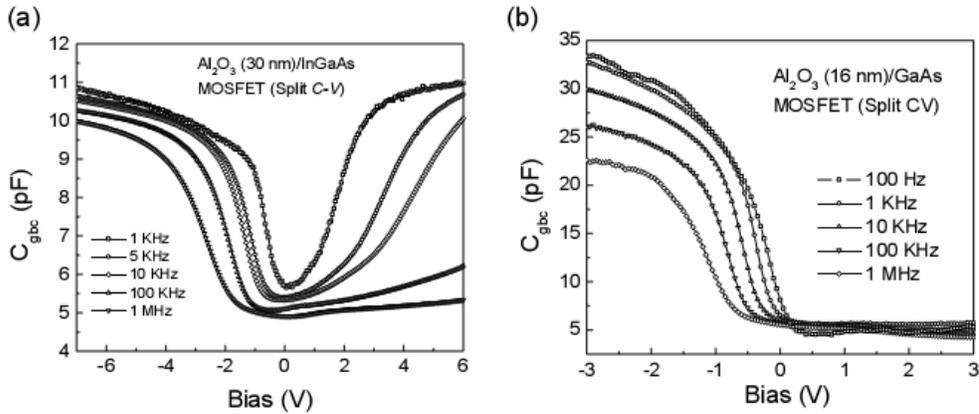


Fig. 3(a) C_{gbc} by split $C-V$ measurement on an $Al_2O_3(30nm)/InGaAs$ MOSFET with a 40 μm gate length and 100 μm gate width at frequency range of 1 KHz - 1 MHz. (b) Similar split $C-V$ measurement on a $Al_2O_3(16nm)/GaAs$ MOSFET with the same dimension at frequency range of 100 Hz-1MHz. No inversion or low-frequency $C-V$ is observed on the GaAs system.

Photo-Assisted $C-V$ Measurement of $Al_2O_3/InGaAs$ and $Al_2O_3/GaAs$ MOS Capacitor at Room-Temperature

The frequency response of a MOS capacitor in the inversion region depends on the inversion-charge generation time. The minority response time for thermal generation/recombination of GaAs is > 400 s, [8] therefore the minority carriers cannot keep up with the low frequency $C-V$ measurement even as low as 1Hz. Actually, both $Al_2O_3/InGaAs$ and $Al_2O_3/GaAs$ MOS capacitors did not show the inversion as low as 100Hz. However, at higher temperature or under photo (light) illumination, more carriers generated and their response time is significantly reduced so that the minority-carrier contribution to the capacitance can be profound. The photo-assisted $C-V$ method is widely used to characterize wide band gap materials such as SiC [24].

Fig. 4 shows photo-assisted $C-V$ measurement for $Al_2O_3/InGaAs$ and $Al_2O_3/GaAs$ MOS capacitors. The inversion $C-V$ for both $Al_2O_3/InGaAs$ and $Al_2O_3/GaAs$ MOS capacitors disappear at 1 KHz under dark measurement. However, the inversion regions of $Al_2O_3/InGaAs$ start to peak upward with increasing light intensity and finally reach full inversion as shown in Fig. 4(a). It implies that directly adsorbed photons with energy larger than the InGaAs band gap excite electron-hole pairs. These excess carriers move toward or away from the $Al_2O_3/InGaAs$ interface depending on the polarity of dc gate bias. In other words, the carriers respond to high frequency ac bias. The higher light density creates more electron-hole pairs and reaches full inversion formation. However, in the case of $Al_2O_3/GaAs$ in Fig. 4(b), the inversion

layer is difficult to form even when illuminated by the same intensity ($0 \sim 0.45 \text{ W/cm}^2$) of light used previously. The difference in surface recombination velocity of $\text{Al}_2\text{O}_3/\text{InGaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ can explain the above phenomena.

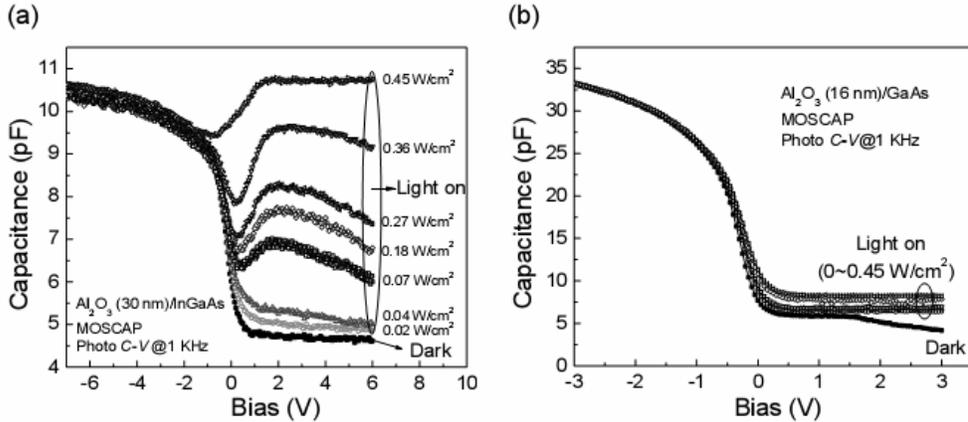


Fig. 4(a) Photo-assisted $C-V$ measurements for both $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ and $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ MOS capacitors. The $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ MOS $C-V$ shows strong inversion with light on. The corresponding light intensity from the microscope (from top to bottom) is measured to be 0.45, 0.36, 0.27, 0.18, 0.07, 0.04, 0.02 W/cm^2 , respectively. (b) No inversion or low-frequency CV is observed for the $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ MOS CV with light on.

High-Temperature $C-V$ Measurement of $\text{Al}_2\text{O}_3/\text{InGaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS Capacitor

Temperature dependent $C-V$ measurements with a wide range of small ac signal frequencies are widely used to study the minority-carrier recombination kinetics. The $C-V$ measurements at 100Hz – 1 MHz and at elevated temperature from 300 K – 500 K are systematically studied. Fig. 5(a) and Fig. 5(b) show the results measured at 10 kHz for $\text{Al}_2\text{O}_3/\text{InGaAs}$ and 1 KHz for $\text{Al}_2\text{O}_3/\text{GaAs}$ as a function of bias with temperature as parameter. The major effect of temperature occurs during depletion-inversion at positive biases. At room temperature (300 K), minority-carriers do not follow the 10 kHz signal for InGaAs and 1 KHz for GaAs; thus a high frequency curve is measured as shown in Fig. 2(a) and Fig. 2(b). However, as temperature is increased from 300 K to 500 K, minority carriers begin to follow because generation and recombination rates increase with temperature and the transition is made from a high frequency curve to a low frequency curve as shown in Fig. 5(a) and Fig. 5(b). To define a transition frequency, we regard any $C-V$ curve exhibiting a minimum capacitance, such as the curve in Fig. 5(b) measured at 400 K, as a low frequency curve even though capacitance in strong inversion does not increase to C_{ox} . The definition is merely a matter of convenience and is arbitrary with 5-10 % error bars. Those $C-V$ curves without a distinct minimum, such as the curve measured at 350 K are considered to be of the high frequency type. The degree of recombination is limited or reduced when the bias is swept toward strong inversion or deep depletion, i.e., the 400 K $C-V$ curve in Fig. 5(a).

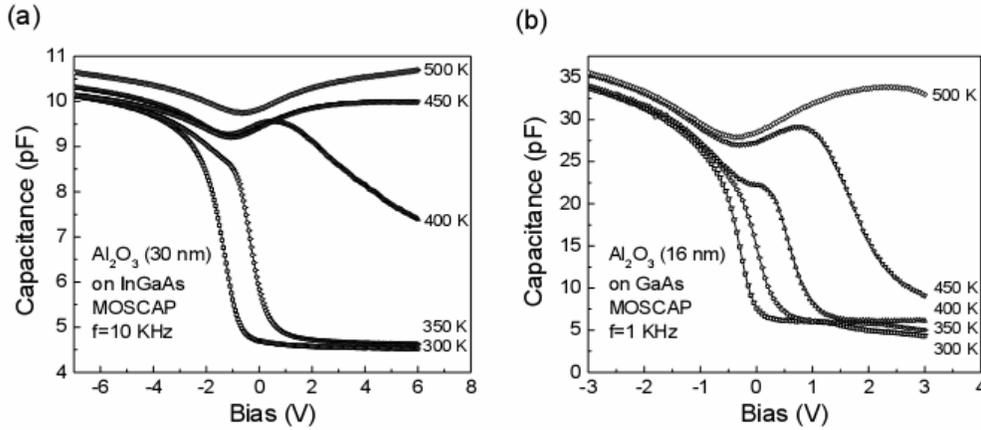


Fig. 5(a) Temperature dependent $C-V$ for both $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ and $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ MOS capacitors. For $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ MOS, the inversion is observed at 385K and 10KHz. (b) Temperature dependent CV for $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ capacitors. The inversion is observed at 400K and 950Hz.

By systematically varying both temperatures and frequencies, the temperature dependence of the transition frequency can be determined. In order to have more insights on minority-carrier response kinetics, we calculate the activation energy (E_A) of minority-carrier generation and recombination for $\text{Al}_2\text{O}_3/\text{InGaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS structures. The E_A is determined by the slope of the transition frequency versus $1000/T$ plot as shown in Fig. 6. The transition frequency has an activation energy of 0.62 ± 0.03 eV and 0.71 ± 0.01 eV, respectively, which is just about half the bandgap energy of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs. This activation energy is that of intrinsic electrons in $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs. Therefore, the dominant mechanism for controlling minority carrier response must be generation and recombination through bulk traps in the measured MOS structures over the temperature range 300 – 500 K. Motivated by the above $C-V$ studies on minority carrier response, we measure the drain current versus drain voltage at a fixed gate bias as a function of temperatures. The elevated temperature generates more minority carriers (electrons) into the inversion channel in the E-mode $\text{Al}_2\text{O}_3/\text{InGaAs}$ MOSFET and boosts the drain current by a factor of ~ 10 . [25]

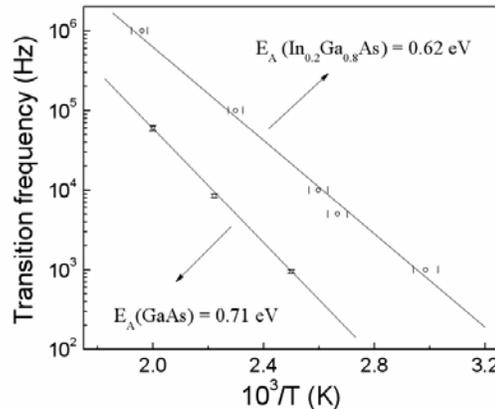


Fig. 6 (a) Temperature dependence of the transition frequency between high and low frequency $C-V$ curves. Activation energies of the minority-carrier recombination for $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ and $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ are obtained from the slope of the linear fitting trace.

Summary

In summary, we have systematically studied C - V characteristics of ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ and $\text{Al}_2\text{O}_3/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ MOS and source-drain implanted MOSFET structure. $\text{Al}_2\text{O}_3(30\text{nm})/\text{InGaAs}$ shows extremely low leakage current, small CV hysteresis, less than 1% per decade frequency dispersion at accumulation capacitance and strong electron inversion layer appeared at split CV measurement. However, $\text{Al}_2\text{O}_3(16\text{nm})/\text{GaAs}$ shows larger hysteresis and frequency dispersion with no inversion layer formed by split C - V measurement. Photo-assisted C - V measurement shows the inversion layer can easily be formed on InGaAs interface but not on GaAs interface, indicating surface recombination rate is much higher in GaAs system. Minority-carrier response of $\text{Al}_2\text{O}_3/\text{InGaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS structures is systematically studied by high-temperature C - V measurements. The minority-carrier activation energies of the $\text{Al}_2\text{O}_3/\text{InGaAs}/\text{GaAs}$ and $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS are 0.62 eV and 0.71 eV, respectively.

Acknowledgments

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