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Cite as: Appl. Phys. Lett. **119**, 263503 (2021); https://doi.org/10.1063/5.0075166
Submitted: 13 October 2021 • Accepted: 09 December 2021 • Published Online: 27 December 2021

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ABSTRACT

Recent advances have enabled the demonstration of record high-performance atomically thin n-type indium oxide (In_2O_3) field-effect transistors with low thermal budget suitable for back-end-of-line logic or memory applications. By using ultra-thin layers of In_2O_3, its degenerate carrier density is suppressed so that it can be modulated by conventional dielectric gating. These devices have high on-currents due to its high mobility and low contact resistance; meanwhile they can have exceptionally low off-currents due to its wide bandgap. For both low-power logic and memory, the off-state performance should be understood in more detail, although they are constrained by the limits of traditional measurement techniques. In this Letter, we systematically probe the off-current of ultra-thin In_2O_3 transistors by adopting a wide channel geometry with temperature-dependent electrical measurements and demonstrate the potential for record high current on/off ratios of 10^{17} on In_2O_3 transistors.

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Recent work on indium oxide (In_2O_3) has shown it to be an excellent oxide semiconductor in the ultra-thin (e.g., <3 nm) limit. In terms of its electrical performance, field-effect transistor (FET) measurements have shown subthreshold swing (SS) down to ~63 mV/dec,[1] mobility as high as 113 cm^2/V s,[2] and on-currents well over 2 A/mm in both the depletion-mode and enhancement-mode with engineerable threshold voltage by plasma treatment[3] or annealing.[1] Some of these qualities are demonstrated in Figs. 1(a) and 1(b), which show the transfer and output characteristics of a previously fabricated high-performance device after O_2 plasma treatment.[3] The devices also show stability in a hydrogen-rich environment[1] and good long-term bias stress stability,[4] which are issues for related materials such as indium-gallium-zinc oxide (IGZO).[5] The combination of these outstanding electrical properties with low-temperature growth and fabrication suggests that this atomic layer deposition (ALD) grown atomically thin oxide semiconductor has potential applications in back-end-of-line (BEOL) logic or memory devices. Some specific example application cases are discussed in detail in Ref. 6. Detailed thickness-dependent electrical characterization can be found in Refs. 7 and 8. To date, the off-state current of these ultra-thin In_2O_3 devices has not been directly addressed due to the measurable minimum current limit of typical equipment. A Keysight B1500A with current noise floor of around 10 fA is used in this work. Indium oxide has a wide bandgap of roughly 2.9 eV in bulk[9] that is calculated to increase in the ultra-thin limit;[8] hence, it should have very low off-current beyond the limitations of typical measurement setups. In this work, we systematically set a new ceiling on ultra-thin In_2O_3's room-temperature I_{off} of around 6×10^{-20} A/μm (with room temperature for further reductions) and I_{on}/I_{off} of around 10^{17} using a serpentine gate wide-channel device geometry and temperature-dependent measurements. The need for this new design and work are highlighted in Figs. 1(c) and 1(d), where the current floor for the measurement limit is around 10^{-15} A/μm. Using a wide-channel geometry simultaneously raises the absolute current level and the denominator, in principle, enabling higher sensitivity in A/μm.

Figure 2(a) shows a cross-sectional illustration of the device structure used. To achieve a large effective channel width (W_{eff}), a serpentine gate geometry is used with interdigitated source and drain fingers. A top-down overview of a fabricated device is shown in the optical microscope image in Fig. 2(b), where the buried gate, source, and drain have been labeled for clarity. Using this design, devices with channel widths greater than 30 000 μm were fabricated. W_{eff} is taken as the sum of the spans of each straight section with corner sections counted as the length of a quarter-circle arc in the middle of the channel. The fabrication process flow is largely identical to those in previous works.[1,3,4] After the substrate (in this case 90 nm SiO_2 on Si) is

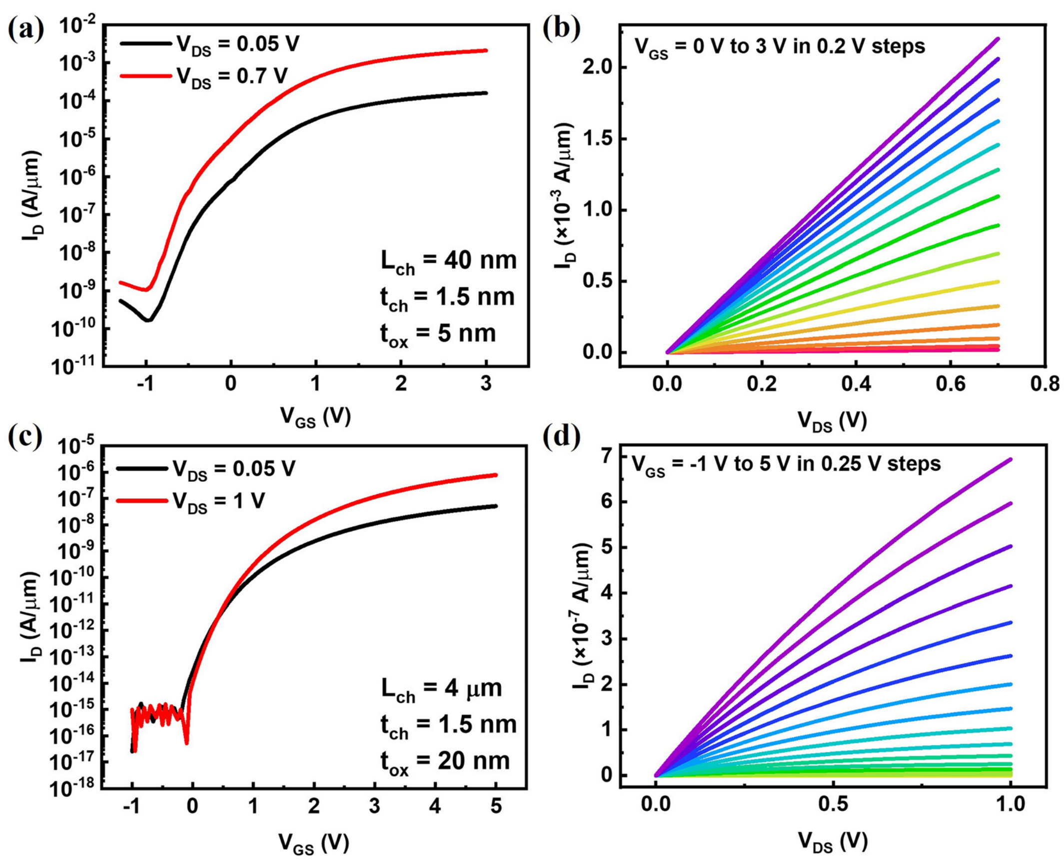

FIG. 1. Ultra-thin In_2O_3 device electrical performance with traditional TFT geometry. (a) Transfer characteristics of a high-performance scaled device and (b) associated output curves. (c) and (d) The transfer and output characteristics, respectively, of a long-channel device with relatively thick (20 nm) gate dielectric, demonstrating the noise floor limit of I_{off} measurement with traditional geometry. The channel width is approximately 10 μm in both cases.

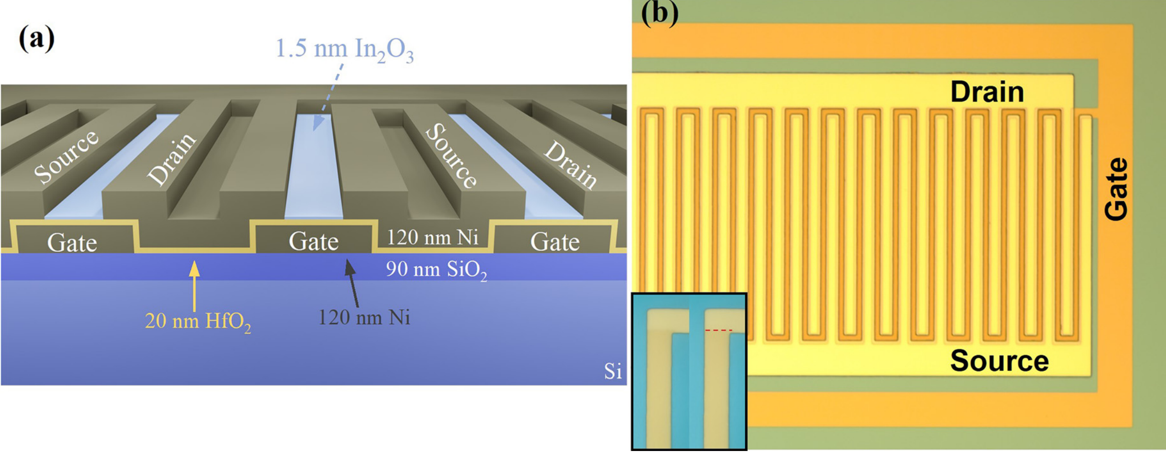

FIG. 2. (a) Cross-sectional illustration of the device structure with each layer labeled. (b) Optical microscope image of a finished device with the gate, source, and drain pads labeled. The inset shows the In_2O_3 layer atop the buried gate after isolation, but before the source and drain are fabricated. Inset, left is the raw image, while the inset, right has a dashed line added to highlight the In_2O_3 boundary.

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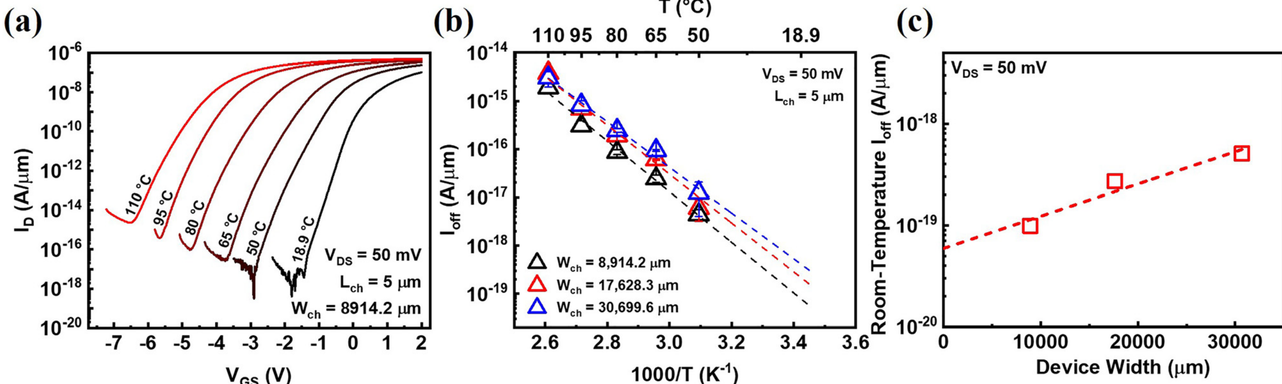

FIG. 3. (a) Example transfer curves showing the trajectory of one device with respect to increasing temperature. It is difficult to directly interpret I_{off} for the lower-temperature measurements because of the noise floor of the measurement unit. (b) Arrhenius plot used to estimate the room-temperature off current of the In_2O_3 devices showing several devices with varying channel widths. Error bars represent one standard deviation from the average value. I_{off} is taken to be the minimum of each measured transfer curve. (c) Further extrapolating out the channel width dependence gives a final estimate of the room-temperature I_{off} of these devices around 6×10^{-20} A/μm.

solvent cleaned with toluene, acetone, and isopropanol, a bilayer photoresist stack (AZ1518 on top of SF9 PMGI-based resist) is applied to yield clean liftoff of the buried gate layer. The buried gates are then defined by photolithography, e-beam evaporation of nickel, and liftoff. ALD is used to grow the gate dielectric (20 nm HfO_2 at 200 °C) and active channel (1.5 nm In_2O_3 at 225 °C) materials. $[(CH_3)_2N]_4Hf$ (TDMAHf) and $(CH_3)_3In$ (TMIn) are used as the hafnium and indium metalorganic precursors, respectively, with H_2O as the oxygen precursor in both cases. The serpentine channel regions are isolated by photolithography and wet etching in concentrated HCl. A subsequent final photolithography step is used to define the interdigitated source and drain contacts. The buried gate, source, and drain all use 120 nm layers of e-beam evaporated nickel. Detailed material characterization work on this fabrication process, including capacitance–voltage (C–V) measurements, transmission electron microscopy (TEM), and atomic force microscopy (AFM), can be found in Refs. 1–3 and 8.

The impact of gate leakage on the measurements appears to be minimal, lying below the noise floor of the gate current measurement except at high temperatures and biases. A 10 minute O_2 plasma treatment is used to shift the threshold voltage positively toward zero and further reduce the impact of gate leakage on the measurements.[3] The precise contributions of different leakage mechanisms to the off-current are difficult to disentangle and warrant further study, in particular, the role of In_2O_3's defects. Various wide bandgap transition metal dichalcogenides show I_{off} ranging from 10^{-15} to 10^{-17} A/μm.[10,11] In addition to obvious benefits for logic devices when combined with low SS, small I_{off} is extremely useful in a BEOL-compatible selector for in-memory computing and monolithic 3D integration.[6]

Figure 3(a) shows the evolution of the transfer characteristics of a selected device as a function of temperature. The threshold voltage decreases significantly with increasing temperature. The average rate of shift, $\partial V_T/\partial T$, is approximately −53.9 mV/K. This value is slightly lower than the one reported for similar devices made with closely related IGZO,[12] where the temperature-dependent shift has been attributed to the temporary creation of double-donor oxygen vacancies (wherein O atoms move from coordinated sites to interstitial sites and then return upon cooling)[13] or to thermal activation of existing traps.[14]

In_2O_3 is known to be rich in oxygen vacancies, which drives its large unintentional n-type doping like in IGZO. Since the devices in this work are essentially all surface/interface without any bulk region and we do not observe an increase in D_{it} with temperature (Fig. 4), the V_T shift behavior can be ascribed to electrons activated from oxygen vacancies at elevated temperatures. The temperature-dependent measurements are repeatable, ruling out other permanent mechanisms as the cause of the V_T shifts. This effect may need to be addressed in more detail to enable reliable device operation over a wider range of temperatures. Figure 3(b) shows an Arrhenius plot of I_{off} as a function of temperature for three channel widths. Error bars represent one standard deviation from an average value. The devices were measured in an enclosed probe station with an integrated temperature controller sensitive to ±0.1 °C. Measurements were collected from ambient

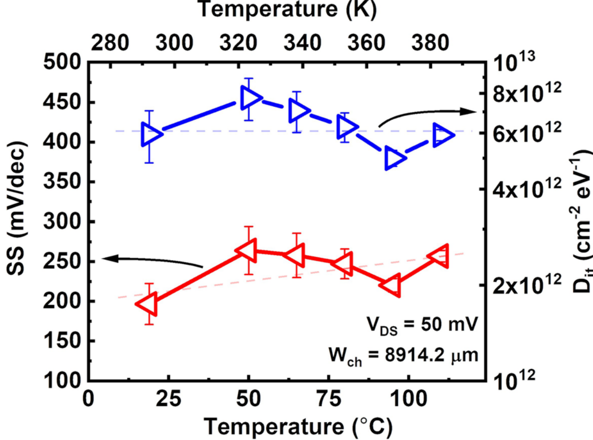

FIG. 4. Measured subthreshold swing (red left-pointing triangles) and extracted D_{it} at the In_2O_3/HfO_2 interface (blue right-pointing triangles) as a function of the ambient temperature. D_{it} is extracted using SS $= \ln(10)\cdot k_BT/q\cdot(1 + C_{it}/C_{ox})$. Depletion capacitance is assumed to be negligible due to the ultra-thin In_2O_3 channel. D_{it} is approximately flat with increasing temperature, showing good thermal stability of the devices.

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temperature (18.9 °C) to 110 °C. The small width dependence observed is likely related to Ohmic losses across the long gate contacts; hence, extrapolation from the narrower devices should give a more accurate room-temperature I_{off} value. An activation energy can be extracted from the slope of the curves taking $I_{off} \propto \exp(-E_a/k_BT)$. From this, E_a between 0.95 and 1.10 eV is found, which is about one third of the bandgap. This might be related to a defect energy level deep inside the bandgap, near the mid-gap of In_2O_3, again similar to IGZO.[15] Extrapolating out the width dependence, shown in Fig. 3(c), gives a final estimated off current of roughly 6×10^{-20} A/μm at our lab's ambient temperature of 18.9 °C. In principle, this value may be further reduced with a reduction of defects in the material.

Figure 4 shows the measured SS and extracted interface trap density (D_{it}) for a set of devices as a function of temperature. D_{it} can be estimated from the measured SS from $SS = \ln(10)\cdot k_BT/q\cdot(1 + C_{it}/C_{ox})$, where k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, C_{it} is the interface trap capacitance, and C_{ox} is the gate dielectric capacitance. Our gate dielectric has previously been characterized in detail.[3] Depletion capacitance is assumed to be negligible due to the ultra-thin nature of the In_2O_3 channel. The SS trends slightly upward with increasing temperature, while D_{it} remains essentially constant, demonstrating the good thermal stability of the devices. In optimized devices with scaled oxides, both values can be significantly lower.[1,3]

With an estimated room-temperature I_{off} of around 6×10^{-20} A/μm and I_{on} exceeding 2×10^{-3} A/μm,[1–3] atomically thin In_2O_3 field-effect transistors can potentially realize a high current on/off ratio of at least 10^{17}. In practice, achieving this requires careful consideration and optimization of the gate dielectric material, dielectric thickness, and channel length to simultaneously minimize gate leakage, eliminate short channel effects, and maximize on current. This work reveals the attainable level of the off current and I_{on}/I_{off} ratio for ultra-thin In_2O_3 devices that can be used by device engineers on an application-specific basis. For low-power logic or memory applications requiring ultra-low current leakage in the back-end-of-line, this is highly desirable.

The authors would like to thank Suman Datta and Eric Pop for valuable discussions. This work was supported by the SRC/DARPA JUMP ASCENT Center and the SRC nCORE IMPACT Center.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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