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Ionic liquid gating on atomic layer deposition passivated GaN: Ultra-high electron density induced high drain current and low contact resistance

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Herein, we report on achieving ultra-high electron density (exceeding $10^{14}\,cm^{-2}$) in a GaN bulk material device by ionic liquid gating, through the application of atomic layer deposition (ALD) of Al_2O_3 to passivate the GaN surface. Output characteristics demonstrate a maximum drain current of 1.47 A/mm, the highest reported among all bulk GaN field-effect transistors, with an on/off ratio of 10^5 at room temperature. An ultra-high electron density exceeding $10^{14}\,cm^{-2}$ accumulated at the surface is confirmed via Hall-effect measurement and transfer length measurement. In addition to the ultra-high electron density, we also observe a reduction of the contact resistance due to the narrowing of the Schottky barrier width on the contacts. Taking advantage of the ALD surface passivation and ionic liquid gating technique, this work provides a route to study the field-effect and carrier transport properties of conventional semiconductors in unprecedented ultra-high charge density regions. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4950816]

The quest for ultra-high carrier density systems has always been a hot topic in the electronic device and condensed matter physics areas, due to the fact that high carrier density can lead to high current density in semiconductor devices and can even induce exotic phase transitions such as superconductivity state at low temperatures.[1–6] Except for dopant diffusion and ion implantation,[7] the field-effect is widely used to modulate channel carrier density in electronic devices.[8] However, field-effect modulation through a solid state dielectric is severely limited by its low dielectric breakdown strength (usually several MV/cm), which limits 2D carrier density to approximately $10^{13}\,cm^{-2}$. The ionic liquid (IL) gating method can exceed this limit and induce an ultra-high carrier density of $10^{14}\,cm^{-2}$ in various materials, such as black phosphorus, graphene, oxide semiconductor ZnO, and InN.[9–12] The ultra-high electron density is a result of the formation of strong dipoles at the IL and the material interface as shown in Fig. 1(a). In general, the dipole layer is only several Å thick, resulting in the normalized gate capacitance being ten times higher than state-of-the-art high-k dielectric gate capacitance with nanometer equivalent oxide thickness. Such ultra-high carrier density of $10^{14}\,cm^{-2}$ is hard to realize in the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), and thus, IL induced ultra-high carrier density can be potentially used for future high carrier density devices.

Many studies have already demonstrated semiconductor to metal or superconductor transitions through IL gating techniques.[1–6,9] The materials which are studied are either 2D materials, such as MoS_2, WS_2, and black phosphorus, which have no dangling bonds as traps at the surface to capture mobile charges, or they are oxides themselves, such as ZnO and $KTaO_3$. Currently, only heavily doped narrow bandgap InN can realize an ultra-high density on the surface by the electrolyte gating method, partly due to the Fermi-level is aligned deeply inside the conduction band in InN.[12] For conventional semiconductors with Fermi-level aligned inside the bandgaps, only weak modulation of resistance, such as unpassivated GaAs and Si, was reported by IL gating. The obtained electron density is far lower than those in the 2D materials and oxides.[13,14]

In order to realize ultra-high carrier density accumulation on the surfaces of conventional semiconductors, it is crucial to effectively passivate the high density surface defects, i.e., dangling bonds, surface states, and traps. Atomic layer deposition (ALD) is widely used for surface cleaning and

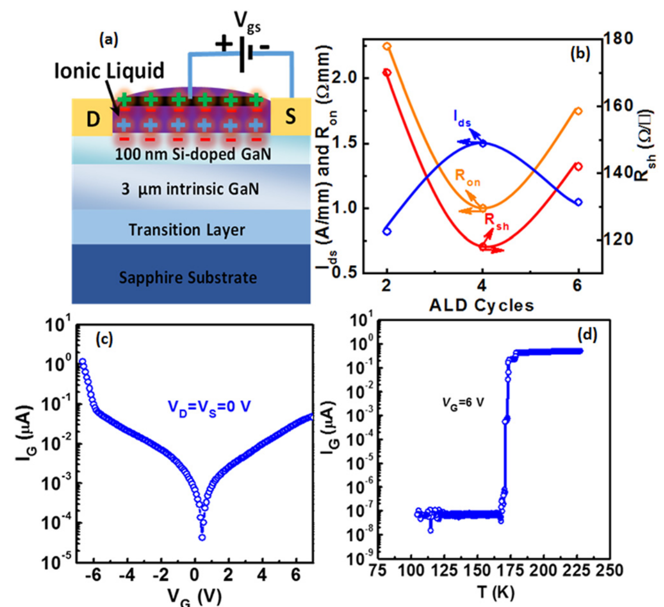

FIG. 1. (a) Schematic view of IL EDLT GaN FET's charge distribution under the positive gate bias condition. (b) ALD cycle dependent I_{ds}, R_{on}, and R_{sh}, which is used to find the optimal passivation conditions. (c) Room temperature gate leakage current of the IL EDLT GaN FET. (d) Temperature dependent gate leakage current at a $V_g = 6$ V IL EDLT Hall bar.

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passivation on III–V compound semiconductors.[15,16] Although the huge excess of ions in the IL can also passivate the dangling bonds and surface defects, those captured electrons serve as an electric field screen layer to prevent the further accumulation of electrons in the channel. On the contrary, if those dangling bonds and surface defects are first passivated by ALD, the IL can induce much more mobile electrons in the channel which conduct the current. After a systematic study of ALD passivation of GaN surface, we have identified that an application of 4 cycles of tri-methyl-aluminum (TMA) and H_2O with pulse times of 1.0 s and 1.2 s is optimal as shown in Fig. 1(c) through electrical characterization. The purpose of longer pulse time compared with normal ALD pulse time is to make the substrate more uniformly exposed to the TMA within several ALD cycles. The number of ALD cycles must be optimized and cannot be too many; otherwise, the deposited Al_2O_3 would limit the whole gate capacitance. Four cycles of ALD passivation correspond to a thickness of 3.6 Å Al_2O_3, which is less than one mono-layer of Al_2O_3. The ALD cycles here are used to passivate the surface defects of GaN rather than a real deposition of ALD Al_2O_3 on GaN. As shown in Fig. 1(b), 2 cycles of ALD are not enough for sufficient surface passivation and 6 cycles of ALD begin to deposit monolayer oxide. After ALD passivation, we fabricated electric-double-layer-transistors (EDLTs) on a slightly Si-doped GaN channel, realizing an accumulation of electron density exceeding $10^{14}\,cm^{-2}$ on a conventional semiconductor GaN surface.

Fig. 1(a) shows a schematic view of the nano-capacitor EDLT GaN device. The GaN substrate has 100 nm of epitaxial Si-doped GaN layer on top, with a carrier concentration of $5\times10^{17}\,cm^{-3}$ followed by a 3 μm intrinsic GaN layer grown on a sapphire substrate. Device fabrication started with mesa isolation by Cl_2/BCl_3 dry etching to a depth of 150 nm. Then, the ohmic contacts were formed by depositing Ti/Al/Au (15/60/50 nm) followed by a 775 °C rapid thermal annealing (RTA) process in nitrogen atmosphere for 30 s. The gate pad was formed by depositing Ni/Au (30/50 nm) on the intrinsic GaN layer of the etched area, which was isolated from the channel. Without IL application, the contact resistance (R_c) and sheet resistance (R_{sh}) are 2.9 Ω mm and 5.4 kΩ/□, respectively. After the device fabrication, the sample was transferred to an ASM F120 ALD system for Al_2O_3 passivation with several cycles of tri-methyl-aluminum (TMA) and H_2O at 300 °C. Both standard FET and Hall-bar structures were fabricated. The FET devices have a gate width of 10 μm and length (L_g) of 0.3, 0.6, 1, 2, 4, 6, 10, 20, and 40 μm. Only the channel areas are conducting; device isolation is realized through dry etching away the 100 nm thick conducting n-GaN layer outside of the channel areas. After baking the IL at 90 °C for 1 h under vacuum to remove moisture, a droplet of IL was applied to the sample, which covered the gate electrode and the channel area. The room temperature I–V measurement is carried out within 5–10 min of each device to avoid oxidation of the ions in the IL. All the room temperature I–V measurements were carried out under air atmosphere. The IL we used is N, N-Diethyl-N-methyl-N-(2-methoxyethl)ammonium-bis(trifluoromethanesulfonyl)imide. The gate leakage current of the FET device is on the order of the 10^{-6} A, as shown in Fig. 1(c). The gate leakage not normalized with the gate pad area is due to uncertainty of the real coverage of IL on the gate pad. When the IL is frozen at low temperatures, the gate leakage current becomes negligible.

Figs. 2(a)–2(c) show the room temperature output characteristics (I_{ds}-V_{ds}) and transfer characteristics (I_{ds}-V_{gs}) of

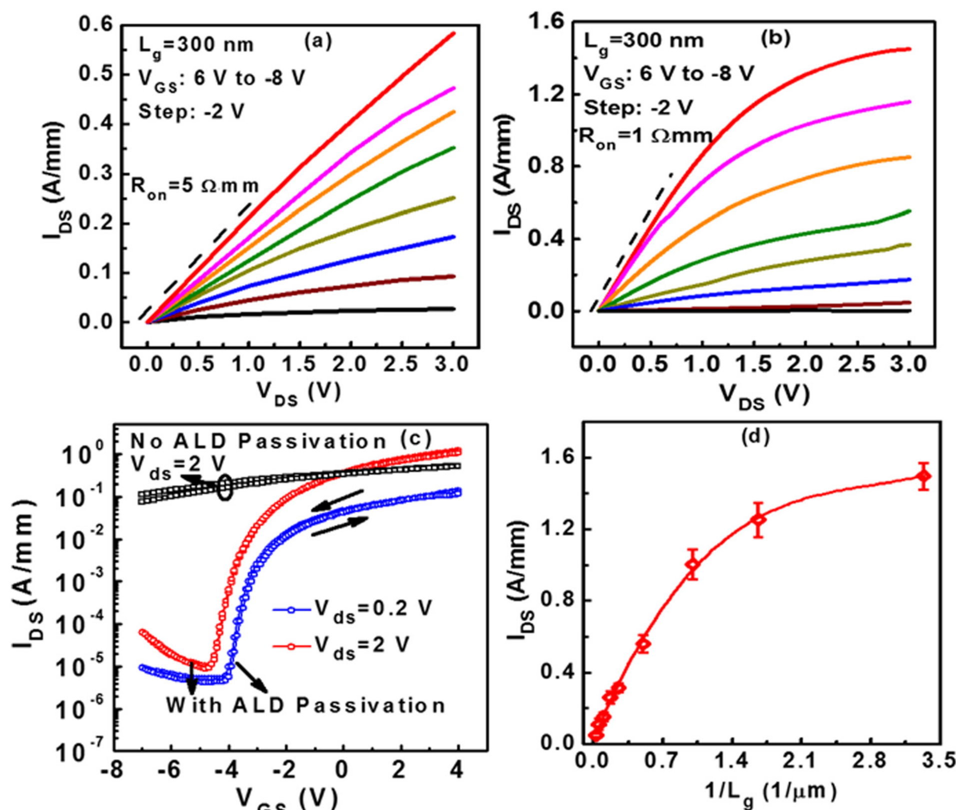

FIG. 2. I_{ds}–V_{ds} output characteristics of EDLT-GaN devices (a) without and (b) with 4 cycles of ALD passivation. (c) I_{ds}–V_{gs} transfer characteristics of the EDLT-GaN device with and without ALD passivation. (d) Scaling metrics of different L_g of the EDLT-GaN device with ALD passivation.

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TABLE I. Performance benchmark of IL on GaN with other published GaN MOSFETs on bulk GaN channel.

	This work	Ref. 17	Ref. 18	Ref. 19	Ref. 26
L_g (μm)	0.3	5	1	1	1
I_{dmax} (A/mm)	1.45	0.25	0.2	0.75	0.35
G_{max} (S/mm)	0.25	0.15	0.02	0.15	N.A.

the EDLT GaN devices without and with 4 cycles of ALD passivation. Compared to most 2D materials, GaN has a wider bandgap of 3.45 eV and higher breakdown electric field of 3 MV/cm. Thus, a higher V_g is applicable to the device. The V_g bias range is within the applicable window of this IL.[1,11] The V_g sweep mode is "quiet mode" with each bias holds for 0.2 s. Without ALD passivation, the EDLT GaN device with L_g of 300 nm shows a fair electron accumulation at the surface, with a maximum drain to source current ($I_{ds,max}$) of 570 mA/mm and an on-resistance (R_{on}) of 5 Ω mm. The device cannot be fully depleted due to the poor interface between the IL and GaN. Without effective passivation, surface defects act as traps preventing the complete depletion of the GaN channel underneath the IL. In contrast, with 4-cycle ALD passivation, the same gate length device exhibits an $I_{ds,max}$ of 1.47 A/mm at $V_g = 6$ V and $V_{ds} = 3$ V, which is the highest reported among all GaN FETs based on GaN bulk channels, as shown in Table I.[17–19,26] In addition to the highest $I_{ds,max}$, this device shows a low R_{on} of 1 Ω mm. We ascribe this high I_{ds} and low R_{on} to the ultra-high electron density induced at the IL-GaN interface. As shown in Fig. 2(c), a clear on/off ratio of 10^5 at $V_{ds} = 2$ V is observed at room temperature of the device with ALD passivation, even with a total channel thickness of 100 nm. There is only a slight hysteresis in I–V curves of the ALD passivated device; on the contrary, the device without ALD passivation shows a large hysteresis indicating high density of the surface traps. By differentiating the I_{ds} versus V_{gs} curve, we obtain a peak transconductance of 245 mS/mm at $V_{gs} = 2$ V. For more than forty devices with optimal ALD passivation and various L_g, we measured I_{ds}–V_{ds} and I_{ds}–V_{gs} curves. All of them show a good electrostatic control by IL gating. Scaling metrics of I_{ds} versus $1/L_g$ are plotted in Fig. 2(d). The error-bar is obtained from the standard deviation of four devices. The scaling behavior fits well for long channel devices (1 to 40 μm), inversely proportional to L_g. I_{ds} begins to slowly saturate as L_g is reduced below 600 nm. This scaling

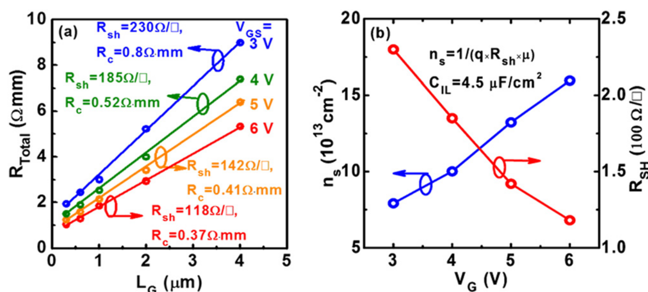

FIG. 3. (a) TLM method extracted contact resistance (R_c) and sheet resistance (R_{sh}) at different V_{gs} conditions and different L_g. (b) V_{gs} dependent 2D electron density (n_s) and R_{sh}.

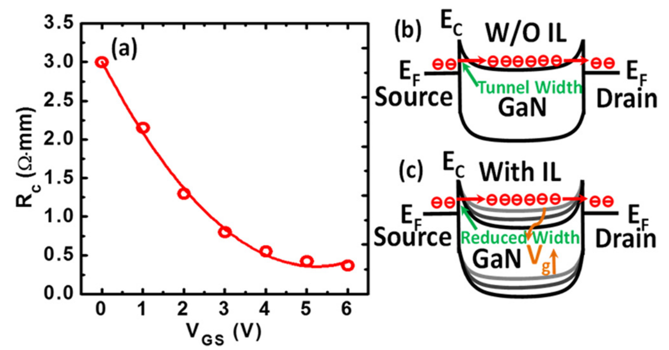

FIG. 4. (a) V_{gs} dependent R_c estimated from TLM structure. Band diagram for metal-GaN-metal structure when there is (b) no IL present and (c) positively biased IL on top. GaN channel conduction band is pulled down for positive V_g. More electrons can tunnel through Schottky barriers with a reduced barrier width.

behavior is similar to that of conventional Si or III–V MOSFETs.[20]

The R_{sh} and R_c for different V_{gs} can also be determined from transfer length measurement (TLM). By linearly fitting each total resistance, which is extracted from the linear part of I_{ds}-V_{ds}, the intercept at $L_g = 0$ gives twice R_c and the slope of the curve gives R_{sh}.[21] As shown in Fig. 3(a) for different V_{gs}, R_{sh} is reduced by 50 times to 118 Ω/□ compared to 5.4 kΩ/□ without IL gating. The 2D electron density (n_s) can be calculated by $\boldsymbol{n_s} = \frac{1}{R_{sh} \times q \times \mu}$, where q and μ are charge quantity of electron and room temperature mobility, respectively. The electron mobility and density are determined as the following sequences: (1) At $V_g = 3$ V and $V_g = 4$ V, room temperature Hall measurement was applied to determine the electron density and Hall mobility. The sheet resistance determined from Hall measurement is consistent with the value from TLM measurement. (2) At $V_g = 5$ V and $V_g = 6$ V, the Hall mobility (250 $cm^2 \cdot V^{-1} \cdot s^{-1}$) at $V_g = 4$ V is used as the field-effect mobility to roughly extract the electron density from the TLM measurement. The reason why we could not perform Hall measurement at $V_g = 5$ and 6 V is that at such high V_g, the gate leakage current (∼μA) becomes comparable to the Hall measurement injection current, making the Hall measurement inaccurate. The approach is an acceptable estimation, because the electron mobility becomes saturated under ultra-high electron density conditions.[22] (3) At low-temperature range, when IL is frozen with very low gate leakage current, we performed the Hall measurement to determine the electron density and Hall mobility at $V_g = 6$ V as usual. The n_s is found to be almost linearly proportional to V_{gs} as shown in Fig. 3(b). An ultra-high electron density of 1.6×10^{14} cm^{-2} is achieved on the GaN surface. Furthermore, the capacitance of the EDLT induced nano-capacitor can be derived from $\boldsymbol{C_{IL}} = \frac{d(n_s \times q)}{dV_{GS}}$. It is estimated to be 4.5 μF/cm^2. This value is much higher than those seen in the conventional MOSFETs with solid state gate dielectrics. R_{sh}, I_{ds}, and R_c were also used to optimize the ALD passivation as described before in Fig. 1(c).

An interesting observation is that R_c is reduced by positive V_g as can be seen in Fig. 4(a). Without the IL on top or at zero bias, R_c is ∼2.9 Ω mm. It is reduced by nearly an order of magnitude to 0.3 Ω mm when $V_g = 6$ V. The mechanism behind this reduction is proposed here. Figs. 4(b) and

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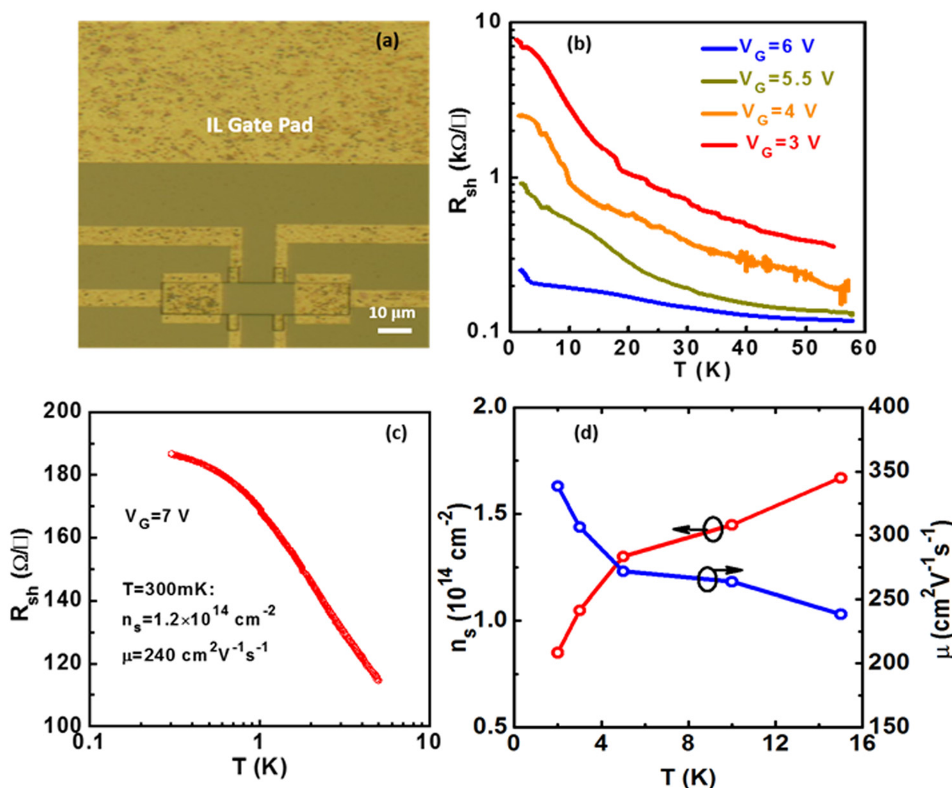

FIG. 5. (a) GaN Hall bar geometry device. (b) Semilog plot of R_{sh} versus T at different V_g conditions. (c) R_{sh} versus T for $V_g = 7$ V from T = 5 K to 300 mK. $n_s = 1.2 \times 10^{14}$ cm^{-2} at T = 300 mK. (d) n_s and μ versus T for $V_g = 6$ V.

4(c) show a schematic view of band diagrams under low V_{ds} conditions for source–semiconductor–drain junctions without and with IL gating, respectively. When a positive V_g is applied to the IL, more electrons populate in the channel, pulling down the conduction band and increasing the channel doping. Therefore, the Schottky barrier width at the contacts narrows. This significantly enhances electron tunneling current at the contacts and thus reduces R_c.[23] Similar phenomenon of R_c reduction is also observed by the chloride doping and IL gating on MoS_2.[24,25] To make a good ohmic contact on GaN is a challenge, due to its wide bandgap and Fermi level pinning near the mid-gap. n++ GaN contact region regrowth or heavily Si-doped GaN is usually implemented.[26,27] This work provides an alternative way to modulate R_c using IL gating.

IL gating research is typically motivated by a desire to realize ultra-high carrier densities or to study phase transition phenomena at low temperatures. We also fabricated Hall bar geometry devices and characterized them at cryogenic temperatures. The Hall bar and gate pad configuration are shown in Fig. 5(a). The IL gated GaN Hall bar devices are cooled by first applying a V_g of 3.0, 4.0, 5.5, and 6.0 V at 240 K and then maintaining constant V_g until sub-150 K to ensure the IL is totally frozen. The glass transition temperature of this IL is 175 K as shown in Fig. 1(d). The normalized longitudinal resistance (R_{xx}) is monitored until 1.6 K. Fig. 5(b) shows the R_{sh} as a function of temperature (T) for different V_g conditions. Unfortunately, we did not observe any superconducting state even when we pushed V_g to 7 V and cooled down to 300 mK as shown in Figure 5(c). At the base temperature of 300 mK, Hall measurement conclusively determines $n_s = 1.2 \times 10^{14}$ cm^{-2} and $\mu = 240$ cm^2 V^{-1} s^{-1} at $V_g = 7$ V. We also carried out temperature dependent Hall measurements to obtain n_s and μ for different V_g. It was found that n_s reaches 1.5×10^{14} cm^{-2} at T = 16 K and $V_g = 6$ V. The n_s is found to decrease when T is lower than 16 K. This might indicate that electron density is still not high enough to observe any correlated electronic states at such low temperature range.

In summary, we have investigated IL gating on ALD passivated GaN field-effect transistors and Hall-bar devices under different V_g conditions. We find that 4 cycles of ALD TMA and H_2O process can effectively passivate GaN surfaces, which allows us to obtain ultra-high electron densities and the highest I_{ds} among all bulk GaN FETs. R_{sh}, R_c, and n_s at various V_g are determined. Both room temperature and low temperature characteristics reveal ultra-high electron density exceeding 10^{14} cm^{-2} at the device surface, achieved on a conventional semiconductor GaN with the potential to explore their correlated physics phenomena in the material systems with much higher transport mobility.

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[1] J. T. Ye, Y. J. Zhang, R. Akashi, M. S. Bahramy, R. Arita, and Y. Iwasa, Science **338**, 1193 (2012).
[2] K. Ueno, S. Nakamura, H. Shimotani, H. T. Yuan, N. Kimura, T. Nojima, H. Aoki, Y. Iwasa, and M. Kawasaki, Nat. Nanotechnol. **6**, 408 (2011).
[3] J. T. Ye, S. Inoue, K. Kobayashi, Y. Kasahara, H. T. Yuan, H. Shimotani, and Y. Iwasa, Nat. Mater. **9**, 125 (2010).
[4] S. Jo, D. Costanzo, H. Berger, and A. F. Morpurgo, Nano Lett. **15**, 1197 (2015).

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[5]Y. J. Yu, F. Y. Yang, X. F. Lu, Y. J. Yan, Y. H. Cho, L. G. Ma, X. H. Niu, S. Kim, Y. W. Son, D. L. Feng, S. Y. Li, S. W. Cheong, X. H. Chen, and Y. B. Zhang, Nat. Nanotechnol. **10**, 270 (2015).
[6]M. Suda, R. Kato, and H. M. Yamamoto, Science **347**, 743 (2015).
[7]H. Ryssel and I. Ruge, *Ion Implantation* (Wiley, Chichester, 1986).
[8]Y. Xuan, Y. Wu, and P. D. Ye, IEEE Electron Devices Lett. **29**, 294 (2008).
[9]Y. Saito and Y. Iwasa, ACS Nano **9**, 3192 (2015).
[10]E. Uesugi, H. Goto, R. Eguchi, A. Fujiwara, and Y. Kubozono, Sci. Rep. **3**, 1595 (2013).
[11]H. T. Yuan, H. Shimotani, A. Tsukazaki, A. Ohtomo1, M. Kawasaki, and Y. Iwasa, Adv. Funct. Mater. **19**, 1046 (2009).
[12]G. F. Brown, J. W. Ager III, W. Walukiewicz, W. J. Schaff, and J. Wu, Appl. Phys. Lett. **93**, 262105 (2008).
[13]M. Endo, D. Chiba, H. Shimotani, F. Matsukura, Y. Iwasa, and H. Ohno, Appl. Phys. Lett. **96**, 022515 (2010).
[14]J. J. Nelson and A. M. Goldman, Phys. Rev. B **91**, 241304(R) (2015).
[15]P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, Appl. Phys. Lett. **83**, 180 (2003).
[16]C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, Appl. Phys. Lett. **92**, 071901 (2008).
[17]C. Y. Tsai, T. L. Wu, and A. Chin, IEEE Electron Devices Lett. **33**, 35 (2012).
[18]Y. Q. Wu, P. D. Ye, G. D. Wilk, and B. Yang, Mater. Sci. Eng. B **135**, 282 (2006).
[19]K. S. Im, C. H. Won, Y. W. Jo, J. H. Lee, M. Bawedin, S. Cristoloveanu, and J. H. Lee, IEEE Trans. Electron Devices **60**, 3012 (2013).
[20]D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, Proc. IEEE **89**, 259 (2001).
[21]D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley-Interscience, Tempe, 2007).
[22]B. V. Zeghbroeck, *Principle of Semiconductor Devices* (University of Colorado, Colorado, 2002).
[23]H. Liu, M. W. Si, Y. X. Deng, A. T. Neal, Y. C. Du, S. Najmaei, P. M. Ajayan, J. Lou, and P. D. Ye, ACS Nano **8**, 1031 (2014).
[24]L. M. Yang, K. Majumdar, H. Liu, Y. C. Du, H. Wu, M. Hatzistergos, P. Y. Hung, R. Tieckelmann, W. Tsai, C. Hobbs, and P. D. Ye, Nano Lett. **14**, 6274 (2014).
[25]M. M. Perera, M. W. Lin, H. J. Chuang, B. P. Chamlagain, C. Wang, X. Tan, M. M. C. Cheng, D. Tománek, and Z. X. Zhou, ACS Nano **7**, 4449 (2013).
[26]S. J. Hong and K. Kima, Appl. Phys. Lett. **89**, 042101 (2006).
[27]H. Kambayashi, Y. Niiyama, S. Ootomo, T. Nomura, M. Iwami, Y. Satoh, S. Kato, and S. Yoshida, IEEE Electron Devices Lett. **28**, 1077 (2007).

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