

Atomic-layer-deposited Al₂O₃/GaAs metal-oxide-semiconductor field-effect transistor on Si substrate using aspect ratio trapping technique

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High quality GaAs epilayers grown by metal-organic chemical vapor deposition are demonstrated on a SiO₂-patterned silicon substrate using aspect ratio trapping technique, whereby threading dislocations from lattice mismatch are largely reduced via trapping in SiO₂ trenches during growth. A depletion-mode metal-oxide-semiconductor field-effect transistor (MOSFET) is demonstrated on a *n*-doped GaAs channel with atomic-layer deposited Al₂O₃ as the gate oxide. The 10 μm gate length transistor has a maximum drain current of 88 mA/mm and a transconductance of 19 mS/mm. The surface mobility estimated from the accumulation drain current has a peak value of ~500 cm²/Vs, which is comparable with those from previously reported depletion-mode GaAs MOSFETs epitaxially grown on semi-insulating GaAs substrates. © 2008 American Institute of Physics. [DOI: 10.1063/1.3050466]

To meet the goal of continuous scaling by International Technology Roadmap for Semiconductor, the traditional Si complementary-metal-oxide-semiconductor (CMOS) industry is now facing a series of grand challenges. In search of alternative channel materials, III-V compound semiconductors are now receiving much attention for MOS devices due to their high electron mobility. It is of great interest and economic importance to develop epitaxial growth technique to integrate III-V high-mobility channel materials on Si substrates for future CMOS applications. Several big challenges of III-V growth on Si substrates are as follows: the high threading dislocation density (TDD) stemming from large lattice mismatch between III-V and Si, the high thermal stress arising from large thermal expansion coefficient mismatch, the formation of antiphase domains, etc. Several methods have been studied to address the lattice mismatch problem since the mid 1980s.^{1–6} However, a process with consistently low TDD has not been demonstrated, except via step-graded Ge/Si_{1-x}Ge_x/Si buffer layers,^{7–9} which are likely too thick (~10 μm) for practical integration onto silicon for CMOS. Exploration of heterogeneously grown GaAs on Si for MOS applications has been very limited. True MOS field-effect transistors (MOSFETs) have not been demonstrated yet using any III-V on silicon technique. Recently, aspect ratio trapping (ART)^{10–13} approach shows quite promising results. By trapping lattice-mismatch induced threading dislocations between vertical dielectric sidewalls, defect-free Ge and GaAs regions can be grown in SiO₂ trenches directly on Si substrates. In this letter, a GaAs MOSFET on Si substrate with the epi-GaAs layers grown by the ART technique, with comparable performance with its counterpart grown on GaAs semi-insulating substrates, has been demonstrated and characterized. The growth of high-quality III-V materials on Si enables to effectively integrate the current III-V MOSFET research on Si CMOS platform. It also provides other appli-

cation opportunities such as integration of optoelectronic, photonic or photovoltaic devices on silicon wafers.

The epitaxial GaAs layers were grown by metal-organic chemical vapor deposition (MOCVD) on Si substrate using the ART technique, which has previously been demonstrated for heteroepitaxial growth of Ge, GaAs, and InP on Si with low TDD.^{10–13} The ART heteroepitaxial technique is compatible with the conventional CMOS processes. The film quality was analyzed by transmission electron microscopy (TEM) and x-ray diffraction, as well as photoluminescence measurements. Great defect reduction in the GaAs or Ge epilayer was demonstrated and provides a platform to integrate alternative channel materials on Si for ultimate CMOS applications. The detailed material structure is schematically shown in Fig. 1(a), and Fig. 1(b) shows the cross section of the scanning electron microscopy (SEM) image of the corresponding structure. A 500 nm thick thermal oxide layer was grown on a *p*-type Si (100) substrate. Multiple SiO₂ trenches were defined by conventional photolithography and reactive ion etching with three different trench widths: 180, 250, and 350 nm. The chemistry used in the AMAT SUPER dry etcher is a mixture of C₄F₈, CO, and Ar gas. The cleaning step after the etch process is critical as a carbon-containing layer is formed in the bottom of the trench and this layer must be

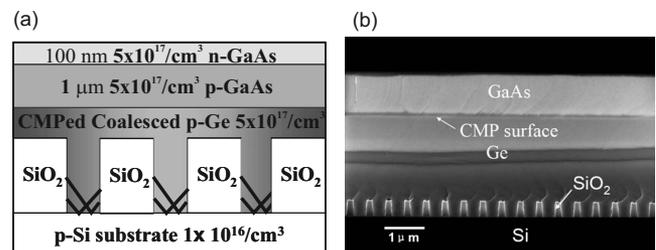


FIG. 1. (a) Cross-sectional schematic view of the ART structure with detailed doping and thickness information. The thick V-shaped lines within SiO₂ trenches are the threading dislocation fault lines. (b) Cross-section SEM image of the GaAs grown by ART technique.

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removed to allow high-quality Ge to be grown. The bottom of the trenches were cleaned by growing 25 nm of SiO₂ using a 1000 °C dry oxidation process and stripping that with a 4 min etch in 100:1 diluted HF solution. *P*-type Ge was then epitaxially grown within all trenches by conventional MOCVD process. These narrow trenches, which can be arbitrary long, are used to trap the threading dislocations and were crucial in the heteroepitaxial growth in order to significantly reduce the TDD. Previous study has shown that for Ge (or III-V) layers grown in the 200–400 nm wide oxide trenches, threading dislocations originating at the Ge/Si interface terminate at the oxide sidewall within the first several 100 nm of epitaxial growth. There was no evidence of defect generation along the SiO₂ sidewall or extended defects out of the trench shown by the cross-sectional TEM images.^{10–13} As a result, the very top layer of the Ge film beyond the defect-trapping region is substantially defect-free. After completely filling the trenches, Ge epilayer was further grown above the trenches and eventually coalesced over the oxide patterns. A step of chemical mechanical polishing (CMP) was used after the coalesced Ge layer was grown to improve the surface morphology. A 100 nm $5 \times 10^{17}/\text{cm}^3$ *n*-GaAs channel and a 1 μm $1 \times 10^{18}/\text{cm}^3$ *p*-GaAs buffer layer were grown by MOCVD on top of the planarized coalesced Ge film as shown in Figs. 1(a) and 1(b).

Depletion-mode MOSFETs were fabricated on this GaAs/Si structure. After a precleaning step of GaAs surface by HCl solution, (NH₄)₂S was used as a surface pretreatment process for 10 min, followed by the growth of a 10 nm atomic-layer-deposited (ALD) Al₂O₃ layer as gate dielectric using an ASM F-120 reactor at 300 °C. A step of postdeposition annealing at 500 °C for 30 s in nitrogen ambient was used to improve the interface quality. Mesa etching of the top GaAs layer by H₂SO₄:H₂O₂:H₂O solution to a depth of about 100 nm was used as a device isolation. Source and drain regions were defined by photolithography after the mesa etching. AuGe/Ni was used as the contact material by e-beam evaporation and lift-off process, followed by a rapid thermal annealing at 400 °C for 30 s in nitrogen ambient. The gate was similarly defined by photolithography and lift-off with Ni/Au as the gate metal. The reported device was fabricated on 250 nm trenches with 250 nm spacing between neighboring trenches. Electrical characterization was carried out using a Keithley 4200 m.

Figure 2 is the dc output characteristics of a GaAs MOSFET with a channel length of 10 μm and a channel width of 60 μm . The gate bias is from +3 to –4 V with a step of –0.5 V. The drain bias is swept from 0 to 2 V. Due to the non-self-aligned process as well as the nonoptimized Ohmic contact, the knee voltage is larger than 1 V. The output performance could be further improved by reducing the access resistance and contact resistance. The *I*-*V* characteristic has very small hysteresis during the sweeping back of drain voltage. This indicates that the mobile charge density in the dielectric and the slow interface trap density are low and the channel material is of high quality. The decent current enhancement of 40 mA/mm in the accumulation region ($V_g > -0.5$ V) suggests good quality of the interface at the upper half bandgap of GaAs.

Figure 3 is the transfer characteristics of the same GaAs MOSFET. The gate voltage is swept from –5 to 3 V with a fixed drain bias at 2 V. The maximum saturation drain cur-

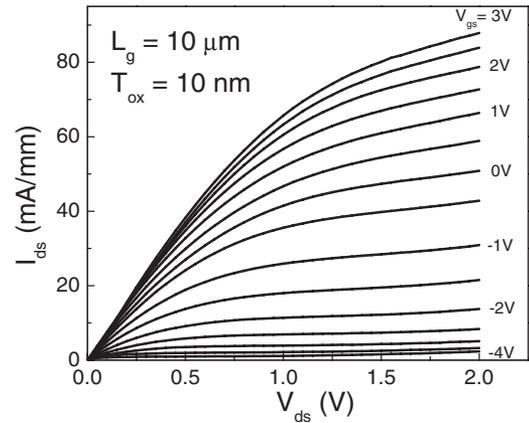


FIG. 2. I_{ds} vs V_{ds} as a function of V_{gs} on a 10 μm gate-length depletion-mode GaAs MOSFET on Si with 10 nm ALD Al₂O₃ as gate dielectric. V_{gs} changes from +3 V (top) to –5 V (bottom) with a step of –1 V.

rent is >88 mA/mm at a gate bias of 3 V and the maximum transconductance is ~ 19 mS/mm at a gate bias of –0.6 V. This current and transconductance could potentially reach 880 mA/mm and 190 mS/mm if the devices would be linearly scaled to 1 μm gate length. The flatband condition in the depletion-mode transistor is around the gate bias where the transconductance in saturation region reaches maximum. In this case, it is around –0.6 V. When the gate bias decreases below this flatband voltage, the continuous depletion of the conducting channel increases the depletion depth. As a result, the gate capacitance is reduced and the transconductance also decreases. On the other hand, with the increase in gate bias above this flatband voltage, the surface potential of the semiconductor moves from depletion to accumulation, with an almost fixed accumulation layer depth. The additional accumulation carrier density at the interface gains more drain current. However, the interface trap density becomes larger when the Fermi level approaches accumulation region or conductance band edge. This degrades the observed transconductance, as well as the mobility. This explains well that the transfer characteristics can determine roughly the position of the flatband voltage.

In order to quantitatively characterize the ALD Al₂O₃/GaAs interface, the accumulation mobility is used and measured by the similar concept of inversion mobility. This surface mobility is directly affected by the interface

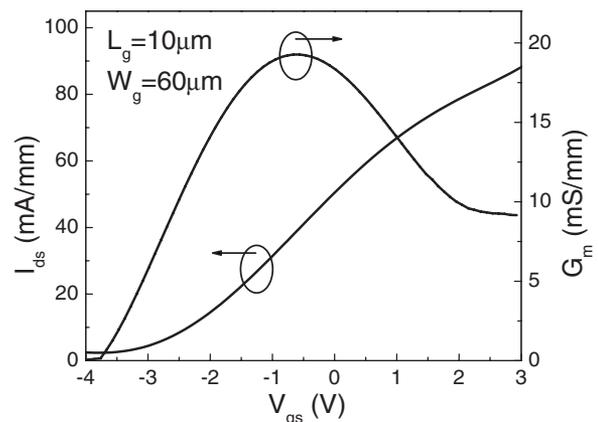


FIG. 3. Transfer characteristics of the same MOSFET with $V_{ds}=2$ V. The maximum drain current is ~ 80 mA/mm and maximum transconductance is ~ 19 mS/mm.

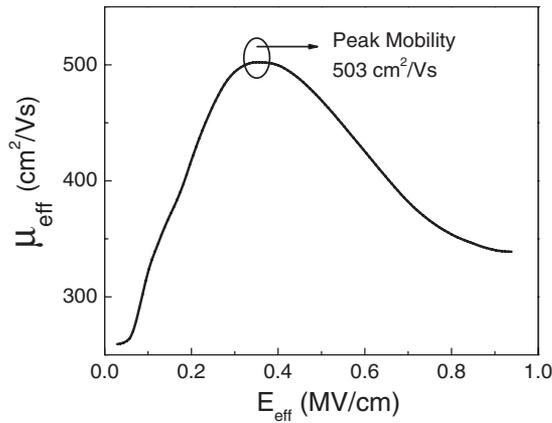


FIG. 4. Effective accumulation electron mobility (μ_{eff}) vs transverse effective electric field (E_{eff}) of GaAs MOSFET on Si substrate.

quality and is suffered from three main scattering mechanisms. Phonon scattering and Coulomb scattering due to the ionized charge centers dominate in the low transverse electric field region, while surface roughness scattering and phonon scattering prevail in the high field region. The high field region here refers to the strong accumulation region. Using the *CV* results at 100 kHz, the total accumulation carrier charge Q_{acc} can be calculated. Transfer characteristics in the linear region ($V_{\text{ds}}=0.1$ V) is used to calculate the accumulation channel sheet resistance R_{ch} as

$$R_{\text{ch}} = \frac{V_{\text{ds}} W_g}{I_{\text{acc}} L_g} = \frac{1}{\mu_{\text{eff}} Q_{\text{acc}}}, \quad (1)$$

where V_{ds} is the drain bias, I_{acc} is the accumulation current by subtracting the bulk channel current from the total current, W_g is the channel width, L_g is the gate length, and μ_{eff} is the effective accumulation mobility. Since the conductance component from the bulk channel region remains at its maximum and is constant in the entire accumulation region, the extra current conduction comes from the accumulation charge layer, which is represented by accumulation current I_{acc} . For this depletion-mode MOSFET, the transverse electric field has contribution only from the accumulation layer. This is different from the case of inversion-mode devices, which contains a charge component from the depletion region. The effective electric field E_{eff} is simply

$$E_{\text{eff}} = \frac{\epsilon_{\text{ox}}(V_{\text{gs}} - V_{\text{Gi}})}{2\epsilon_{\text{GaAs}}T_{\text{ox}}}, \quad (2)$$

where T_{ox} is the oxide physical thickness and V_{Gi} is the voltage at the point of inflection of the I_{ds} versus V_{gs} curve (near the flatband voltage). As can be seen from Fig. 4, the peak accumulation mobility is around $500 \text{ cm}^2/\text{V s}$ at an effective electric field of 0.4 MV/cm , which is higher than the Si universal mobility curve for the SiO_2/Si interface. Note that this mobility value is underestimated since the parasitic resistance is not taken into account yet. The mobility value of this device (GaAs on Si) is comparable with the values of 480 and $400 \text{ cm}^2/\text{V s}$ at 0.4 MV/cm previously reported on

depletion-mode $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs MOSFETs on GaAs semi-insulating substrates, respectively.^{14,15} This encouraging result indicates that ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ interface and the ART grown GaAs channel on silicon substrate is of high quality.

In conclusion, depletion-mode ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFETs are demonstrated on high-quality MOCVD epi-GaAs grown on the post-CMP Ge coalesced layer on Si using the ART heteroepitaxial technique. The relatively high current and effective accumulation electron mobility shows the comparable performance between GaAs MOSFETs on Si substrate and their counterparts on GaAs substrates. The high quality of ART grown GaAs on Si and ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ interface demonstrate the great promise to integrate *n*-channel III-V MOSFETs on large-area Si wafers. *P*-channel III-V MOSFETs are expected to have low performance due to their low hole mobility in III-V semiconductors in general. However, Ge *p*-channel MOSFETs show the great promise due to its high hole mobility in Ge, compared to Si. The ART technique opens up a way to integrate high-quality Ge and III-V semiconductors on Si and develop an ultimate CMOS technology combined with III-V *n*-channel MOSFETs and Ge *p*-channel MOSFETs on the Si platform.

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- ¹E. A. Fitzgerald and N. Chand, *J. Electron. Mater.* **20**, 839 (1991).
- ²D. B. Noble, J. L. Hoyt, C. A. King, J. F. Gibbons, T. I. Kamins, and M. P. Scott, *Appl. Phys. Lett.* **56**, 51 (1990).
- ³R. M. Sieg, S. A. Ringel, S. M. Ting, S. B. Samavedam, M. Currie, T. Langdo, and E. A. Fitzgerald, *J. Vac. Sci. Technol. B* **16**, 1471 (1998).
- ⁴T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, A. Lochtefeld, and D. A. Antoniadis, *Appl. Phys. Lett.* **76**, 3700 (2000).
- ⁵Q. Li, S. M. Han, S. R. J. Brueck, S. Hersee, Y.-B. Jiang, and H. Xu, *Appl. Phys. Lett.* **83**, 5032 (2003).
- ⁶S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubichev, W. K. Liu, M. Radosavljevic, W. Rachmady, and R. Chau, *IEEE Electron Device Lett.* **28**, 685 (2007).
- ⁷M. M. Oye, D. Shahrjerdi, I. Ok, J. B. Hurst, S. D. Lewis, S. Dey, D. Q. Kelly, S. Joshi, T. J. Mattord, X. Yu, M. A. Wistey, J. S. Harris, Jr., A. L. Holmes, Jr., J. C. Lee, and S. K. Banerjee, *J. Vac. Sci. Technol. B* **25**, 1098 (2007).
- ⁸D. Choi, E. Kim, P. C. McIntyre, and J. S. Harris, *Appl. Phys. Lett.* **92**, 203502 (2008).
- ⁹D. Shahrjerdi, N. Nuntawong, G. Balakrishnan, D. I. Garcia-Gutierrez, A. Khoshakhlagh, E. Tutuc, D. Huffaker, J. C. Lee, and S. K. Banerjee, *J. Vac. Sci. Technol. B* **26**, 1182 (2008).
- ¹⁰J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, *Appl. Phys. Lett.* **90**, 052113 (2007).
- ¹¹J. Bai, J.-S. Park, Z. Cheng, M. Curtin, B. Adekore, M. Carroll, A. Lochtefeld, and M. Dudley, *Appl. Phys. Lett.* **90**, 101902 (2007).
- ¹²J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, *Appl. Phys. Lett.* **91**, 021114 (2007).
- ¹³J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, *J. Appl. Phys.* **103**, 106102 (2008).
- ¹⁴P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H. J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, *Appl. Phys. Lett.* **83**, 180 (2003).
- ¹⁵P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H. J. L. Gossmann, M. Hong, K. K. Ng, and J. Bude, *Appl. Phys. Lett.* **84**, 434 (2004).