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How Important Is the Metal−Semiconductor Contact for Schottky Barrier Transistors: A Case Study on Few-Layer Black Phosphorus?

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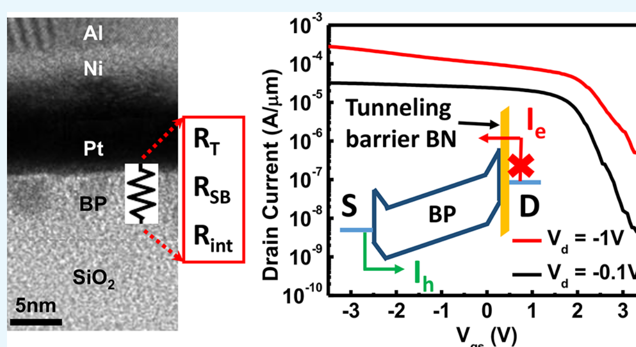
Supporting Information

ABSTRACT: Black phosphorus (BP) is a recently rediscovered layered two-dimensional (2D) semiconductor with a direct band gap (0.35−2 eV), high hole mobility (300−5000 cm^2/Vs), and transport anisotropy. In this paper, we systematically investigated the effects of metal−semiconductor interface/contacts on the performance of BP Schottky barrier transistors. First, a "clean" metal−BP contact is formed with boron nitride (BN) passivation. It is found that the contact resistance of the clean metal−BP contact is seven times less than the previously reported values. As a result, high-performance top-gate BP transistors show a record high ON-state drain current (I_{on}) of 940 μA/μm. Second, BN tunneling barriers are formed at the source/drain contacts to help understand the abnormally high OFF-state drain current (I_{off}) in devices with clean metal−BP contacts. This high I_{off} is attributed to the electron tunneling current from the drain to the channel. Finally, the I_{on}/I_{off} of BP field-effect transistors can be significantly improved by using an asymmetric contact structure. By inserting a thin BN tunneling barrier at the drain side, I_{off} is reduced by a factor of ∼120 with a cost of 20% reduction in I_{on}. This case study of contacts on BP reveals the importance of understanding the metal−semiconductor contacts for 2D Schottky barrier transistors in general.



INTRODUCTION

Two-dimensional (2D) materials have shown great potential in the application of nanotransistors, especially for beyond 5 nm node technology.[1−5] Among thousands of 2D materials, black phosphorus (BP) has triggered intensive research interests owing to its unique material properties.[6−8] Depending on the number of layers, the band gap of BP varies from 0.35 to 2.0 eV.[9,10] The hole Hall mobility of BP is as high as 5200 cm^2/V s at room temperature with hexagonal boron nitride (h-BN) passivation.[11] BP has a puckered honeycomb atomic structure, which leads to its highly anisotropic transport characteristics.[12,13] The moderate direct band gap and high carrier mobility make BP a strong candidate for high-performance transistor applications.[14−19]

However, field-effect transistors (FETs) based on most 2D semiconductors are Schottky barrier transistors.[20−23] Namely, the transistor characteristics are significantly affected by the source/drain Schottky contacts. This phenomenon is more obvious for short-channel devices, where the contact resistance is even more dominant than the channel resistance. It is thus very important to form a low-resistance metal−semiconductor contact to fully access the intrinsic material properties of the channel. Typically, the contact resistance of 2D semiconductor FETs includes three parts: (i) the Schottky barrier resistance (R_{sb}), which is the result of Fermi-level pinning and the difference between the metal work function and the electron affinity of the semiconductor; (ii) the tunneling resistance (R_t) owing to the existence of a physical gap between the metal and the semiconductor. The physical gap may stem from any interfacial oxide; and (iii) the interlayer resistance (R_{inter}) contacting from top layers to bottom layers. R_{inter} is usually much smaller than R_{sb} and R_t. However, in 2D FETs, R_{inter} cannot be ignored, especially for bottom-gate device owing to a significantly higher out-of-plane effective mass, which is usually several times larger than the in-plane effective mass.[24]

One disadvantage of BP is that it easily reacts with O_2 and H_2O in an ambient environment forming an oxide after cleaving from the bulk.[25−27] The existence of this phosphorus oxide/acid at the surface makes the formation of a clean and low-resistance BP−metal interface complicated.[28] This leads us

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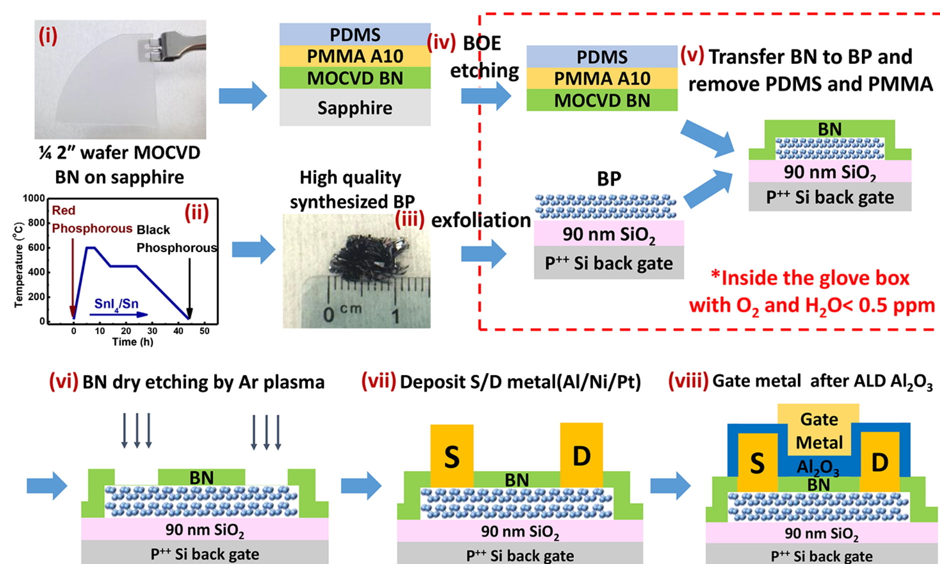

Figure 1. Fabrication process flow for the top-gate BP FETs with BN−Al_2O_3 gate dielectric/passivation layers. Key steps include (i) MOCVD BN, (ii) bulk BP growth, (iii) BP exfoliation, (iv) BN release, (v) BN transfer, (vi) BN dry etching, (vii) S/D metallization, and (viii) ALD Al_2O_3 and gate metallization. Step (iii) BP exfoliation and step (v) BN transfer were performed in a glovebox with O_2/H_2O concentration less than 0.5 ppm.

to believe that much better contacts can be achieved with a clean metal−BP interface by preventing the formation of phosphorus oxide/acid. In this work, we demonstrate how to minimize the total contact resistance ($R_{total} = R_{sb} + R_t + R_{inter}$) using several strategies, including high-work-function contact metal, BN passivation, and top-gate structure. This allows the BP contact resistance to be reduced to a record low value of 0.58 kΩ·μm, resulting in an I_{on} that exceeds 940 μA/μm.[15] As a consequence, the I_{off} is also increased significantly in these low-resistance contact devices. To understand the abnormally high I_{off}, R_t is intentionally increased by adding a thin BN barrier to the contact. It is found that the high I_{off} is due to the reverse electron tunneling current on the drain side, which can be suppressed by the BN tunneling barrier. Finally, by using an asymmetric contact structure with a clean metal−BP contact at the source and BN tunneling barrier at the drain, we have successfully reduced I_{off} by a factor of 120 with only a 20% reduction in I_{on}.

DEVICE FABRICATION

Figure 1 shows the device fabrication flow for fabricating top-gate BP FETs. Few-layer BP flakes were exfoliated onto the 90 nm SiO_2/p^{++} Si substrate. The BN thin film was grown on sapphire by metal−organic chemical vapor deposition (MOCVD) with a thickness of 1.6 nm and a root-mean-square roughness of 0.1 nm.[29,30] The relative dielectric constant of BN is about 3, which is similar to the reported value of CVD BN.[31] MOCVD BN was first transferred onto the BP−SiO_2−Si substrate (details in Materials and Methods). The source/drain region was patterned by electron-beam lithography. After that, BN was etched by a low-power Ar reactive ion etching (RIE) with an etching rate of ∼1 nm/10 s. The BN thickness can be controlled by adjusting the Ar etching time. Figure 2 shows the atomic force microscopy (AFM) image of BN etching pattern after Ar RIE for 10 s. The roughness of BN increases from 0.1 nm to about 0.5 nm after RIE. Immediately after the etching process, 5 nm Pt/8 nm Ni/30 nm Al was deposited as the contact metals. A second dielectric layer, 4 nm Al_2O_3, was deposited by atomic layer deposition (ALD) at 200 °C after the

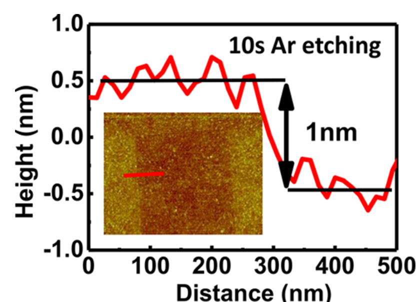

Figure 2. AFM height profile and inset image of BN etched pattern after Ar RIE for 10 s.

metal lift-off process. The total equivalent oxide thickness of the BN−Al_2O_3 top-gate dielectric layer is around 4 nm. Finally, 20 nm Ti/50 nm Au was deposited as the top-gate metal. All devices were fabricated with the current flow along the high-mobility armchair direction of BP, which was determined by polarization-dependent Raman spectra using a HORIBA LabRAM HR800 Raman spectrometer with a 532.8 nm wavelength He−Ne laser. All devices have the same channel length of 200 nm and a thickness between 4 and 12 nm. The characterization of FETs was performed in air at room temperature by using a Keithley 4200 semiconductor parameter analyzer.

RESULTS AND DISCUSSION

A cross-sectional transmission electron microscopy (TEM) image of the fabricated Al−Ni−Pt−BP contact is shown in Figure 3a. A sharp BP−Pt interface can be seen in the picture, although the 2D crystal structure of BP is vague because of the damage caused during the TEM sample preparation. Figure 3b shows the EDS element analysis along the Al−Ni−Pt−BP−SiO_2 stack. No nitrogen or boron is detected (above the detection limit), confirming that the BN barrier layer has been fully etched away. Along the stack, the carbon signal is negligible showing that the organic residue [polydimethylsiloxane (PDMS) or poly(methymethacrylate) (PMMA)] has been removed because of the transfer process. However, a significant

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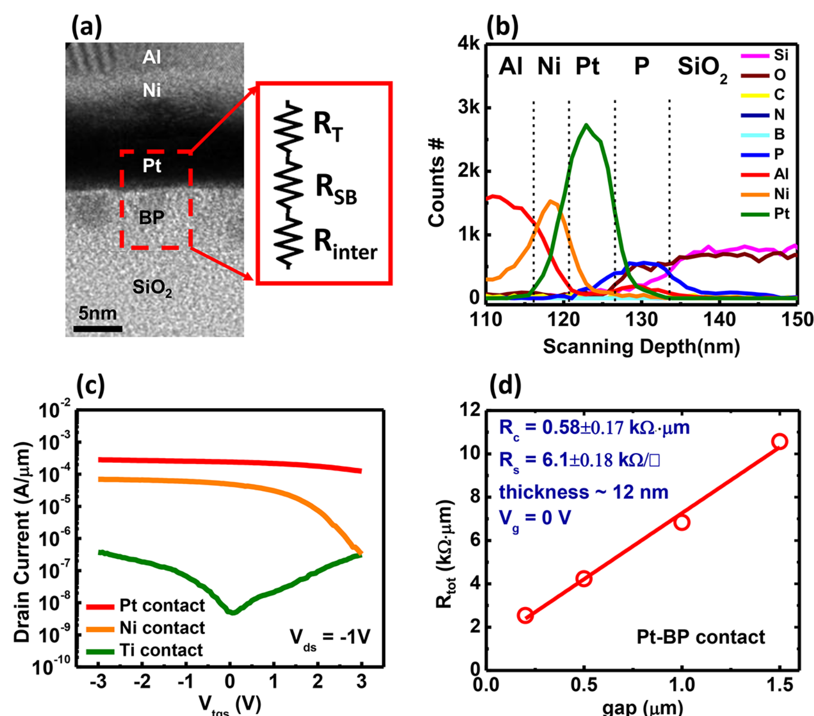

Figure 3. (a) Cross-sectional TEM image of Pt−BP contact and the diagram of the composition of R_c. (b) Element analysis of Pt−BP contact by EDS. The signal of carbon, boron, or nitrogen is below the detection limit. (c) *I*−*V* transfer curves of BP FETs with different contact metals: Pt, Ni, and Ti. (d) TLM resistance of BP with Pt contact at zero back-gate bias. Contact resistance is extracted to be 0.58 kΩ·*μ*m, which is seven times less than the previously reported value.

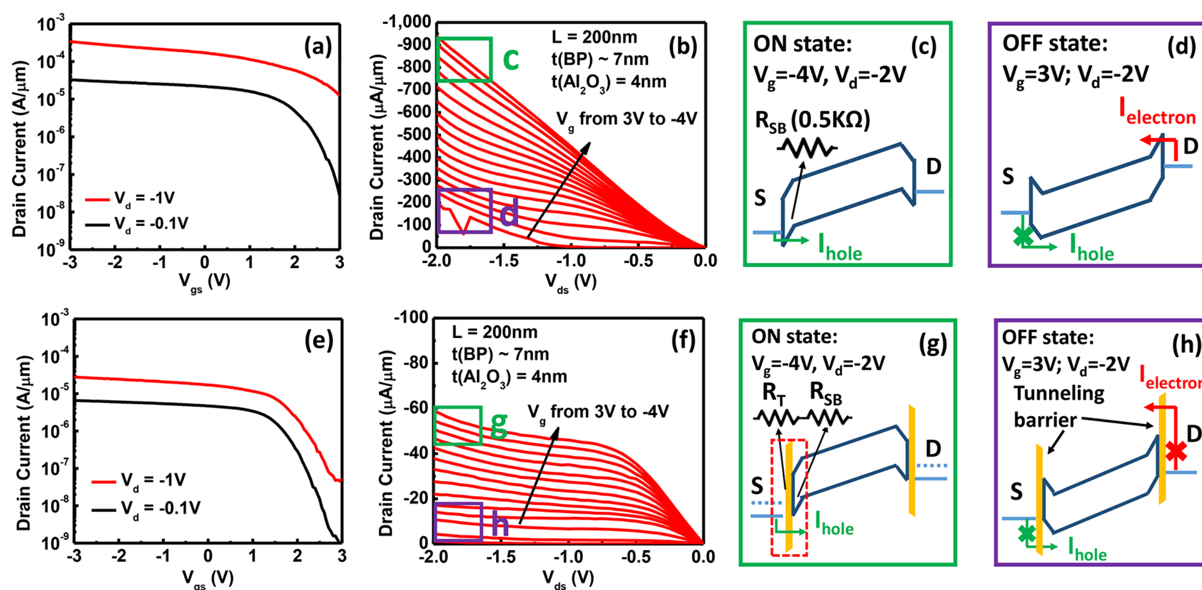

Figure 4. (a−d) BP FETs without BN tunneling barriers at source/drain contacts and (e−h) BP FETs with BN tunneling barriers at both source/drain contacts. (a) Transfer curves and (b) output curves of a 7 nm thick BP PMOSFET without BN tunneling barriers. Band diagram of (c) ON state and (d) OFF state for devices without BN barriers. (e) Transfer curves and (f) output curves of a 7 nm thick BP PMOSFET with two-layer BN tunneling barriers. Band diagram of (g) ON state and (h) OFF state for devices with BN barriers.

amount of oxygen is still detected within the phosphorus layer, even though BP has been fully isolated from O_2 and H_2O by BN−Al_2O_3 passivation. The effectiveness of BN−Al_2O_3 passivation on BP has been confirmed by time-dependent Raman and electrical measurements, as shown in the Supporting Information (accelerated degradation experiment data of BP, BP−BN, and BP−BN−Al_2O_3 and time dependence of *I*−*V* characteristics of BP FETs with BN−Al_2O_3 passivation). Meanwhile, the *I*−*V* hysteresis has also been reduced to 0.25 V after BN−Al_2O_3 passivation.[15] As a result, it is very likely that the oxygen is introduced because of exposure to air between the focused ion beam processing and TEM imaging. If oxygen contamination occurred during exfoliating and processing, a higher oxygen concentration would be expected at the Pt−BP interface than at the BP−SiO_2 interface.

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The selection of a contact metal with the appropriate work function is the critical first step to reducing R_c. Three contact metals with a range of work functions were investigated: Pt (~5.6 eV), Ni (~5.2 eV), and Ti (~4.33 eV). Figure 3c shows the transfer curves of BP FETs with different source/drain metals. Clearly, the FET with BP−Pt contacts performed the best, whereas BP−Ti performed the worst. Interestingly, the device with Ti contacts shows symmetric electron and hole transport, which indicates that the Fermi level at the BP surface and the work function of Ti are aligned near the middle of the band gap. This result is in good agreement with the theoretical energy band diagram of the BP−Ti contact, in which E_c and E_v of few-layer BP are about 4.1−4.2 and 4.5−4.7 eV, respectively.[19] Notably, there is a big difference in the threshold voltage (V_t) between these devices with different contact metals. This is a result of charge transfer from the floating BP channel to the contact metal, where electrons tend to move from the high-potential region (BP channel) to the low-potential region (metal). Consequently, V_t becomes more positive when a higher work function (i.e., lower potential) metal is used.

The contact resistance of BP−Pt contacts is measured with the transfer length method (TLM) on a 12 nm thick sample. At zero back-gate bias, the extracted R_c is about 0.58 kΩ·μm, and the sheet resistance is about 6.1 kΩ/square as shown in Figure 3d. Encouragingly, the measured R_c of the clean BP−metal contact is 1/7 of the previously reported R_c for BP−Pd contacts.[32] Because Pt and Pd have similar work functions, the Schottky barrier height and R_{sb} of the two contacts should be similar. Thus, the significant reduction of total R_c is due to the contribution of the other resistance factors: R_t and R_{inter}, which we will address later in this paper.

The transfer and output characteristics of a 7 nm thick BP FET with Pt contact are shown in Figure 4a,b. Owing to the improvement of R_c, the 200 nm channel length device shows I_{on} as high as 940 μA/μm at a V_{ds} of −2 V. To the best of our knowledge, this is the highest I_{on} achieved among all 2D semiconductor-based FETs. However, the I_{on}/I_{off} is about ~10^3 at small drain bias (−0.1 V) and decreases to about ~20 at large drain bias (−1 V). The I_{off} increases to 200 μA/μm at a drain bias of −2 V, and the drain current in Figure 4b increases almost linearly with V_{ds} and does not saturate. The abnormally high I_{off} and nonsaturation phenomena have never been reported for BP FETs. This phenomenon can be explained as follows. First, few-layer BP has a small band gap approaching the bulk value of 0.35 eV, and BP FETs are Schottky barrier transistors, that is, the observed electrical characteristics are the outcomes of both the channel and more importantly the contacts. In principle, the total drain current of a Schottky barrier transistor contains (i) hole current from source to drain and (ii) electron current from drain to source. As can be seen from the band diagram in Figure 4c, in the ON state, the majority of the drain current is the hole current injected from the source terminal. As long as the holes are able to overcome the source Schottky barrier, they can be collected at the drain side. In other words, the total current level is mainly determined by the hole injection at source. In the OFF state, the channel potential is pulled down by the gate voltage to reduce the hole injection at source; however, this gate bias also lowers the potential of the channel region near the drain terminal. Meanwhile, the drain potential is lifted up by the negative drain bias, which results in a steep potential gradient. As a result, the electrons at the drain terminal can be injected into the conduction band of a channel by tunneling through the triangle barrier. In other words, by turning off the forward hole current, the reverse electron current is turned on by top-gate bias. Indeed, this phenomenon is universal for all the top-gate Schottky barrier transistors. However, the reverse tunneling probability at the drain side is inversely related to the Schottky barrier height for minority carriers. Consequently, a high reverse tunneling current is observed in narrow band gap semiconductors. For wide band gap 2D semiconductors, such as MoS_2, the drain-to-channel Schottky barrier for holes is so large that the tunneling current can be ignored in the OFF state. So far, the device characteristics have been well-explained by the transport model. However, for narrow band gap BP devices, this raises important questions: what happens in the BP devices with both low I_{off} and I_{on} as reported in the literature and where does this inconsistency come from?

A possible explanation for the absence of a high reverse tunneling current in previously reported BP devices is the presence of a tunneling barrier at the source/drain interface. This additional tunneling barrier may stem from surface phosphorus oxide/acid formed during fabrication. The presence of this tunneling barrier would explain why previous works reported much higher R_c than what we are reporting in this work. On the other hand, this tunneling barrier blocks the reverse electron tunneling current, which leads to a low I_{off}. To verify this hypothesis, we fabricated BP FETs with a thin layer of BN intentionally kept at the source/drain contacts. Figure 4e,f shows the transfer and output characteristics of a BP FET with a thin BN barrier (two layers) added to the source/drain contacts. The geometry of this device is the same as the one without a BN barrier. However, there are several clear differences between the electrical characteristics of these two devices: (i) in the ON state, I_{on} of the device with BN contacts is 10 times lower than the device without BN. The reduction of I_{on} is due to the additional tunneling barrier resistance R_t. (ii) In the linear region, the I_d−V_d curve of the device with BN is more linear than the device without BN owing to the Fermi-level depinning.[33,34] Figure 4g shows the band diagram of the device with BN contacts in the ON state. The Schottky barrier height becomes smaller with Fermi-level depinning, and the I_d−V_d curves become more linear. However, R_t increases significantly with insertion of a BN barrier in contacts. As a result, the total R_c (R_t + R_{sb} + R_{inter}) of the device with BN is much larger than that of the device without BN. This also tells us that the linear I_d−V_d curves do not necessarily indicate that an Ohmic contact has been achieved. (iii) In the saturation region, the current saturates at V_{ds} < −0.5 V. Below this voltage, the drop across the tunneling barrier becomes dominant. Increasing V_d no longer improves the drain current. (iv) In the OFF state, I_{off} is reduced by a factor of 400 at a V_{ds} of −1 V due to the presence of the BN barrier at the drain terminal, which reduces the reverse electron tunneling current. Figure 4h shows the band diagram of the device with BN contacts in the OFF state. In short, the presence of a tunneling barrier at source/drain contacts reduces I_{on}, leads to linear I−V (Fermi-level depinning), leads to current saturation (V_d drop at contacts), and reduces I_{off} (blocks the reverse tunneling current). All of these observations from our BP devices with BN barriers are in good agreement with the characteristics of the previously reported BP devices, which did not use any passivation method to avoid the formation of phosphorus oxidation at contacts.[7,8,14,16,21,32] As a result, for Schottky barrier transistors, it is extremely important to distinguish between the contribution

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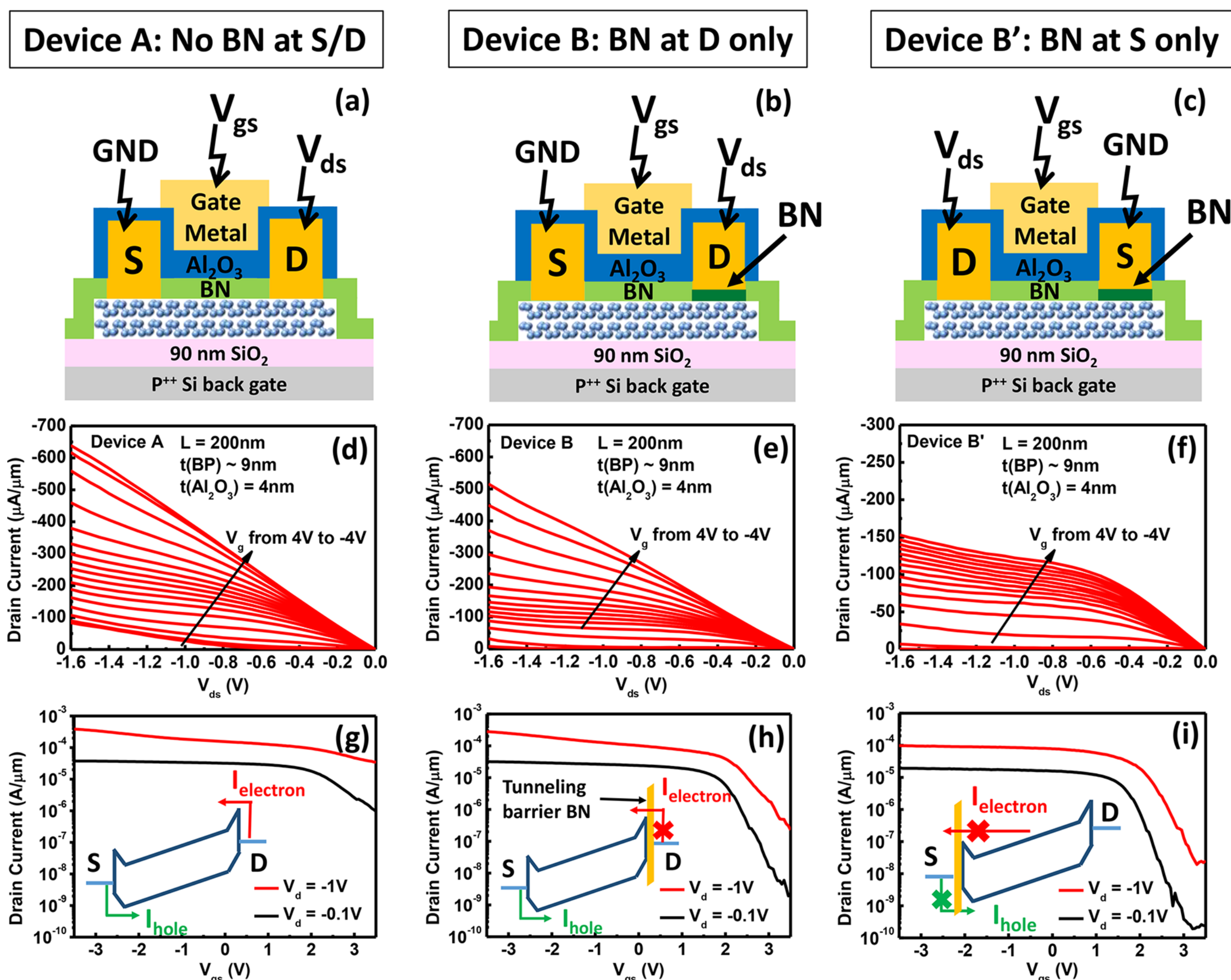

Figure 5. Device A: no BN tunneling barrier at source/drain. Device B: with bilayer BN tunneling barrier only at drain. Device B′: with BN tunneling barrier only at source. Schematic diagram for (a) device A, (b) device B, and (c) device B′. Output curves for (d) device A, (e) device B, and (f) device B′. Transfer curves and band diagrams for (g) device A, (h) device B, and (i) device B′. Device A and device B(B′) were made from the same BP flake.

from the contacts and the intrinsic channel to the overall electrical characteristics.

Taking advantage of the benefits of having a clean BP−metal contact (high I_{on}) and a BN barrier contact (low I_{off}), we have demonstrated an asymmetric source/drain contact structure to improve the I_{off}, while keeping the I_{on} as high as possible. It is well-known that in FETs I_{on} is mainly controlled by the electrostatics at the source terminal. The asymmetry between source and drain can be used to suppress either the electron or the hole current, depending on the sign of the drain voltage.[35−37] For BP Schottky barrier transistor, the majority current (i.e., forward hole current) is determined by the potential barrier from metal to the source contact region. The reverse electron current can be suppressed by adding a tunneling barrier at the drain terminal without losing too much hole current. Figure 5a−c shows the schematic diagram and measurement configuration for a BP FET without BN barriers (device A) and a BP FET with only one BN barrier (~bilayer thickness) at the drain (device B) or the source (device B′). Device A and device B(B′) were fabricated from the same BP flake to reduce potential variability between flakes.

The output and transfer curves of device A are shown in Figure 5d,g. The I_{on} and I_{off} are about 638 and 84 μA/μm, respectively, at a V_{ds} of −1.6 V for the device without BN. With a BN tunneling barrier at the drain side, the I_{off} is reduced by a factor of 120 to 700 nA/μm at a V_{ds} of −1.6 V, whereas I_{on} is still about 80% of the device without the BN barrier. Because I_{on} is mainly determined by the source contact, a BN barrier at the drain does not have a significant impact. Figure 5f,i shows the output and transfer curves of device B′ that has a BN barrier at the source terminal. As expected, the device shows a much smaller I_{on} of 153 μA/μm and has current saturation as well. We conclude that the reverse electron tunneling current or high I_{off} current of BP FETs can be significantly reduced by an asymmetric source/drain contact structure and contact engineering.

In general, the strategies used in this work can be applied to other Schottky-type FETs. The strategies (i) include BN or other effective passivation for environmentally sensitive materials; (ii) choose contact metals with proper work function for either electron or hole transport; and (iii) control/suppress the electron or hole current by tuning the contact tunneling

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barrier. As a case study on BP, we have successfully utilized these methods to improve the electrical performance of BP FETs.

CONCLUSIONS

To summarize, the BP−metal contact has been systematically studied and improved, resulting in record low contact resistance. As a result, record high I_{on} of BP FETs has also been obtained. However, an abnormally high I_{off} of BP FETs is also identified owing to the reverse electron tunneling current at the drain terminal. By contact engineering, the I_{off} has also been significantly reduced with minor sacrifice in I_{on}. All of these results have shown the importance of contacts for its electrical characteristics in Schottky barrier transistors.

MATERIALS AND METHODS

BP Bulk Synthesis. High-quality bulk BP was synthesized from red phosphorus and SnI_4−Sn in a sealed quartz ampoule. A growth temperature between 500 and 600 °C for 20−50 h produced single crystals of BP.

BN Thin-Film Synthesis. Few-layer sp^2 BN was synthesized on 1/4 2 in. sapphire wafers by MOCVD at 1050 °C and 20 Torr from triethylborane and ammonia with a III/IV source ratio of 2250. The Raman peak position and full width at half maximum for the BN E_{2g} mode are 1370 and 24 cm^{-1}, respectively.

Transfer of BN to the BP−SiO_2 Substrate. BN−sapphire samples (size of 5 mm × 5 mm) were coated with a layer of PMMA A10 (3000 rpm, 2 min) and then a PDMS film (Gel-Pak, PF-30-X4). The BN film was separated from the sapphire substrate after etching in buffered oxide etch for 2−3 h at room temperature. The PDMS−PMMA−BN film was rinsed and dried before transferring to the BP−SiO_2−Si substrate. The sample was baked at 100 °C for 30 min after the transfer process to improve the adhesion between BP and BN. The critical processes of BP exfoliation and BN transfer were all performed in a glovebox with H_2O and O_2 concentrations <0.5 ppm to prevent the oxidation of BP. PDMS can be lifted off, and PMMA is removed after soaking the sample in acetone for about 20 min. A forming gas anneal at 200 °C was used to remove any organic residue.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsomega.7b00634.

Time dependence of integrated intensity of Raman mode for BP samples without BN passivation, with BN passivation, and with BN−Al_2O_3 passivation; BP degradation is accelerated by laser irradiation; time dependence of $I-V$ characteristics of BP FETs with BN−Al_2O_3 passivation; and calculation of BN tunneling barrier thickness by the $I-V$ transport model at low bias (PDF)

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Notes

The authors declare no competing financial interest.

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