β-Ga2O3 Nanomembrane Negative Capacitance Field-Effect Transistors with Steep Subthreshold Slope for Wide Band Gap Logic Applications

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Supporting Information

ABSTRACT: Steep-slope β-Ga2O3 nanomembrane negative capacitance field-effect transistors (NC-FETs) are demonstrated with ferroelectric hafnium zirconium oxide in the gate dielectric stack. Subthreshold slope less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage sweeps with minimum values of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at VDS = 0.5 V. Enhancement-mode operation with a threshold voltage of ~0.4 V is achieved by tuning the thickness of the β-Ga2O3 membrane. Low hysteresis of less than 0.1 V is obtained. The steep-slope, low hysteresis, and enhancement-mode β-Ga2O3 NC-FETs are promising as an nFET candidate for future wide band gap complementary metal-oxide-semiconductor logic applications.

INTRODUCTION

High-temperature solid-state devices and circuits are required for many applications such as in aerospace, automotive, nuclear instrumentations, and geothermal wells.1-2 Silicon-based complementary metal-oxide-semiconductor (CMOS) technology is not able to operate at such high temperatures, which is limited by its relatively small band gap of 1.12 eV. CMOS circuits using wide band gap semiconductors are promising in these high-temperature logic applications. Monoclinic β-Ga2O3 is one of the promising candidates as an n-type channel material because of its ultrawide band gap of 4.6–4.9 eV and high electron mobility of ~100 cm²/V.s.3–10 The ultrawide band gap can suppress the carrier distribution at the tail of Boltzmann distribution at high temperatures. Meanwhile, β-Ga2O3 also has the advantage of having low-cost native bulk substrates that can be synthesized in large sizes through melt-grown Czochralski, edge-defined film-fed growth, and floating zone methods.11-16 To reduce power consumption in wide band gap CMOS logic circuits, enhancement-mode operation with a threshold voltage (Vt) greater than zero and small subthreshold slope (SS) are required, similar to Si CMOS because the enhancement-mode operation and small SS reduce both the static leakage current and the supply voltage.17 The SS of metal-oxide-semiconductor field-effect transistors (MOSFETs) is limited by the Boltzmann thermal distribution of electrons as 2kT/q, which is around 60 mV/dec at room temperature. The SS would increase much more for conventional MOSFETs operated at high temperatures. Negative capacitance FETs (NC-FETs) have been proposed and attracted much attention to overcome the thermionic limit of the SS.18 In an NC-FET, an insulating ferroelectric material layer is inserted in the gate stack and serves as a negative capacitor so that the channel surface potential can be amplified more than the gate voltage, and hence, the device can operate with the SS less than 60 mV/dec at room temperature. Hafnium zirconium oxide (HZO) is a recently discovered CMOS compatible ferroelectric thin-film insulator with the ability to maintain ferroelectricity with an ultrathin physical thickness down to less than 2 nm.19-23 Therefore, the integration of wide band gap semiconductors and ferroelectric HZO can reduce the thermionic SS degradation at high temperatures and can reduce power consumption in high-temperature logic applications.

In this paper, we demonstrate β-Ga2O3 NC-FETs with ferroelectric HZO in a gate dielectric stack. SS less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage (VGS) sweeps with a minimum value of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at VDS = 0.5 V. The enhancement-mode operation is achieved by tuning the thickness of β-Ga2O3 with a Vt of 0.47 V for the forward gate-voltage sweep, a Vt of 0.38 V for the reverse gate-voltage sweep, and a low hysteresis less than 0.1 V.

EXPERIMENTS

Figure 1a shows the schematic diagram of β-Ga2O3 NC-FETs, which consists of a 86 nm thick β-Ga2O3 nanomembrane as the channel, a 3 nm amorphous aluminum oxide (Al2O3) layer and...
a 20 nm polycrystalline HZO layer as the gate dielectric, a heavily n-doped (n++) silicon substrate as the gate electrode, and a Ti/Au source/drain as the metal contacts. The silicon substrate was first cleaned by an RCA standard cleaning and diluted by an HF dip, to remove organic, metallic contaminants, particles, and unintentional oxides, followed by rinsing in deionized water and drying. The substrate was then transferred to an atomic layer deposition (ALD) chamber to deposit a 20 nm Hf1−xZrO2 film at 250 °C, using [(CH3)2N]4Hf (TDMAHf), [(CH3)2N]2Zr (TDMAZr), and H2O as the Hf precursor, Zr precursor, and oxygen precursor, respectively. The Hf1−xZrO2 film with x = 0.5 was achieved by controlling the Hf/Zr ratio. To encapsulate the Hf1−xZrO2 film, 3 nm Al2O3 was subsequently situ-deposited by using Al(CH3)3 (TMA) and H2O as precursors at the same 250 °C, to prevent the degradation of HZO by the reaction with moisture in air. The amorphous Al2O3 layer is also used for capacitance matching and gate leakage current reduction. The importance of this interfacial Al2O3 layer on capacitance matching is discussed in detail in ref 23. Rapid thermal annealing in nitrogen ambient was then performed for 1 min at 500 °C to enhance the ferroelectricity. A thin β-Ga2O3 nanomembrane was mechanically exfoliated and transferred to the Al2O3/HZO/n++ Si substrate from a (−201) β-Ga2O3 bulk substrate with an Sn-doping concentration of 2.7 × 1018 cm−3 (determined by the C–V measurement). Source and drain regions were defined by electron-beam lithography using ZEP520A as the e-beam resist. An Ar plasma bombardment for 30 s was then applied to generate oxygen vacancies to enhance the surface n-type doping for the reduction of the contact resistance, followed by Ti/Au (30/60 nm) electron-beam evaporation and lift-off processes. Figure 1b shows the false-color scanning electron microscopy (SEM) image of the fabricated β-Ga2O3 NC-FETs with four different channel lengths on the same membrane, capturing the β-Ga2O3 membrane and the Ti/Au electrodes. Figure 1c shows the cross-sectional transmission electron microscopy image of the HZO/Al2O3 gate stack. All device electrical characterizations were carried out at room temperature with a Keysight B1500 Semiconductor Parameter Analyzer and a Cascade Summit probe station.

**RESULTS AND DISCUSSION**

Figure 2a shows the polarization versus voltage hysteresis loop (P–V) for the TiN/20 nm HZO/TiN capacitor at different annealing temperatures. The P–V shows a clear dielectric to ferroelectric transition of HZO after annealing, whereas the P–V shows a weak dependence on the annealing temperature above 400 °C. The metal–insulator–metal capacitors are used for the extraction of Landau coefficients (∂α, ∂β, and ∂γ) for the ferroelectric HZO layer only. Figure 2b shows the polarization versus voltage (∂P–V) characteristics for the n++ Si/20 nm HZO/3 nm Al2O3/Ni stack (the same gate stack of β-Ga2O3 NC-FETs) annealed at 450 °C at different voltage sweep ranges. The P–V shows a clear ferroelectric hysteresis loop. The P–V characteristics of a thin-film ferroelectric insulator can be modeled using the Landau–Khalatnikov (L–K) equation. The L–K equation for P–V can be expressed as 

\[ V_i = \alpha \gamma P + 4\beta \gamma P^3 + 6\gamma P^3 + \rho \frac{dP}{dV} \]

where \( V_i \) is the voltage across the ferroelectric insulator, \( P \) is the polarization charge, \( t_i \) is the thickness of the ferroelectric insulator, \( \alpha/\beta/\gamma \) are the Landau coefficients, and \( \rho \) is an equivalent damping constant of the ferroelectric insulator. Landau coefficients are extracted directly from the P–V characteristics in Figure 2a on ferroelectric HZO after annealing. In addition, the Landau coefficients are also extracted by fitting to the experimental data using the L–K equation (assuming \( d\gamma/dt = 0 \) for static P–V measurement) to be \( \alpha = -7.91 \times 10^8 \text{ m/F}, \beta = 1.72 \times 10^{10} \text{ m}^2/\text{F/C}^2 \) and \( \gamma = 0 \text{ m}^2/\text{F/C}^2 \) as shown in Figure 2c. Note that the negative dP/dV shows S-shape, where the negative dP/dV is the negative capacitance, as shown in Figure 2c. However, this negative dP/dV cannot be observed from the experimental P–V (Figure 2a,b) because the negative capacitance state is unstable, which leads to hysteresis in the real experimental P–V measurement. Energy (U) versus charge...
(Q) is plotted based on the experimental Landau coefficients and calculated using L–K equations as in Figure 2d. The negative second-order derivative (d²U/dQ²) also indicates the existence of negative capacitance. The energy of the ferroelectric capacitor tends to stay at the local minimums of the U–Q such that the negative capacitance (where d²U/dQ² < 0) becomes unstable. As a result, NC-FETs may exhibit a large hysteresis if the unstable negative capacitance effect is too strong. The key design for the β-Ga₂O₃ NC-FETs in this work is to stabilize the unstable negative capacitance by matching the capacitance of the Al₂O₃ layer (Cₘ) and the depletion capacitance (C_D) of the β-Ga₂O₃ layer with the capacitance of the ferroelectric HZO layer (C_HZO). Therefore, low hysteresis and sub-60 mV/dec SS at room temperature can be achieved at the same time.

Figure 3a shows the normalized I_D–V_GS characteristics in the log scale of a β-Ga₂O₃ NC-FET. The back-gate bias is swept from ~0.4 to 2 V in 40 mV per step, whereas the drain voltage (V_DS) is biased at 0.1, 0.5, and 0.9 V. The whole sweep takes roughly 1 min. This device has a channel length (L_ch) of 0.5 μm and a channel thickness (T_ch) of 86 nm, measured by an atomic force microscope. This particular thickness is chosen to tune the existence of negative capacitance.

I_D for both forward sweep (SS min,For) and reverse sweep (SS min,Rev) at various V_DS Figure 3b–d shows the SS–I_D characteristics extracted from Figure 3a at V_DS = 0.1, 0.5, and 0.9 V, respectively. The device exhibits SS min,For = 57.2 mV/dec and SS min,Rev = 41.0 mV/dec at V_DS = 0.1 V, SS min,For = 53.1 mV/dec and SS min,Rev = 34.3 mV/dec at V_DS = 0.5 V, and SS min,For = 55.0 mV/dec and SS min,Rev = 34.4 mV/dec at V_DS = 0.9 V. SS less than 60 mV/dec at room temperature is demonstrated for both forward and reverse gate-voltage sweeps even at relatively high V_DS = 0.9 V. SS min,Rev = 34.4 mV/dec as shown in Supporting Information section 1. SS–I_D characteristics at different V_DS are similar, slightly better at high V_DS because of the larger impact of a Schottky barrier at lower V_DS. Because of the large band gap of β-Ga₂O₃, the band-to-band tunneling current at high V_DS is suppressed.

Figure 4a shows the I_D–V_GS characteristics in the linear scale of the same β-Ga₂O₃ NC-FET as in Figure 3. V_T is extracted by linear extrapolation at V_DS = 0.1 V for both forward and reverse gate-voltage sweeps. V_T in the forward gate-voltage sweep (V_T,For) is extracted as 0.47 V, whereas V_T in the reverse gate-voltage sweep (V_T,Rev) is extracted as 0.38 V. Hence, the enhancement-mode operation with V_T greater than zero for both forward and reverse gate-voltage sweeps is demonstrated. A negligible hysteresis is obtained for both on-state (high V_GS as shown in Figure 4a) and off-state (low V_GS as shown in Figure 3a), except that when V_GS is near the threshold voltage region. At the threshold voltage, low hysteresis is achieved to be 90 mV, calculated by using IV_T,Rev − IV_T,For. Note that this hysteresis is negative if we do not take the absolute value because of the gate-voltage-induced polarization charge inside the ferroelectric HZO. This is in stark contrast to the
conventional hysteresis from MOSFETs with interface and oxide traps, where hysteresis is usually positive because of charge trapping in the defect states. The hysteresis of NC-FETs generally comes from two origins. The first origin is from the unstable negative capacitance state in the ferroelectric insulator ($d^2U_{FE}/dQ^2 < 0$). This hysteresis can be completely removed by well-matched capacitances ($C_{GS}$, $C_{ot}$, and $C_{Gp}$) so that $d^2(U_{FE} + U_{ox} + U_{p})/dQ^2$ is generally greater than zero for all $Qs$ for total capacitance to remove the unstable negative capacitance state. The stability condition (static nonhysteretic condition) for 20 nm HZO/3 nm Al$_2$O$_3$ has been confirmed to be fulfilled in ref 23 so that it is not the origin of the hysteresis in the β-Ga$_2$O$_3$ NC-FETs in this work. The second origin of the hysteresis is a dynamic effect of the measurement because of the ferroelectric damping factor ($\rho$) in dynamic $L$–$K$ equations, which can explain the hysteresis measured in the β-Ga$_2$O$_3$ NC-FETs in this work. Figure 4b shows the $I_D$–$V_{DS}$ characteristics of the same β-Ga$_2$O$_3$ NC-FET with $V_{GS}$ from −0.5 to 2.5 V in 0.5 V step and $V_{DS}$ swept from 0 to 2 V. A linear current–voltage relationship at low $V_{DS}$ shows a relatively good contact property at the metal/β-Ga$_2$O$_3$ interface. The relative low drain current in this work, compared to that in ref 10, is not clear. The interface situation of β-Ga$_2$O$_3$ on the HZO gate stack seems very different from that on SiO$_2$ in ref 10. The requirement of a thick β-Ga$_2$O$_3$ membrane (60–80 nm) to observe the β-Ga$_2$O$_3$ enhancement-mode operation indicates the existence of significant interface traps and surface depletion. Although the exact mechanism why interface traps do not affect steep-slope observation on β-Ga$_2$O$_3$ NC-FETs is not clear at this moment, we suspect that it is related to the ultrawide band gap of β-Ga$_2$O$_3$.

**CONCLUSIONS**

Steep-slope β-Ga$_2$O$_3$ NC-FETs are demonstrated with ferroelectric HZO in the gate dielectric stack. SS less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage sweeps with a minimum value of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at $V_{DS} = 0.5$ V. The enhancement-mode operation with a threshold voltage of ~0.4 V is achieved by tuning the thickness of the β-Ga$_2$O$_3$ membrane. In addition, a low hysteresis less than 0.1 V is obtained. The steep-slope, low hysteresis, and enhancement-mode β-Ga$_2$O$_3$ NC-FETs are a promising nFET candidate for future wide band gap CMOS logic applications.

**ASSOCIATED CONTENT**

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsomega.7b01289. Additional details of Ga$_2$O$_3$ MOSFETs with Al$_2$O$_3$ only as gate dielectric (PDF)

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**Author Contributions**

P.D.Y. conceived the idea and supervised the experiments. M.S. studied the ALD of HZO and Al$_2$O$_3$. H.Z. exfoliated the β-Ga$_2$O$_3$ membrane. M.S. and L.Y. performed the $P$–$V$ measurement. M.S. performed the device fabrication and electrical characterization and analyzed the experimental data. M.S. and P.D.Y. co-wrote the manuscript, and all authors commented on it.

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**Notes**

The authors declare no competing financial interest.

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**REFERENCES**


