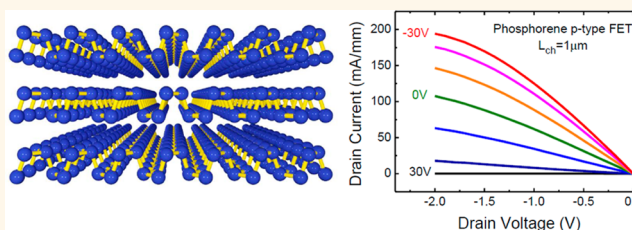


Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility

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ABSTRACT We introduce the 2D counterpart of layered black phosphorus, which we call phosphorene, as an unexplored p-type semiconducting material. Same as graphene and MoS₂, single-layer phosphorene is flexible and can be mechanically exfoliated. We find phosphorene to be stable and, unlike graphene, to have an inherent, direct, and appreciable band gap. Our *ab initio* calculations indicate that the band gap is direct, depends on the number of layers and the in-layer strain, and is significantly larger than the bulk value of 0.31–0.36 eV. The observed photoluminescence peak of single-layer phosphorene in the visible optical range confirms that the band gap is larger than that of the bulk system. Our transport studies indicate a hole mobility that reflects the structural anisotropy of phosphorene and complements n-type MoS₂. At room temperature, our few-layer phosphorene field-effect transistors with 1.0 μm channel length display a high on-current of 194 mA/mm, a high hole field-effect mobility of 286 cm²/V·s, and an on/off ratio of up to 10⁴. We demonstrate the possibility of phosphorene integration by constructing a 2D CMOS inverter consisting of phosphorene PMOS and MoS₂ NMOS transistors.



KEYWORDS: phosphorene · anisotropic transport · transistor · inverter

Preceding the current interest in layered materials for electronic applications, research in the 1960s found that black phosphorus combines high carrier mobility with a fundamental band gap. We introduce its counterpart, which we call phosphorene, as a 2D p-type material. Same as graphene and MoS₂, we find single-layer phosphorene to be flexible and capable of mechanical exfoliation. These findings are in-line with the current interest in layered solids cleaved to 2D crystals, represented by graphene and transition metal dichalcogenides (TMDs) such as MoS₂, which exhibit superior mechanical, electrical, and optical properties over their bulk counterparts and open the way to new device concepts in the post-silicon era.^{1–4} An important advantage of these atomically thin 2D semiconductors is their superior resistance to short channel effects at the scaling limit.⁵ Massless Dirac fermions endow graphene with superior carrier mobility, but its semimetallic nature seriously limits its device applications.^{6,7} Semiconducting TMDs, such as MoS₂, do

not suffer from a vanishing gap^{8,9} and have been applied successfully in flexible n-type transistors⁴ that pave the way toward ultimately scaled low-power electronics. Recent studies on MoS₂ transistors have revealed good device performance with a high drain current of up to several hundred mA/mm, a subthreshold swing down to 74 mV/dec, and an I_{on}/I_{off} ratio of over 10⁸.^{3,10–12} Due to the presence of S vacancies in the film and the partial Fermi level pinning near the conduction band,^{11,13,14} MoS₂ transistors show n-type FET characteristics. In previously demonstrated MoS₂ logic circuits based on n-type transistors only, the static power consumption is likely too large for low-power integrated systems.^{15,16} This fact alone calls for new p-type semiconductors that would allow the realization of CMOS logic in a 2D device. In this study, we introduce phosphorene, a name we coined for a single-layer or few-layer of black phosphorus, as novel 2D p-type high-mobility semiconductors for CMOS applications. We study the optical and electronic properties and transport behavior

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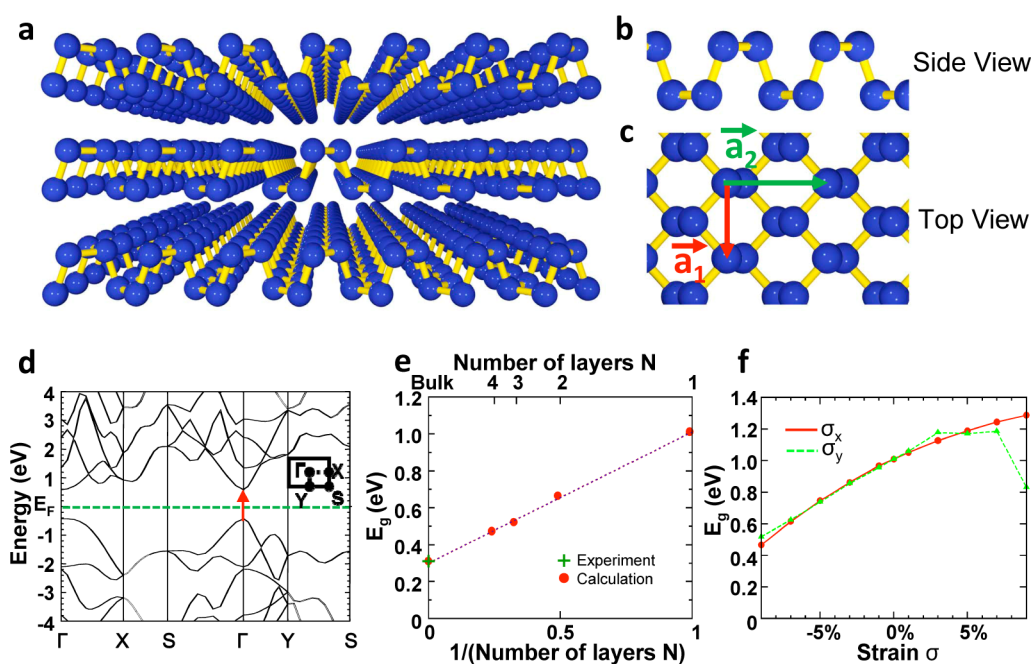


Figure 1. Crystal structure and band structure of few-layer phosphorene. (a) Perspective side view of few-layer phosphorene. (b,c) Side and top views of few-layer phosphorene. (d) DFT-HSE06 band structure of a phosphorene monolayer. (e,f) DFT-HSE06 results for the dependence of the energy gap in few-layer phosphorene on (e) the number of layers and (f) the strain along the *x*- and *y*-direction within a monolayer. The observed band gap value in the bulk is marked by a cross in (e).

and, furthermore, demonstrate the first CMOS inverter using few-layer phosphorene as the p-channel and MoS₂ as the n-channel.

Black phosphorus, the bulk counterpart of phosphorene, is the most stable phosphorus allotrope at room temperature^{17,18} that was first synthesized from white phosphorus under high pressure and high temperature in 1914.¹⁹ Similar to graphite, its layered structure is held together by weak interlayer forces with significant van der Waals character.^{20–22} Previous studies have shown this material to display a sequence of structural phase transformations, superconductivity at high pressures with T_c above 10 K, and temperature-dependent resistivity and magnetoresistivity.^{17,22–27} Two-dimensional phosphorene is, besides graphene, the only stable elemental 2D material that can be mechanically exfoliated.

RESULTS AND DISCUSSION

We have determined the equilibrium geometry, bonding, and electronic structure of black phosphorus, few-layer and single-layer phosphorene using *ab initio* density functional theory (DFT) calculations with the PBE²⁸ and HSE06²⁹ functionals as implemented in the SIESTA³⁰ and VASP³¹ codes. As seen in the optimized structure depicted in Figure 1a–c, phosphorene layers share a honeycomb lattice structure with graphene with the notable difference of nonplanarity in the shape of structural ridges. The bulk lattice parameters $a_1 = 3.36$ Å, $a_2 = 4.53$ Å, and $a_3 = 11.17$ Å, which have been optimized by DFT-PBE calculations, are in good agreement with the experiment. The relatively large

value of a_3 is caused by the nonplanar layer structure and the presence of two AB stacked layers in the bulk unit cell. The orthogonal lattice parameters $a_1 = 3.35$ Å and $a_2 = 4.62$ Å of the monolayer lattice, depicted in Figure 1b,c, are close to those of the bulk structure, as expected in view of the weak 20 meV/atom interlayer interaction that is comparable to graphite. We note that the ridged layer structure helps to keep orientational order between adjacent phosphorene monolayers and thus maintains the in-plane anisotropy; this is significantly different from graphene with its propensity to form turbostratic graphite.³²

Our calculated band structure in Figure 1d indicates that a free-standing phosphorene single layer is a semiconductor with a direct band gap of 1.0 eV at Γ , significantly larger than our calculated band gap value $E_g = 0.31$ eV for the bulk system. These calculations, performed using the HSE06 functional,²⁹ reproduce the observed bulk band gap value 0.31–0.36 eV^{17,20,22} and are based on the assumption that the same mixing parameter α in HSE06 is appropriate in bulk as well as in few-layer systems. Of particular interest is our finding that the band gap depends sensitively on the number of layers N in a few-layer slab, as shown in Figure 1e. We find that E_g scales as the inverse number of layers and changes significantly between 1.0 eV in a single layer and 0.3 eV in the bulk, indicating the possibility to tune the electronic properties of this system. Equally interesting is the sensitive dependence of the gap on in-layer strain along different directions, shown in Figure 1f. Of particular importance is our finding that a moderate in-plane compression of $\approx 5\%$

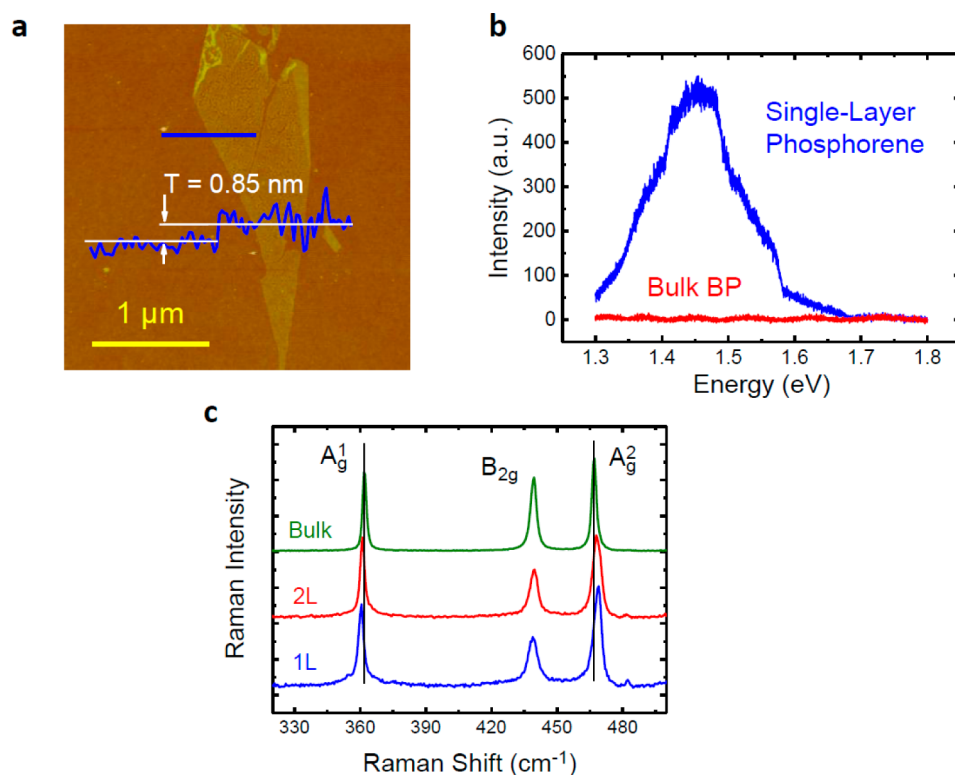


Figure 2. Material characterizations of single-layer and few-layer phosphorene. (a) Atomic force microscopy image of a single-layer phosphorene crystal with the measured thickness of ≈ 0.85 nm. (b) Photoluminescence spectra for single-layer phosphorene and bulk black phosphorus samples on a 300 nm SiO_2/Si substrate, showing a pronounced PL signal around 1.45 eV. To prevent the single-layer phosphorene reacting with the environment, it is covered by PMMA layer during experiments. (c) Raman spectra of single-layer and bilayer phosphorene and bulk black phosphorus films.

or more, possibly caused by epitaxial mismatch with a substrate, will change phosphorene from a direct-gap to an indirect-gap semiconductor with a significantly smaller gap. Details of the computational approach are listed in the Experimental Methods section and in the Supporting Information.

Atomically thin single-layer or few-layer phosphorene was achieved *via* mechanical exfoliation of commercially available (Smart-elements) bulk black phosphorus. A 300 nm SiO_2 -coated silicon wafer was used as the substrate. Figure 2a shows the atomic force microscopy (AFM) image of an exfoliated single-layer phosphorene crystal. A step height of ~ 0.85 nm measured at the crystal edge confirms the presence of single-layer phosphorene. Even though the step height is slightly larger than the theoretical value of 0.6 nm for single-layer phosphorene, we generally expect that the AFM-measured thickness value of a single-layer 2D crystal on SiO_2/Si substrate is higher than the theoretical value; this is widely observed in graphene and MoS_2 cases.³³ Photoluminescence (PL) of exfoliated single-layer phosphorene is observed in the visible wavelengths as shown in Figure 2b. For 10 nm thick black phosphorus flakes, no PL signal is observed within the detection spectrum range because the expected band gap of bulk black phosphorus is as low as ~ 0.3 eV, falling in the infrared wave region. In contrast, a

pronounced PL signal centered at 1.45 eV with a ~ 100 meV narrow width is obtained on a single-layer phosphorene crystal. This observed PL peak is likely of excitonic nature and thus a lower bound on the fundamental band gap value. The measured value of 1.45 eV indirectly confirms that the band gap in the monolayer is significantly larger than in the bulk. Further studies are required to properly interpret the PL spectra, which depend on the density of states, frequency-dependent quantum yield, the substrate, and the dielectric environment. We conclude that the predicted increased band gap value in single-layer phosphorene, caused by the absence of interlayer hybridization near the top of the valence and bottom of the conduction band, is consistent with the observed photoluminescence signal. The expected position of the PL peak for bilayer phosphorene is outside our spectral detection range. Still, we believe to have achieved few-layer phosphorene, as confirmed by Raman spectroscopy. Our Raman spectra of single-layer, bilayer, and bulk black phosphorus are presented in Figure 2c. The Raman spectra show a well-defined thickness dependence, with the A_g^1 and A_g^2 modes shifting toward each other in frequency when the thickness is increased, similar to what has been observed in MoS_2 .³⁴

Although single-layer or bilayer phosphorene can be physically realized by exfoliation, it is more sensitive to

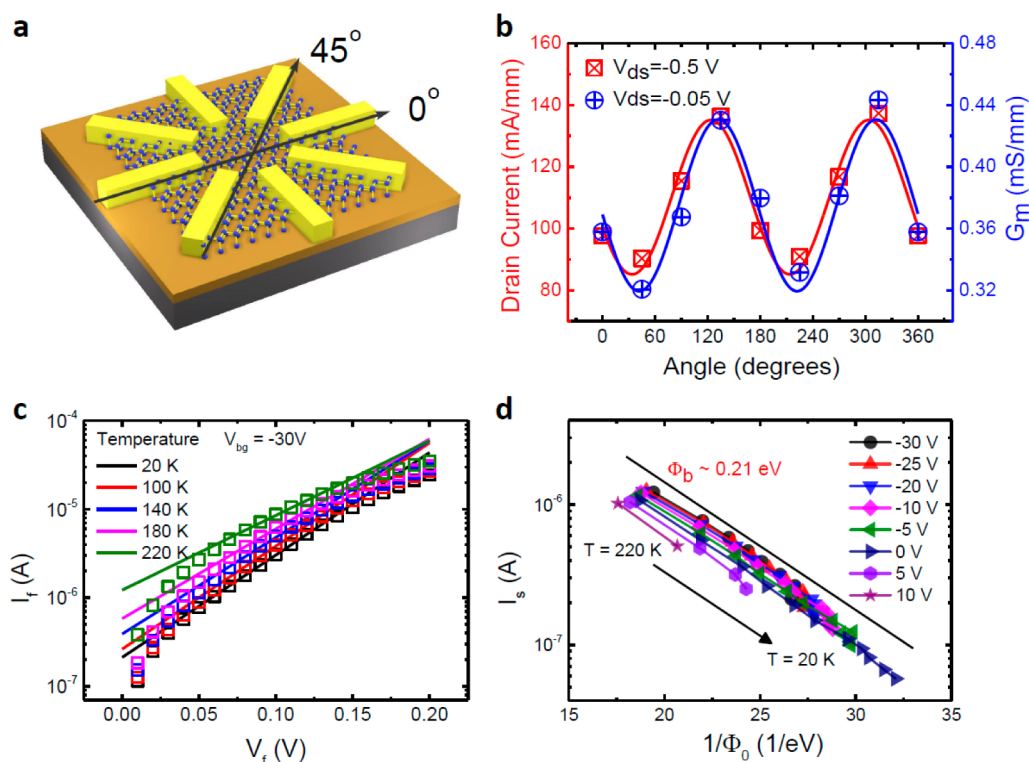


Figure 3. Transport properties of phosphorene. (a) Device structure used to determine the angle-dependent transport behavior. Zero degree is defined by the electrodes, not few-layer phosphorene crystal orientation. (b) Angular dependence of the drain current and the transconductance G_m of a device with a film thickness of ~ 10 nm. The solid red and blue curves are fitted by the directional dependence of low-field conductivity in anisotropic material with minimum and maximum conductivity times sine and cosine square of the angle. (c) Forward bias I_f – V_f characteristics of the Ti/black phosphorus junction. (d) Logarithmic plot of the characteristic current I_s as a function of the reciprocal characteristic energy Φ_0 , based on data from (c), which is used to determine the Schottky barrier height Φ_b .

the environment compared to graphene or MoS_2 . All attempts to study transport properties or device performance on phosphorene films less than ~ 2 nm thick were not successful. Since single-layer phosphorene is one atomic layer thick, it should be more stable and display a lower defect density than transition metal dichalcogenides such as MoS_2 . The processes to significantly reduce the defect density in back phosphorus and phosphorene films and to passivate the defects and surfaces need to be further developed. We focus on few-layer phosphorene thicker than 2 nm in the following transport and device experiments.

Anisotropic transport behavior along different directions is a unique property for few-layer phosphorene. A black phosphorus crystal with the thickness of ~ 10 nm was peeled and transferred onto a 90 nm SiO_2 -capped Si substrate. Metal contacts were symmetrically defined around the crystal with 45° as the angular increment of the orientation, as shown in Figure 3a. We fabricated $1 \mu\text{m}$ wide 20/60 nm thick Ti/Au contacts to few-layer phosphorene so that the spacing between all opposite bars was $5 \mu\text{m}$. We used the four pairs of diametrically opposite bars as source/drain contacts for a transistor geometry and measured the transistor behavior for each of these devices. The maximum drain current at 30 V back gate bias and 0.5 V

drain bias, which we display in Figure 3b as a function of the orientation of the contact pair, shows clearly an angle-dependent transport behavior. The anisotropic behavior of the maximum drain current is roughly sinusoidal, characterized by the minimum value of ≈ 85 mA/mm at 45° and 225° , and the maximum value of ≈ 137 mA/mm at 135° and 315° . In spite of the limited 45° angular resolution, the observed 50% anisotropy between two orthogonal directions is significant. The same periodic trend can be found in the maximum value of the transconductance, which could be partially related to a mobility variation in the x – y plane of few-layer phosphorene. This large mobility variation is rarely seen in other conventional semiconductors. It could be partially related to the uniquely ridged structure in the 2D plane of few-layer phosphorene, seen in Figure 1a–c, suggesting a different transport behavior along or normal to the ridges. On the basis of the band dispersion plotted in Figure 1d, we find that perpendicular to the ridges, corresponding to the Γ – Y direction, the effective mass of electrons and holes $m_e \approx m_h \approx 0.3 m_0$ is a fraction of the free electron mass m_0 . Parallel to the ridges, along the Γ – X direction, the carriers are significantly heavier, with the effective mass of holes amounting to $m_h \approx 8.3 m_0$ and that of electrons to $m_e \approx 2.6 m_0$, suggesting anisotropic transport behavior.

The observed anisotropy is less pronounced than the prediction because the angle resolution is as large as 45 °C and the fringe current flow in the real device averages out partly the anisotropy.

In order to investigate the nature of the metal/phosphorene junction, we used a three-terminal method, similar to the Kelvin probe, to measure the forward bias I – V characteristics of the Ti/phosphorene metal/semiconductor junction³⁵ at the constant back gate voltage $V_{bg} = -30$ V and display our results in Figure 3c. Current was passed between two Ti/phosphorene contacts of a multi-terminal device with contacts around the perimeter of the phosphorene flake. Voltage was measured between the forward biased contact and a third contact adjacent to it with zero current flowing through the third contact. Under these conditions, the measured voltage difference is equal to the voltage across the forward biased Ti/phosphorene contact. These data show an exponential increase in the current I_f as the voltage V_f across the junction increases from 70 to 130 mV. In view of the degenerate doping of the phosphorene sample and the exponential I – V characteristics across this junction at temperatures as low as 20 K, we conclude that thermally assisted tunneling through the Schottky barrier is responsible for the transport through the junction. To determine the Schottky barrier height of the Ti/phosphorene contact, we fit the exponential I – V characteristics by the equation $I_f = I_s \exp(V_f/\Phi_0)$, where I_s is the characteristic current and Φ_0 the characteristic energy, which characterizes transport across the junction at a particular temperature. Fits of the semilogarithmic plots in a wide temperature range are shown in Figure 3c. The temperature-dependent characteristic current I_s can be furthermore viewed as proportional to $\exp(-\Phi_b/\Phi_0)$, where Φ_b is the height of the Schottky barrier at the metal–semiconductor junction and Φ_0 is a temperature-dependent quantity. This provides a way to use our temperature-dependent I – V measurements to determine Φ_b from the slope of the quantity $\log I_s$ as a function of $1/\Phi_0$. Figure 3d shows the corresponding plot, where each data point has been determined by fitting the I – V characteristic curve at a particular gate voltage and temperature. The slope of all curves shows an impressive independence of the measurement conditions, indicating the Schottky barrier height $\Phi_b \approx 0.21$ eV for holes at the Ti/phosphorene junction. We note that the barrier height determined here is the true Schottky barrier height at the metal/phosphorene junction, not an effective Schottky barrier height that is commonly determined for metal/semiconductor junctions *via* the activation energy method.¹¹

We proceed to fabricate transistors of this novel 2D material in order to examine its performance in actual devices. We employed the same approach to fabricate transistors with a channel length of 1.0 μm as in our previous transport study. We used few-layer

phosphorene with a thickness ranging from 2.1 to over 20 nm. The I – V characteristic of a typical 5 nm thick few-layer phosphorene field-effect transistor for back gate voltages ranging from +30 to –30 V, shown in Figure 4a, indicates a reduction of the total resistance with decreasing gate voltage, a clear signature of its p-type characteristics. Consequently, few-layer phosphorene is a welcome addition to the family of 2D semiconductor materials since most pristine TMDs are either n-type or ambipolar as a consequence of the energy level of S vacancy and charge-neutral level coinciding near the conduction band edge of these materials.^{11,14} In only a few cases, p-type transistors have been fabricated by externally doping 2D systems using gas adsorption, which is not easily practicable for solid-state device applications.^{4,36} The observed linear I – V relationship at low drain bias is indicative of good contact properties at the metal/phosphorene interface. We also observe good current saturation at high drain bias values, with the highest drain current of 194 mA/mm at 1.0 μm channel length at the back gate voltage $V_{bg} = -30$ V and drain voltage $V_{ds} = -2$ V. In Figure 4b, we present the transfer curves for drain bias values $V_{ds} = 0.01$ and 0.5 V, which indicate a current on/off ratio of $\sim 10^4$, a very reasonable value for a material with a bulk band gap of 0.3 eV. We also note that, according to Figure 1d, the band gap of few-layer phosphorene is widened significantly due to the absence of interlayer hybridization between states at the top of the valence and bottom of the conduction band.

Inspecting the transfer curves in Figure 4b, we find the maximum transconductance to range from $G_m = 45 \mu\text{S/mm}$ at $V_{ds} = 0.01$ V to 2.28 mS/mm at 0.5 V drain bias. Using simple square law theory, we can estimate the field-effect mobility μ_{FE} from $G_m = \mu_{FE} C_{ox}(W/L)V_{ds}$, where C_{ox} is the capacitance of the gate oxide, W and L are the channel width and length, and V_{ds} is the drain bias. Our results for $V_{ds} = 0.01$ V indicate a high field-effect mobility $\mu_{FE} = 286 \text{ m}^2/\text{V}\cdot\text{s}$ at room temperature, and our four-terminal measurements suggest a factor of 5 improvement at low temperatures (see the Supporting Information). These values are still smaller than those in bulk black phosphorus, where the electron and hole mobility is $\approx 1000 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature and could exceed $15\,000 \text{ cm}^2/\text{V}\cdot\text{s}$ for electrons and $50\,000 \text{ cm}^2/\text{V}\cdot\text{s}$ for holes at low temperatures.³⁷ We consider the following factors to cause the mobility reduction in few-layer phosphorene. (i) The exposed surface of few-layer phosphorene is chemically unstable. Chemisorbed species from the process and the environment change the electronic structure and scatter carriers, thus degrading the mobility. (ii) In a particular transistor, the current flow may not match the direction, where the material has the highest in-plane mobility. (iii) The Schottky barrier at the metal/phosphorene interface induces a large contact resistance within the undoped source/drain regions.

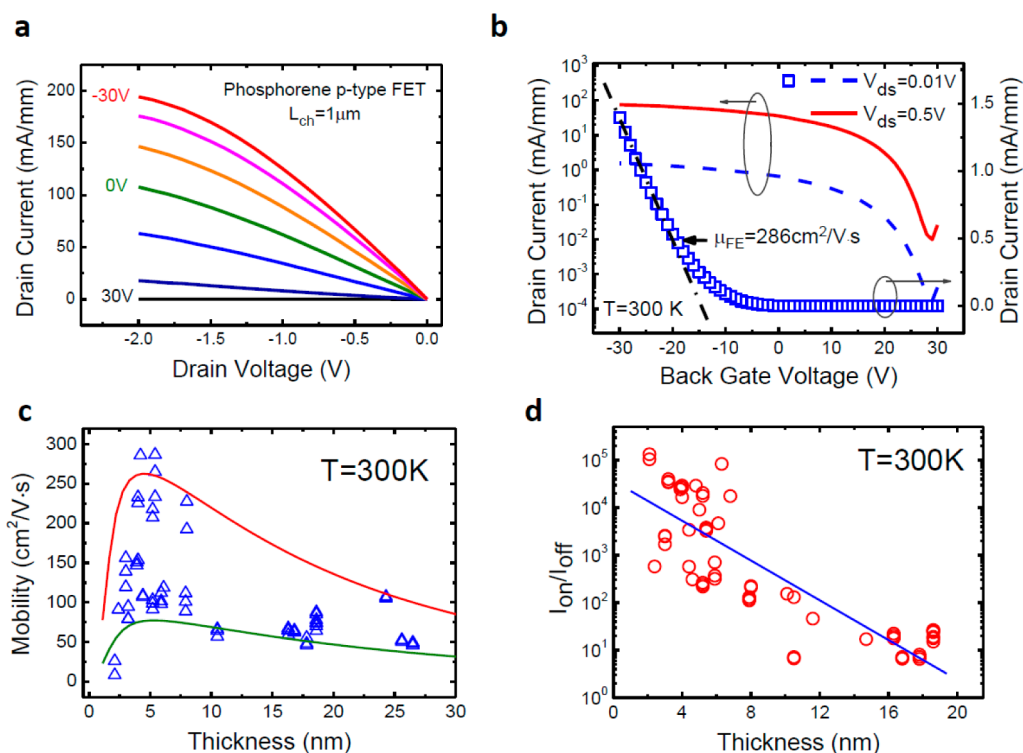


Figure 4. Device performance of p-type transistors based on few-layer phosphorene. Output (a) and transfer (b) curves of a typical few-layer phosphorene transistor with a film thickness of ~ 5 nm. The arrow directions are also back gate bias sweeping directions. (c) Mobility summary of few-layer phosphorene and black phosphorus thin film transistors with varying thicknesses. Red and green lines are models after ref 14 with light and heavy hole masses for phosphorene, respectively. (d) Current on/off ratio summary of few-layer phosphorene and black phosphorus thin film transistors with varying thicknesses.

We expect that the real mobility of few-layer phosphorene should increase significantly upon appropriate surface passivation and in a high- k dielectric environment.³⁸

We further compare field-effect mobility in few-layer phosphorene transistors with various crystal thicknesses. Field-effect mobilities extracted from devices fabricated on phosphorene crystals with various thicknesses are displayed in Figure 4c. Similar to previous studies on MoS_2 transistors, the field-effect mobility shows a strong thickness dependence. It peaks at around 5 nm and decreases gradually with further increase of crystal thickness. Such trend can be modeled with screening and interlayer coupling in layered materials, as proposed in several previous studies.¹⁴ A more dispersive mobility distribution is observed for few-layer phosphorene transistors. This is due to the fact of anisotropic mobility in few-layer phosphorene or black phosphorus as discussed in previous parts and the random selection of crystal orientation in device fabrication. Thus carrier transports along at any directions between the two orthogonal ones in the x – y plane. Therefore, two curves are modeled for phosphorene transistors, as shown in Figure 4c, where the red and green curves show the fittings with mobility peak and valley, respectively. The current on/off ratio is shown in Figure 4d. It shows a general decreasing trend with increasing crystal thickness, steeply dropping

from $\sim 10^5$ for a 2 nm crystal to less than 10 once the crystal thickness exceeds 15 nm. This suggests the importance of crystal thickness selection of phosphorene transistors from the point of view of device applications. Transistors on a 4–6 nm crystal display the best trade-off with higher hole mobility and better switching behavior.

Finally, we demonstrate a CMOS logic circuit containing 2D crystals of pure few-layer phosphorene as one of the channel materials. Since phosphorene shows well-behaved p-type transistor characteristics, it can complement well n-type MoS_2 transistors. Here we demonstrate the simplest CMOS circuit element, an inverter, by using MoS_2 for the n-type transistor and phosphorene for the p-type transistor, both integrated on the same Si/SiO₂ substrate. Few-layer MoS_2 and phosphorene flakes were transferred onto the same substrate successively by the scotch tape technique. Source/drain regions were defined by e-beam lithography, similar to the PMOS fabrication described above. We chose different channel lengths of 0.5 μm for MoS_2 and 1 μm for phosphorene transistors to compensate for the mobility difference between MoS_2 and phosphorene by modifying the width/length ratio for NMOS and PMOS. Ti/Au of 20/60 nm was used for both MoS_2 and phosphorene contacts. Prior to top growth of a high- k dielectric, a 1 nm Al layer was deposited on the sample by e-beam evaporation.

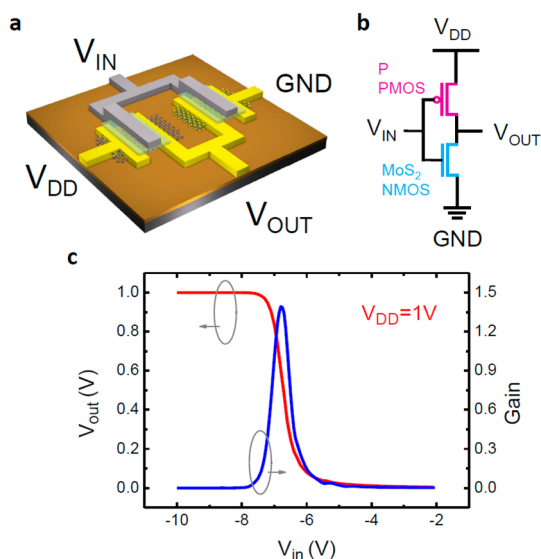


Figure 5. CMOS logic with 2D crystals. (a) Schematic view of the CMOS inverter, with ~ 5 nm MoS_2 serving as the NMOS and ~ 5 nm few-layer phosphorene serving as the PMOS. (b) Circuit configuration of the CMOS inverter. (c) Voltage transfer curve $V_{\text{out}}(V_{\text{in}})$ and gain of the 2D CMOS inverter.

The Al layer was oxidized in ambient conditions to serve as the seeding layer. A 20 nm Al_2O_3 grown by atomic layer deposition (ALD) at 250 °C was used as the top gate dielectric. Finally, 20/60 nm Ti/Au was used for the top gate metal electrode and interconnects between the transistors. The final device structure is shown in Figure 5a and the corresponding circuit configuration in Figure 5b. In our CMOS inverter, the power supply at voltage V_{DD} is connected to the drain electrode of the phosphorene PMOS. The PMOS source and the NMOS drain are connected and provide the output voltage signal V_{OUT} . The NMOS source is connected to the ground (GND). Both top gates of the NMOS and the PMOS are connected to the source of the input voltage V_{IN} . The voltage transfer characteristics (VTC) are shown in Figure 4c. The power supply voltage was set to be 1 V. Within the input voltage

range from -10 to -2 V, the output voltage shows a clear transition from V_{DD} to 0. A maximum gain of ~ 1.4 is achieved. Due to the generally large contact resistance exhibited in 2D materials and less obvious current saturation for Schottky barrier transistors, much more work is needed to improve the gain and move the 2D CMOS circuit research forward.

CONCLUSIONS

In summary, we have investigated the optical and electrical properties and potential device applications of exfoliated single- and few-layer phosphorene films as a new p-type semiconducting 2D material with high hole mobility. We used *ab initio* calculations to determine the equilibrium structure and the interlayer interaction of bulk black phosphorus as well as few-layer phosphorene with 1–4 layers. Our theoretical results indicate that the band gap is direct, depends on the number of layers and the in-layer strain, and is significantly larger than the bulk value of 0.31–0.36 eV. We have successfully achieved a single-layer phosphorene film. The observed photoluminescence peak in the visible wavelength from single-layer phosphorene indirectly confirms the widening of the band gap as predicted by theory. We find substantial anisotropy in the transport behavior of this 2D material, which we associate with the unique ridge structure of the layers. The overall device behavior can be explained by considering a Schottky barrier height of 0.21 eV for hole tunneling at the junctions between phosphorene and Ti metal contacts. We report fabrication of p-type transistors of few-layer phosphorene with a high on-current of 194 mA/mm at 1.0 μm channel length, a current on/off ratio over 10^4 , and a high field-effect mobility up to 286 $\text{cm}^2/\text{V}\cdot\text{s}$ at room temperature. We have also constructed a CMOS inverter by combining a phosphorene PMOS transistor with a MoS_2 NMOS transistor, thus achieving heterogeneous integration of semiconducting phosphorene crystals as a novel channel material for future electronic applications.

EXPERIMENTAL METHODS

All optical measurements are carried out in ambient atmosphere at room temperature using a microscope coupled to a grating spectrometer with a CCD camera. Optical beams are focused on the sample with a spot diameter of $\sim 1 \mu\text{m}^2$. For the PL study, the samples are excited with a frequency-doubled Nd:YAG laser at a wavelength of 532 nm, and the CCD camera senses photons in the spectrum range between 1.3 and 2.0 eV.

Scotch-tape-based microcleavage of the layered bulk black phosphorus and MoS_2 crystals is used for fabrication of all 2D devices containing phosphorene or MoS_2 layers, followed by transfer onto the Si/SiO₂ substrate, as previously described in graphene studies. Bulk crystals were purchased from Smart-elements (black phosphorus) and SPI Supplies (MoS_2). Degenerately doped silicon wafers (0.01–0.02 $\Omega\cdot\text{cm}$) capped with 90 nm SiO₂ were purchased from SQI (Silicon Quest International). After few-layer crystals of phosphorene and/or

MoS_2 were transferred onto the substrate, all samples were sequentially cleaned by acetone, methanol, and isopropyl alcohol to remove any scotch tape residue. This procedure has been followed by a 180 °C postbake process to remove solvent residue. The thickness of the crystals was determined by a Veeco Dimension 3100 atomic force microscope. E-beam lithography has been carried out using a Vistec VB6 instrument. The 20/60 nm Ti/Au contacts were deposited using the e-beam evaporator at a rate of 1 $\text{\AA}/\text{s}$ to define contact electrodes and metal gates. No annealing has been performed after the deposition of the metal contacts. The top gate dielectric material was deposited by an ASM F-120 ALD system at 250 °C, using trimethylaluminum (TMA) and H₂O as precursors. The pulse time was 0.8 s for TMA and 1.2 s for water, and the purge time was 5 s for both.

Theoretical Methods. Our computational approach to determine the equilibrium structure, stability, and electronic properties of black phosphorus is based on *ab initio* density functional

theory (DFT) as implemented in the SIESTA³⁰ and VASP³¹ codes. We used periodic boundary conditions throughout the study, with multilayer structures represented by a periodic array of slabs separated by a 15 Å thick vacuum region. We used the Perdew–Burke–Ernzerhof²⁸ exchange–correlation functional, norm-conserving Troullier–Martins pseudopotentials,³⁹ and a double- ζ basis including polarization orbitals. The reciprocal space was sampled by a fine grid⁴⁰ of $8 \times 8 \times 1$ k-points in the Brillouin zone of the primitive unit cell. We used a mesh cutoff energy of 180 Ry to determine the self-consistent charge density, which provided us with a precision in total energy of less than 2 meV/atom. All geometries have been optimized by SIESTA using the conjugate gradient method,⁴¹ until none of the residual Hellmann–Feynman forces exceeded 10^{-2} eV/Å. Our SIESTA results for the optimized geometry, interlayer interactions, and electronic structure were found to be in general agreement with VASP calculations. The electronic band structure of bulk and multilayer black phosphorus was determined using the HSE06 hybrid functional,²⁹ as implemented in VASP, with the mixing parameter $\alpha = 0.04$.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Details of *ab initio* calculations, temperature-dependent carrier mobility, determination of field-effect mobility, and discussions on the Schottky barriers in phosphorene transistors are shown in Supporting Information. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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