Ferroelectric Field-Effect Transistors Based on MoS$_2$ and CuInP$_2$S$_6$ Two-Dimensional van der Waals Heterostructure

Mengwei Si, Pai-Ying Liao, Gang Qiu, Yuqin Duan, and Peide D. Ye$^{*}$

School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States

Supporting Information

**ABSTRACT:** We demonstrate room-temperature ferroelectric field-effect transistors (Fe-FETs) with MoS$_2$ and CuInP$_2$S$_6$ two-dimensional (2D) van der Waals heterostructure. The ferroelectric CuInP$_2$S$_6$ is a 2D ferroelectric insulator, integrated on top of MoS$_2$ channel providing a 2D/2D semiconductor/insulator interface without dangling bonds. The MoS$_2$- and CuInP$_2$S$_6$-based 2D van der Waals heterostructure Fe-FETs exhibit a clear counterclockwise hysteresis loop in transfer characteristics, demonstrating their ferroelectric properties. This stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS$_2$ transistors because of the tuning of capacitance matching between the MoS$_2$ channel and the ferroelectric CuInP$_2$S$_6$, leading to the enhancement of the on/off current ratio. Meanwhile, the CuInP$_2$S$_6$ thin film also shows resistive switching characteristics with more than four orders of on/off ratio between low- and high-resistance states, which is also promising for resistive random-access memory applications.

**KEYWORDS:** MoS$_2$, CuInP$_2$S$_6$, 2D heterostructure, ferroelectric, field-effect transistors, resistive switching

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Two-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have been extensively explored as channel materials for future electronic device applications because their atomically thin channels offer ideal electrostatic control to enhance the immunity to short channel effects. Molybdenum disulfide (MoS$_2$) has been widely studied in recent years as a promising channel material because of its ambient stability, appropriate band gap, and moderate mobility. Inserting a ferroelectric insulator (such as hafnium zirconium oxide and lead zirconate titanate) into the gate stack of a metal-oxide-semiconductor field-effect transistor (MOSFET) as a ferroelectric field-effect transistor (Fe-FET) and negative capacitance field-effect transistor (NC-FET) has been widely studied for nonvolatile memory and low-power logic applications. The integration of 2D ferroelectric materials together with 2D semiconductors as 2D ferroelectric insulator/2D semiconductor interfaces without dangling bonds is very promising for nonvolatile memory, variability, and reliability. The lack of dangling bonds on the surface of 2D materials also makes the atomic layer deposition (ALD) process of ferroelectric insulators difficult. How to integrate an ALD ferroelectric insulator (i.e., hafnium zirconium oxide) as a top-gate dielectric on 2D materials remains a challenge. The integration of 2D ferroelectric insulators together with 2D semiconductors as 2D van der Waals (vdW) heterostructures as 2D van der Waals (vdW) heterostructures can be a potential solution to eliminate the interface issue, reduce the interface trap density, and achieve high-performance Fe-FETs. However, 2D ferroelectric material is rather rare because ferroelectricity tends to disappear on very thin films and requires breaking of the structural centrosymmetry. A few 2D materials have been studied theoretically and experimentally that show ferroelectricity. The choice of a proper 2D ferroelectric insulator to integrate with 2D semiconductors is crucial because 2D vdW heterostructure Fe-FETs require a low leakage current gate insulator and room-temperature ferroelectricity for real device applications. Among these materials, CuInP$_2$S$_6$ (CIPS) has been recently explored as a room-temperature 2D ferroelectric material with switchable polarization down to $\approx$4 nm and low leakage current, which can be a promising candidate for 2D vdW heterostructure Fe-FETs.

In this work, we synthesize the bulk CIPS crystal and examine the ferroelectricity of the 2D CIPS thin film by...
electrical polarization–voltage ($P−V$) measurement. We demonstrate MoS$_2$/CIPS 2D vdW heterostructure Fe-FETs at room temperature. The ferroelectric CIPS is integrated on top of the MoS$_2$ channel as a ferroelectric insulator, which offers a 2D/2D semiconductor/insulator interface. The MoS$_2$/CIPS 2D vdW heterostructure Fe-FETs exhibit a clear
counterclockwise hysteresis loop in transfer characteristics, demonstrating their ferroelectric properties. Meanwhile, this stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS2 transistors because of the tuning of capacitance matching between the MoS2 channel and the ferroelectric CuInP2S6 which leads to the enhancement of the on/off current ratio. Meanwhile, the resistive switching characteristics of CIPS are also studied, and more than four orders of on/off ratio between low- and high-resistance states are realized.

RESULTS AND DISCUSSION

The schematic view of a MoS2/CIPS 2D heterostructure Fe-FET is shown in Figure 1a. The device consists of few-layer MoS2 as the channel material, a few hundred nanometer CIPS as the ferroelectric gate insulator for a top-gate Fe-FET, a 300 nm SiO2 as the back-gate insulator, and heavily doped silicon substrate as the back-gate electrode. The device has a dual-gate structure, in which the MoS2 channel can be controlled by both top-gate and back-gate. A top-view false-color scanning electron microscopy (SEM) image of several fabricated devices with different channel lengths (Lch) is shown in Figure 1b, capturing Ni/Au top-gate electrodes, Ni source/drain electrodes, CIPS ferroelectric gate insulators, and MoS2 channels. The detailed fabrication process is shown in Figure 2, and detailed information can be found in the Methods section.

Figure 3a illustrates the Raman spectrum of an exfoliated CIPS thin film at room temperature, showing the same ferroelectric phase.33 Cation (CuI, InIII) and anion (P2S6−) vibrations are responsible for peaks in the 50–80, 90–140, and 300–320 cm−1 ranges. Multiple peaks between 140 and 290 cm−1 are caused by S–P–P and S–P–S modes, and the peak at 380 cm−1 corresponds to P–P stretching. The 410–460 cm−1 peaks correspond to P–S oscillations. Figure 3b shows the energy-dispersive spectroscopy (EDS) spectrum of the exfoliated CIPS thin film. The atomic percent (atom %) of S, P, Cu, and In is 59.9, 20.3, 10.3, and 9.6, respectively. EDS analysis shows near perfect CuInP2S6 stoichiometry. The CIPS thin film samples used in Raman and EDS measurement were mechanically exfoliated from a bulk CIPS crystal (the synthesis of the bulk CIPS crystal is discussed in Supporting Information section 1) onto a silicon substrate with 300 nm thermally grown SiO2. The atomic structure illustration of CIPS is shown in Supporting Information section 2. It contains an ABC sulfur stacking filled by Cu, In, and P–P pair. The noncentrosymmetric structure leads to spontaneous polarization and ferroelectricity at temperatures below the Curie point.31 To study the ferroelectric properties of the CIPS thin film, metal–insulator–metal (MIM, Ni/CIPS/Ni) capacitors are fabricated as a test structure. The P–V characteristics are measured from 290 to 330 K. Figure 3c shows the P–V measurement at 290 K on a CIPS MIM capacitor with a CIPS thickness (tCIPS) of ~0.6 μm. The P–V characteristic of CIPS shows a clear ferroelectric hysteresis loop with 3.2 μC/cm2 remnant polarization (Pr) and 8.9 × 10−3 V/nm coercive field (Ec). Note that the success in P–V measurement of the CIPS MIM capacitor suggests that the leakage current through CIPS is sufficiently low, which indicates CIPS can be a good candidate as a ferroelectric gate insulator for Fe-FETs and NC-FETs. Figure 3d shows the temperature-dependent remnant polarization of CIPS extracted from the P–V measurement of the same device as in Figure 3c from 290 to 330 K. The Pr of

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characteristics have minor changes of top-gate or bottom-gate back-gate bias can be used to modulate the on/off floating, showing the two gates’ capacitance coupling has a minor effect on each other. Figure 4c shows the $I_D-V_{GS}$ characteristics measured using the bottom-gate (0.4 μm CIPS as gate insulator) at $V_D$ = 0.1 V with different $V_{BG}$ from −5 to 5 V. The ferroelectric hysteresis loop in the $I_D-V_{GS}$ characteristics is found to be modulated by the back-gate bias, as shown in Figure 4c. With more negative $V_{BG}$ a larger hysteresis loop can be observed, which suggests that back-gate bias can be used to modulate the on/off current ratio of the MoS2/CIPS 2D vdW heterostructure Fe-FETs for better memory performance. The origin of the modulation of the ferroelectric hysteresis loop comes from the capacitance matching between the capacitance of CIPS ($C_{FE}$) and the semiconductor capacitance ($C_S$) of the MoS2 channel. For a ferroelectric-gated FET, it is already known that because of the negative capacitance effect of the ferroelectric material, if $|C_{FE}|<C_S$, the ferroelectric-gated FET is a Fe-FET with hysteresis, whereas if $|C_{FE}|>C_S$, the ferroelectric-gated FET is a NC-FET without hysteresis if parasitic capacitance is negligible. A detailed analysis on the value of $|C_{FE}|$ and $C_S$ is discussed in Supporting Information section 4.

Figure 4 shows the electrical characterization of a MoS2/CIPS 2D vdW heterostructure Fe-FET at room temperature. The device has a channel length of 1 μm and channel width of 2.1 μm. The thickness of the MoS2 flake ($T_{fl}$) is about 7 nm, and the thickness of CIPS thin film is about 0.4 μm. Figure 4a shows the $I_D-V_{GS}$ characteristics measured using the top-gate (0.4 μm CIPS as ferroelectric gate insulator) with the back-gate floating at top-gate voltage ($V_{TG}$) from −5 to 5 V and at drain-to-source voltage ($V_{DS}$) from 0.1 to 0.9 V. The gate leakage current is smaller than drain current at all different gate voltages, so that the leakage current through CIPS does not have impact on the $I_D-V_{GS}$ characteristics. The simultaneously measured gate leakage current can be found in Supporting Information section 3. The transfer characteristics show a clear ferroelectric hysteresis loop (counterclockwise) at all $V_{DS}$. A larger on/off ratio between the low- and high-resistance state can be observed at lower $V_{DS}$. Figure 4b shows the $I_D-V_{GS}$ characteristics measured using the back-gate (300 nm SiO2 as gate insulator) with the top-gate floating at back-gate voltage ($V_{BG}$) from −5 to 5 V and at $V_{DS}$ from 0.1 to 0.9 V. The transfer characteristics show a clockwise hysteresis loop, which is common in MoS2 MOSFETs and is induced by charge trapping at the SiO2/MoS2 interface and in bulk SiO2. The characteristics have minor changes of top-gate or bottom-gate being grounded instead of floating, showing the two gates’ capacitance coupling has a minor effect on each other. Figure 4c shows the $I_D-V_{GS}$ characteristics measured using the bottom-gate (0.4 μm CIPS as gate insulator) at $V_D$ = 0.1 V with different $V_{BG}$ from −5 to 5 V. The ferroelectric hysteresis loop in the $I_D-V_{GS}$ characteristics is found to be modulated by the back-gate bias, as shown in Figure 4c. With more negative $V_{BG}$ a larger hysteresis loop can be observed, which suggests that back-gate bias can be used to modulate the on/off current ratio of the MoS2/CIPS 2D vdW heterostructure Fe-FETs for better memory performance. The origin of the modulation of the ferroelectric hysteresis loop comes from the capacitance matching between the capacitance of CIPS ($C_{FE}$) and the semiconductor capacitance ($C_S$) of the MoS2 channel. For a ferroelectric-gated FET, it is already known that because of the negative capacitance effect of the ferroelectric material, if $|C_{FE}|<C_S$, the ferroelectric-gated FET is a Fe-FET with hysteresis, whereas if $|C_{FE}|>C_S$, the ferroelectric-gated FET is a NC-FET without hysteresis if parasitic capacitance is negligible. A detailed analysis on the value of $|C_{FE}|$ and $C_S$ is discussed in Supporting Information section 4. Therefore, as the back-gate voltage can affect the electrostatics in the MoS2 channel and also tune the $C_S$, the back-gate bias can modulate the capacitance matching between $C_{FE}$ and $C_S$, so that the ferroelectric hysteresis loop can be modulated. It also indicates that this dual-gate structure enables the electrically controllable reconfiguration of the devices as either logic devices or memory devices by applying proper back-gate voltage. Figure 4d shows the $I_D-V_{GS}$ characteristics measured using the same $V_{BG}$ and $V_{DS}$ as $V_D$ from 0.1 to 0.9 V, which is simply the result of impact from both gates.

Except for the ferroelectricity in the CIPS thin film and its applications in Fe-FETs, the CIPS with a MIM capacitor structure also shows resistive switching characteristics which can be used in nonvolatile resistive random-access memory (ReRAM) applications, as shown in the Figure 5. Figure 5a illustrates the $I-V$ measurement process on the MIM capacitors. The voltage across the capacitor was first swept from 0 V to a positive maximum voltage ($V_{Max}$) then to a negative $-V_{Max}$ and then back to 0 V. Figure 5b shows the $I-V$ characteristics with different gate voltage sweep ranges ($V_{Max}$ from 4 to 7 V) of a CIPS MIM capacitor with $T_{FE}$ = 0.26 μm, measured at room temperature, showing ferroelectric resistive switching with more than four orders of on/off ratio between low- and high-resistance states. The resistive switching between the low- and high-resistance states originates from the ferroelectric polarization switching, which leads to the change of band alignment between metal and CIPS. The detailed band diagrams in different polarization states are discussed in Supporting Information section 7. The resistive switching characteristics of the CIPS are also affected by $V_{Max}$. A larger $V_{Max}$ leads to a smaller on-resistance but a larger voltage to reset to high-resistance state, as shown in Figure 5b, which can enable multiple design rooms. These results suggest that CIPS is a promising 2D material for nonvolatile ReRAM applications also.

CONCLUSION

In summary, MoS2/CIPS 2D vdW heterostructure Fe-FETs at room temperature are demonstrated. The ferroelectric CIPS is integrated on top of the MoS2 channel as a ferroelectric
insulator, which offers a 2D/2D semiconductor/insulator interface. The MoS₂/CIPS 2D vdW heterostructure Fe-FETs exhibit a stable ferroelectric hysteresis loop in transfer characteristics. Meanwhile, this stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS₂ transistors because of the tuning of capacitance matching between the MoS₂ channel and the ferroelectric CuInP₂S₆, leading to the enhancement of the on/off current ratio. Meanwhile, the resistive switching characteristics of CIPS are also studied, with more than four orders of on/off ratio between low- and high-resistance states demonstrated.

METHODS

**CulnP₂S₆ Growth.** Single-crystal CIPS were grown by solid-state reaction based on previous works. The detailed growth process can be found in Supporting Information section 1.

**Device Fabrication.** MoS₂ was transferred onto a 300 nm SiO₂/Si substrate using Scotch tape exfoliation. Fifteen nanometer Ni was deposited by electron-beam evaporation, followed by a lift-off process as a MoS₂ back-gate transistor. The procedure to transfer CIPS on top of MoS₂ is based on a dry transfer process. CIPS was first mechanically exfoliated onto a polydimethylsiloxane (PDMS) substrate. Then the PDMS/CIPS film was stamped on top of the MoS₂ channel. The PDMS film was then removed mechanically because of the stronger adhesion between CIPS and the substrate. Another 40 nm Ni and 50 nm Au were then deposited by electron-beam evaporation and realized by a lift-off process.

**Device Characterization.** The thickness of the CIPS was measured using a Veeco Dimension 3100 atomic force microscope system. SEM and EDS analysis were done using a Hitachi S-4800 FE-SEM and an Oxford X-Max silicon drift detector. Electrical characterization was carried out with a Keysight B1500 system with a Cascade Summit probe station. P–V measurement was done using a Radiant RT66C ferroelectric tester. Raman measurements were carried out on a HORIBA LabRAM HR800 Raman spectrometer.

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**REFERENCES**


