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ARTICLE

Superconducting Field-Effect Transistors with Pd_xTe–Te Intimate Contacts

Chang Niu, Mingyi Wang, Zhuocheng Zhang, Gang Qiu, Yixiu Wang, Dongqi Zheng, Pai-Ying Liao, Wenzhuo Wu,* and Peide D. Ye*

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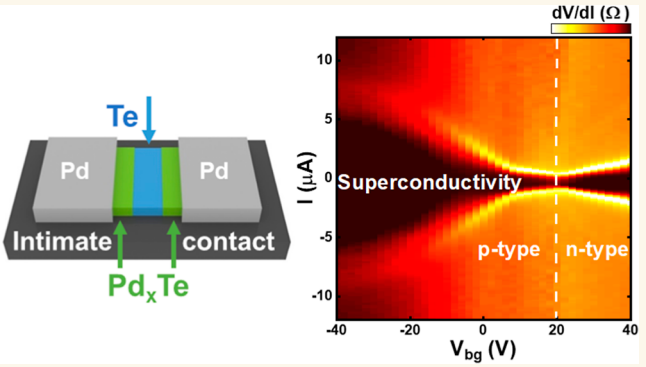
ABSTRACT: **Superconducting-based electronic devices have shown great potential for future quantum computing applications. One key building block device is a superconducting field-effect transistor based on a superconductor–semiconductor–superconductor Josephson-junction (JJ) with a gate-tunable semiconducting channel. However, the performance of such devices is highly dependent on the quality of the superconductor to semiconductor interface. In this study, we present an alternative method to obtain a high-quality interface by using intimate contact. We investigate the proximity-induced superconductivity in chiral crystal tellurium (Te) and fabricate a Pd_xTe–Te–Pd_xTe JJ with an ambipolar supercurrent that is gate-tunable and exhibits multiple Andreev reflections. The semiconducting two-dimensional Te single crystal is grown hydrothermally and partially converted to superconducting Pd_xTe by controlled annealing. Our work demonstrates a promising path for realizing controllable superconducting electronic devices with high-quality superconducting interfaces; thus, we can continue to advance the field of quantum computing and other interface-based technologies.**



KEYWORDS: *tellurium, superconductivity, interface, contact engineering, interdiffusion, Josephson-junction*

The study of interface physics between different materials has garnered significant attention in the fields of semiconductor device and condensed matter physics research. The heterogeneous integration of materials with varying band structures and properties has led to the development of numerous electronic devices with interesting and exotic physical phenomena. In addition to commonly studied electronic devices like heterojunction bipolar transistors[1] (semiconductor–semiconductor) and Schottky barrier diodes (metal–semiconductor), these heterostructure devices have also accelerated the discovery and study of phenomena such as quantum Hall and fractional quantum Hall effect,[2] quantum spin Hall effect,[3] and interface superconductivity.[4,5] As device sizes continue to shrink and the ratio of the interface (surface) area to bulk volume increases, the electrical transport properties originating from the interface (surface) become increasingly dominant. Consequently, a clean or high-quality interface is crucial for optimal device performance and the study of mesoscopic physics.

Of all the interfaces, the superconductor to semiconductor junction[6] has attracted extensive studies due to the prediction of hosting Majorana fermions[7,8] and the possible realization of topological quantum computation.[9,10] A Josephson-junction (JJ),[11,12] which is the building block of one type of quantum computers, is formed when two superconductors are coupled by weak-links or barriers. The weak-links or barriers can be an insulator, a nonsuperconducting metal, or a semiconductor. By utilizing the controllable chemical potential (carrier density) of a semiconductor, a superconducting field-effect transistor (Su-FET) can be realized in a planar superconductor–semiconductor–superconductor JJ with a gate. However, the tunneling of copper pairs in the junction is sensitive to the quality of the superconductor–semiconductor interface. Therefore, achieving a high-quality and transparent contact is crucial to effectively control the supercurrent and observe profound effects in these devices.

Tellurium (Te) is a chiral semiconductor with a narrow band gap of 0.32 eV. Spiral chains formed by covalently

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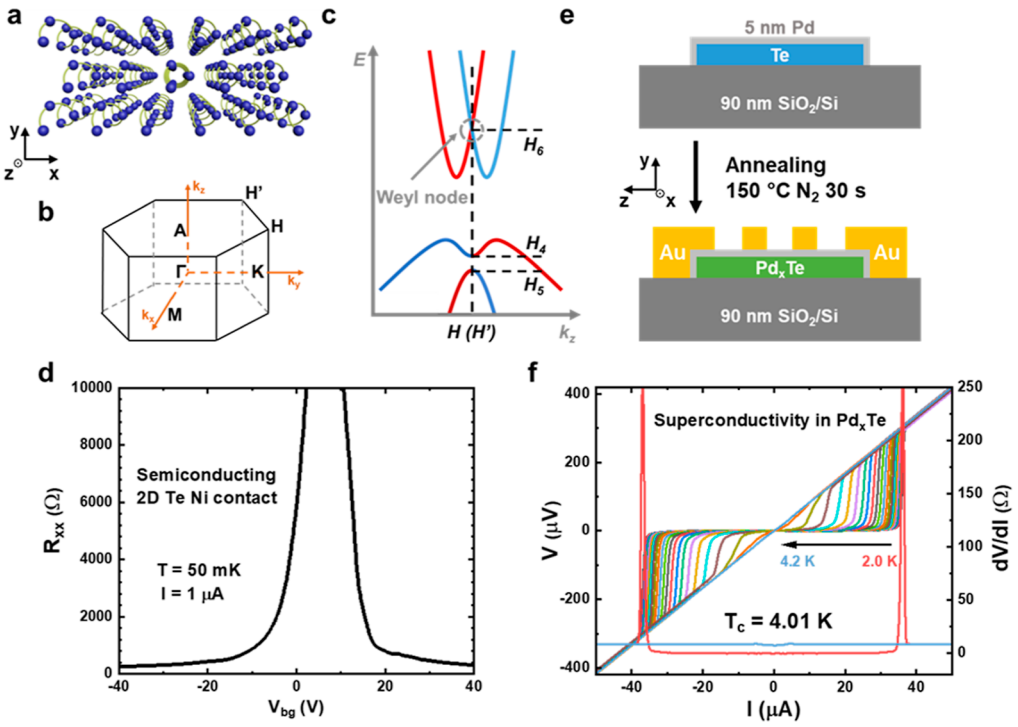

Figure 1. 2D Te and superconductivity in Pd_xTe. (a) Crystal structure of Te. (b) First Brillouin zone of Te. The conduction band minimum and the valence band maximum are located at H (H') points. (c) Electronic band structure of Te along the k_z direction around the H (H') point. Due to the strong spin−orbit interaction, the spin-splitting bands induce the Weyl node in the conduction band and the camelback structure in the valence band. (d) Ambipolar transport of Ni-contacted semiconducting 2D Te controlled by the gate voltage. (e) Schematic diagram of the Pd_xTe device. Superconducting Pd_xTe is formed after the electron beam evaporated 5 nm Pd/2D Te bilayer structure is annealed. (f) Current (I)-dependent voltage (V) and differential resistance (dV/dI) characterization of superconducting Pd_xTe under different temperatures.

bonded Te atoms are arranged in a trigonal lattice through van der Waals interaction, with the z-direction assigned to the three-fold screw axis and the x-direction assigned to the two-fold rotation axis Figure 1a. The first Brillouin zone of Te is shown in Figure 1b. The lowest unoccupied states and the highest occupied states are located at the H (H') point. A strong spin−orbit interaction[13] (high atomic number Z) and a chiral crystal structure (broken inversion symmetry) give rise to the exotic band structure (Figure 1c) of Te, including the camelback structure[14] (valence band) and the radial spin texture.[15−17] Two spin-splitting bands cross at the H (H') point and form a Weyl node in the conduction band.[15,18−20] The air-stable high-mobility hydrothermally grown two-dimensional tellurium[21] (2D Te) offers tunable carrier density and different carrier types for the investigation of quantum transport in Te.

In this paper, we demonstrated an innovative method to achieve a high-quality interface between a superconductor and a semiconductor by forming an intimate contact in the Pd−Te material system. By utilizing the diffusion of Pd atoms, an intimate contact is formed by converting a part of the semiconducting 2D Te single crystal to superconducting Pd_xTe. This intimate junction type can vastly reduce the interface impurity and lower the contact barrier between the superconductor and semiconductor. As a result, Pd_xTe−Te−Pd_xTe gate-tunable JJs are fabricated using a single-step lift-off process (see Methods), with the transition temperature and the chemical composition of Pd_xTe being easily controllable through the diffusion and annealing process. Notably, the observed multiple Andreev reflections (MARs) indicate that the contact is highly transparent. Our findings suggest that this method can be used for developing high-quality interfaces and gate-controlled superconducting electronic devices.

RESULTS AND DISCUSSION

Hydrothermally grown 2D Te flakes were carefully transferred onto a 90 nm SiO_2/Si substrate, which served as a back-gate. The flakes have an approximate thickness of 20 nm, and their electronic band structure closely resembles that of bulk Te. The probing current was sent along the chiral chain direction z. Figure 1d shows the typical electrical characterization (four-terminal resistance R_{xx} as a function of the gate voltage V_{bg}) of semiconducting 2D Te at a temperature of 50 mK, with Ni as the contact metal. The device manifests ambipolar behavior with the electron (hole) density controlled by the gate voltage V_{bg}, as shown in Figure S1. The 2D Te flakes are slightly p-doped at $V_{bg} = 0$ V. Figure 1e depicts a schematic diagram for the chemical transformation process from semiconducting 2D Te to superconducting Pd_xTe. A 5 nm thick layer of electron-beam-evaporated Pd is deposited on top of 2D Te as a palladium (Pd) source. After 30 s 150 °C annealing in a N_2 atmosphere using rapid thermal annealing (RTA), the converted Pd_xTe flakes were measured by the four-terminal method with gold electrodes. Superconductivity is observed and measured by the temperature-dependent $I−V$ characteristic and differential resistance (dV/dI) as a function of the dc current I in converted Pd_xTe flakes, as shown in Figure 1f. The gate voltage response within the ±40 V range was absent due to the high carrier density in superconducting Pd_xTe. The superconducting transition temperature in this device is

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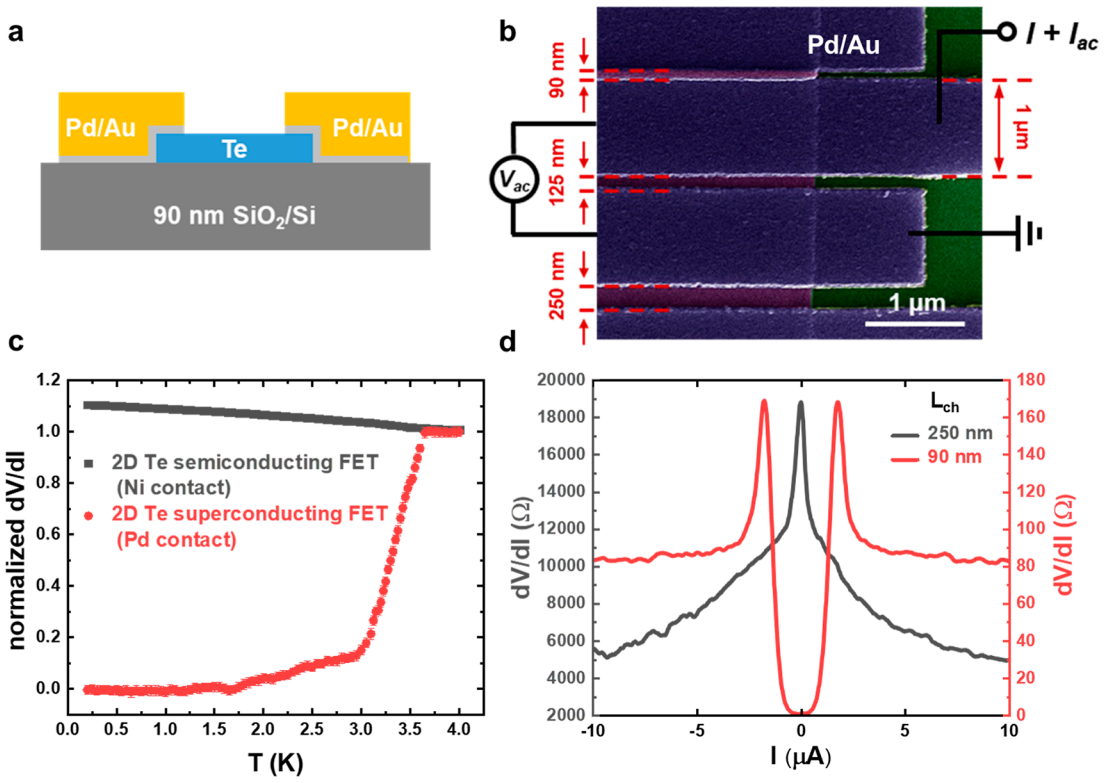

Figure 2. Proximity-induced superconductivity in intimate-contacted (Pd) 2D Te. (a) Device structure of intimate-contacted 2D Te. 5/50 nm Pd/Au is used as contact metal for 2D Te. (b) False colored SEM image of intimate-contacted 2D Te with three different channel lengths. The device is characterized using the two-terminal method by applying a dc current I and a small ac current I_{ac} at the same time. (c) Temperature-dependent normalized zero-bias differential resistance of semiconducting 2D Te (black) and proximity effect induced superconductivity 2D Te (red). (d) Differential resistance dV/dI as a function of dc current I in intimate-contacted 2D Te with the channel length of 250 nm (black) and 90 nm (red).

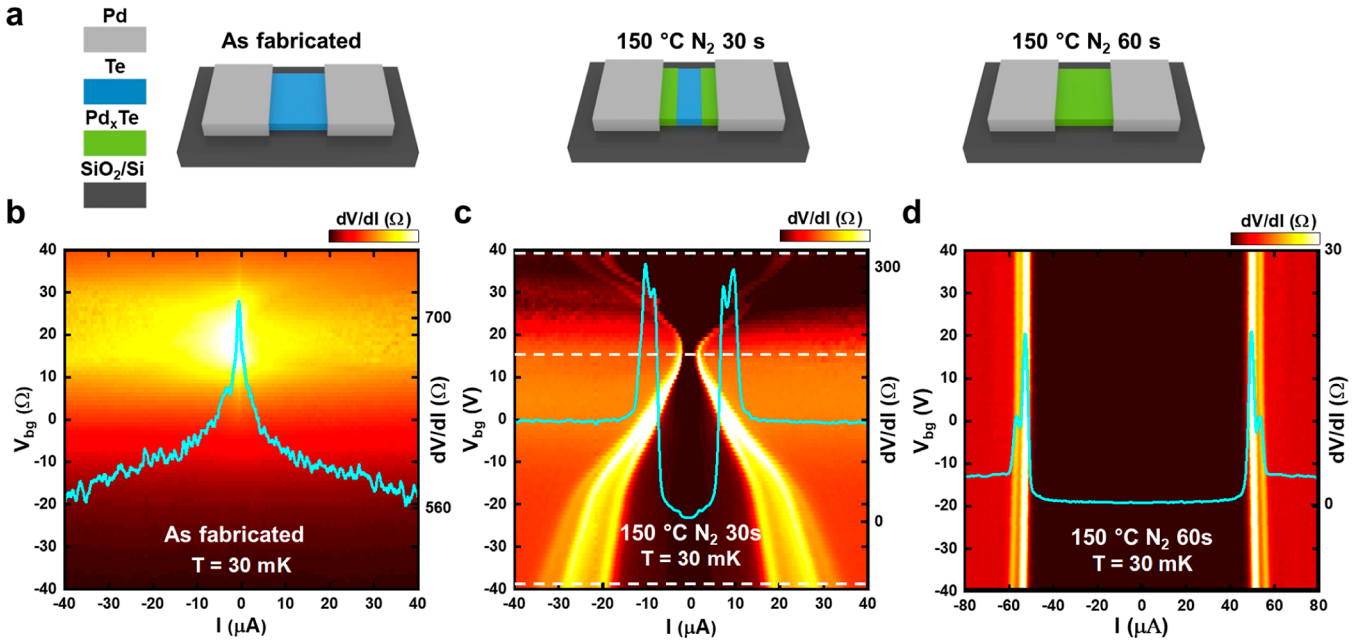

Figure 3. Controlling the diffusion of Pd atoms by RTA. (a) Cartoon schematic of the diffusion of Pd atoms in the intimate-contacted 2D Te device controlled by annealing time. (b–d) Color mapping of the differential resistance dV/dI as a function of the gate voltage V_{bg} and dc current I under different annealing conditions: (b) as fabricated, (c) 150 °C 30 s annealing in a N_2 atmosphere, and (d) 150 °C 60 s annealing in a N_2 atmosphere.

around 4 K. Note that pure Pd is not superconducting above 2 mK, while the Pd_xTe compound is a superconductor with transition temperature depending on the chemical composition x (1.8 K for x = 0.5 and 4.5 K for x = 1).[22,23] Additionally, the

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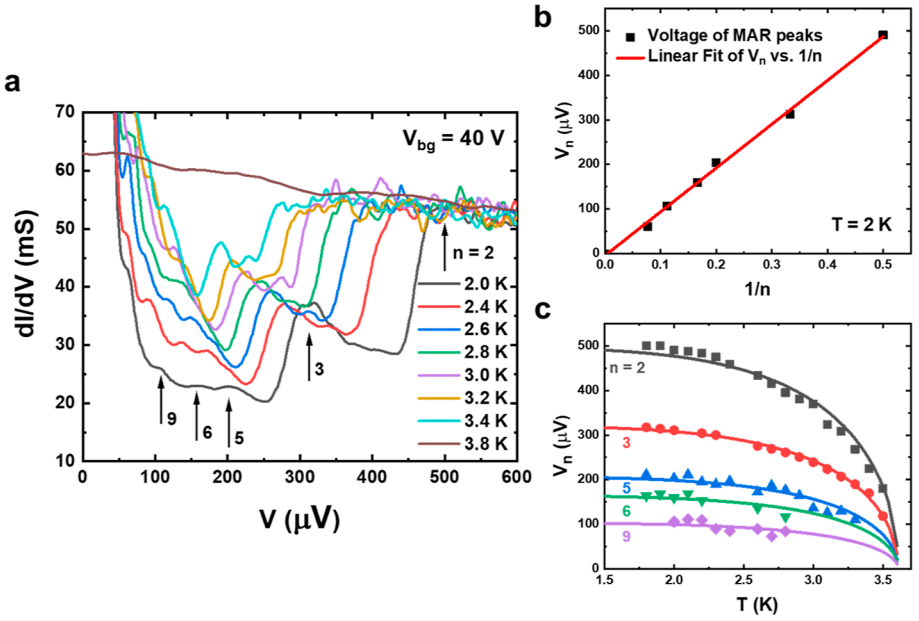

Figure 4. MARs in intimate-contacted Pd_xTe−Te−Pd_xTe devices. (a) Temperature dependence of the differential conductance dI/dV as a function of voltage V. The maxima in dI/dV are assigned with integer index n. (b) dI/dV peak positions V_n as a function of 1/n. The red solid line is a linear fit with a slope of 980 μV. (c) Temperature dependence of V_n for n = 2, 3, 5, 6, and 9. The solid lines are BCS theory fits with $eV_n = 2\Delta_0/n$ and Δ_0 = 496 μV.

transition temperature can be tuned by controlling the diffusion of Pd atoms, which we discuss in the following section. A similar interdiffusion process is observed in Al and Ge−Si systems after thermal treatments.[24]

Intimate-contacted Pd_xTe−Te−Pd_xTe JJs were fabricated in a single-crystal 2D Te flake using selective area chemical transformation.[25−27] As illustrated in Figure 2a, two 5/60 nm Pd/Au electrodes were deposited on top of 2D Te, separated by a small gap (L_{ch} < 0.3 μm). The device was annealed for 30 s in a N_2 atmosphere at 150 °C. Without Pd capping, Te in the gap area remains semiconducting. Thus, a superconducting FET with a gate-tunable barrier (Te) sandwiched by two superconductors (Pd_xTe) is fabricated using a single-step lift-off process. Figure 2b is a false-color scanning electron microscopy (SEM) image of the intimate-contacted superconducting FET device with three different channel lengths L_{ch} (90, 125, and 250 nm). The devices were measured using two electrodes by sending a dc current I and a small ac excitation I_{ac} and monitoring the ac (dc) voltage drop $V_{ac}(V_{dc})$ between the two electrodes. The differential resistance dV/dI was calculated using V_{ac}/I_{ac}. Figure 2c shows the temperature-dependent zero bias (I = 0 μA) differential resistance dV/d$I(T)$ normalized by dV/d$I(T$ = 4 $K)$. We observed supercurrent (zero resistance) in intimate-contacted Pd_xTe−Te devices (red), while the resistance increases upon cooling in Ni-contacted semiconducting Te devices (black). The superconducting behavior was found to be sensitive to the channel length in the intimately contacted Pd_xTe−Te device. The resistance of the junction in long channel devices (250 nm) increased about 2 orders of magnitude compared to the normal resistance in short channel devices (90 nm). In Figure 2d, the dc current I dependence of the differential resistance dV/dI is measured at a temperature of 50 mK, which demonstrates the transition to semiconducting behavior in the same Te flake with different channel lengths. The I_cR_n value, calculated to be 146 μV, is obtained at zero gate bias in the 90 nm short channel length device.

The chemical transformation from Te to Pd_xTe can be controlled by the diffusion of Pd atoms in 2D Te flakes using an annealing process, which is essential for the superconducting behavior. Figure 3a illustrates the cartoon schematic of the Pd-contacted devices with a channel length of 100 nm that were annealed under different conditions (as-fabricated no annealing and 30 and 60 s 150 °C annealing in a N_2 atmosphere). The color mapping of differential resistance dV/dI as a function of the gate voltage V_{bg} and dc current I was used to characterize the electrical transport of the junctions at the temperature of 30 mK. Cyan curves are dV/dI plots at V_{bg} = 0 V. The as-fabricated device did not exhibit superconducting behavior (Figure 3b). However, in the annealed device (30 s, 150 °C), gate-tunable supercurrent is observed with ambipolar behavior (Figure 3c), indicating the formation of Pd_xTe−Te−Pd_xTe junctions. After 60 s of annealing, the channel fully transforms to superconducting Pd_xTe. The superconducting critical current shows no response to the gate voltage (Figure 3d). Moreover, the annealing temperature and time impact the chemical composition x in Pd_xTe, as reflected in the change in the superconducting transition temperature (Figure S2).

The Andreev reflection is a charge transfer process when normal current is converted to supercurrent at the normal conductor to superconductor interface. In a JJ with high interface transparency and low inelastic scattering probabilities, electrons undergo Andreev reflection multiple times at two interfaces until they lose coherence. This is referred to as MARs.[28,29] The temperature-dependent differential conductance dI/dV as a function of the dc voltage V in a Pd_xTe−Te−Pd_xTe JJ is plotted in Figure 4a. The presence of several peaks in dI/dV at $V = V_n = 2\Delta_0/en$ (where Δ_0 is the superconducting gap of Pd_xTe) is a signature of MAR. We assign the integer index n, indicated by black arrows, to each peak and plot the V_n

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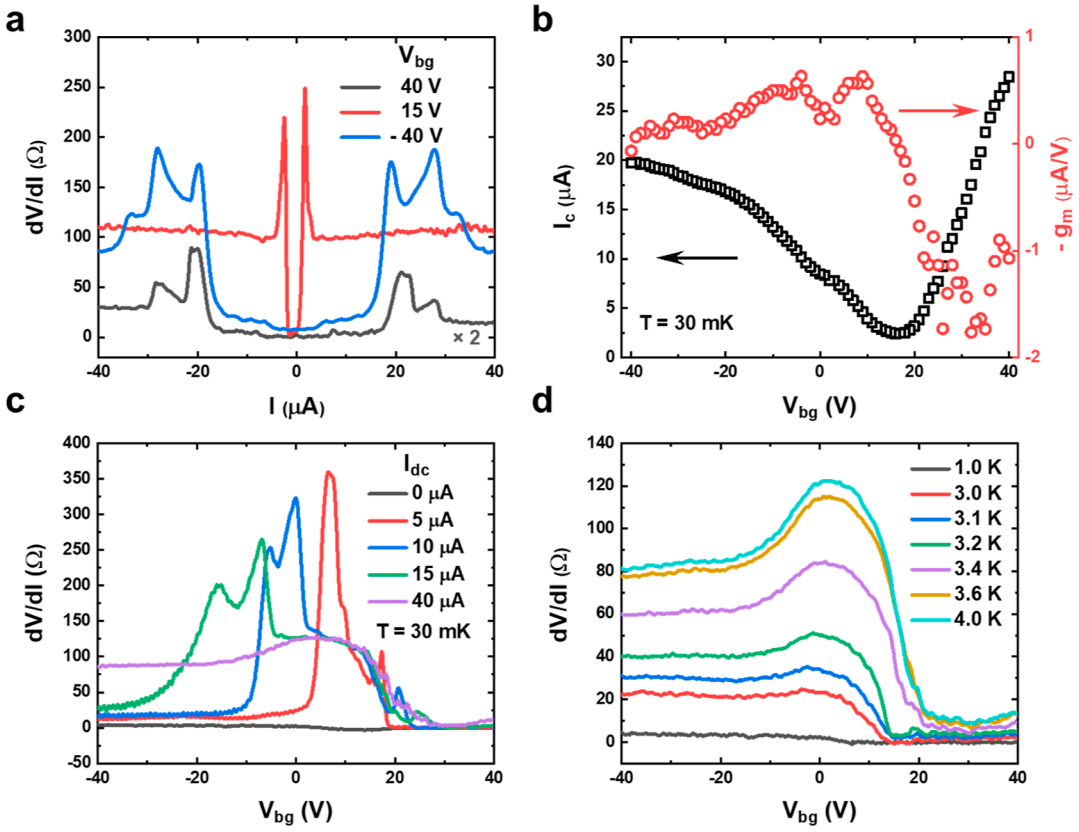

Figure 5. Su-FETs. (a) Differential resistance dV/dI as a function of current I at different gate voltages. (b) Gate voltage dependence of the critical current I_c and transconductance g_m. The device was measured at T = 30 mK. (c) Differential resistance dV/dI as a function of gate voltage V_{bg} at different dc current I. (d) Temperature dependence of the differential resistance dV/dI as a function of gate voltage V_{bg}. The device returns to normal semiconducting field-effect transistor when the temperature is above the superconducting transition temperature.

as a function of 1/n, as shown in Figure 4b. The slope of the linear fitting gives us a superconducting gap of 491 μeV, which agrees well with the superconducting gap of Pd_xTe (550 μeV) obtained from BCS theory[30] ($\Delta = 1.76k_BT_c$). The high transparency of the intimate-contacted Pd_xTe−Te junction is indicated by the observation of MAR features up to n = 9. Additionally, the temperature-dependent MAR peak voltages V_n with n = 2, 3, 5, 6, and 9 are extracted (Figure 4c) and fitted well by BCS theory. The transparency of the semiconductor to superconductor junction is calculated to be 0.32, using $D = 1/(1 + Z^2)$; $Z = eI_{exc}R_n/\Delta$, where I_{exc} is the excess current.[31]

A superconducting FET is also realized in the intimately contacted Pd_xTe−Te−Pd_xTe junction. Figure 5a shows the differential resistance dV/dI as a function of dc current I at V_{bg} = −40, 15, and 40 V. The asymmetrical characterization observed at positive and negative currents may stem from the inherent asymmetry present in the left and right contacts. The gate-tunable normal resistance and critical current indicate that the tunneling barrier of the JJs is controlled by the field-effect. An ambipolar behavior in critical current I_c corresponding to the electrons and holes conducting 2D Te is observed in Figure 5b at the temperature of 30 mK. In a superconducting FET, the transconductance g_m, defined as $g_m = dI_c/dV_{bg}$, describes the gate controllability over the critical current.[32] The maximum transconductance is calculated to be 1.8 μA/V, which could be improved using a scaled high-k dielectric layer such as HfO_2 with a thickness of 10 nm since the critical current is related to the carrier density of 2D Te. The dependence of the differential resistance dV/dI on dc current I (Figure 5c) reveals the ambipolar transition from the superconducting state to the normal state and then the superconducting state at T = 30 mK. When I_{dc} = 40 μA, the device returns to being semiconducting, which is consistent with the zero-bias differential resistance characterization (Figure 5d) at T = 4 K (above the superconducting transition temperature). The color mappings of the differential resistance as a function of the temperature and the direct current at different gate voltages are presented in Figure S3. More than five different 2D Te superconducting FETs were measured, and Figure S4 shows the electrical characterization of another device with a gate-controlled ambipolar supercurrent.

It is worth noting that other compound materials which contain the Te element also exhibit a similar chemical transformation effect.[33,34] Using the high-quality interface provided by the intimate contact, the study of superconducting heterojunctions can be expanded to many other interesting material systems, including ferroelectric (GeTe),[35] ferromagnetic (Fe_3GeTe_2),[36] and topological materials ($MnBi_2Te_4$).[37] This approach also holds promise for achieving a low contact resistance between metals and semiconductors.

CONCLUSIONS

Our study explores the potential of intimate Pd_xTe contacts in inducing superconductivity in chiral semiconductor 2D Te. By diffusing Pd atoms into 2D Te films, we can control the superconductivity of Pd_xTe. This approach leads to the fabrication of Te-based JJs with gate-tunable critical currents and MARs. Our findings represent a significant contribution to

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the field of superconducting electronics as they offer an alternative and effective way to achieve high-quality superconductor−semiconductor interfaces and develop gate-controlled superconducting devices, such as superconducting FETs.

MATERIALS AND METHODS

Growth of 2D Te Flakes. 2D Te flakes are grown by the hydrothermal method. 0.092 g of Na_2TeO_3 and 0.5 g of polyvinylpyrrolidone (Sigma-Aldrich) were added in 33 mL of double-distilled water under vigorous magnetic stirring. 3.35 mL of aqueous ammonia solution (25−28%, w/w %) and 1.65 mL of hydrazine hydrate (80%, w/w %) were added to the solution. The mixture was added in a 50 mL Teflon-lined stainless-steel autoclave and heated at 180 °C for 32 h before naturally cooling down to room temperature.

Device Fabrication. Te flakes were transferred onto a 90 nm SiO_2/Si substrate. For the pure Pd_xTe devices: a 5 nm thin layer of Pd was deposited on the top surface of the 2D Te flakes using electron beam evaporation. After annealing at 150 °C in a N_2 atmosphere using RTA, superconducting Pd_xTe was formed. The standard four-terminal devices were fabricated using electron beam lithography and 50 nm Au metal contacts deposited by electron beam evaporation. For the two-terminal Pd_xTe−Te Su-FETs: 5/50 nm Pd/Au was deposited by using electron beam evaporation after electron beam lithography patterning.

Low-Temperature Electrical-Transport Measurements. The electrical-transport measurements were performed in a Triton 300 (Oxford Instruments) dilution fridge system with 12 T superconducting coils at temperatures down to 20 mK. The electrical data were acquired by the standard small signal ac measurement technique using SR830 lock-in amplifiers (Stanford Research) at a frequency of 13.333 Hz. The differential resistance measurement was performed with a low ac excitation (under 20 nA).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c02352.

Additional details for carrier density and Hall mobility, controlling the superconducting transition temperature, temperature-dependent color mapping at different gate voltages, and the characterization of another device (PDF)

AUTHOR INFORMATION

Corresponding Authors

Wenzhuo Wu − *School of Industrial Engineering, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0003-0362-6650; Email: wu996@purdue.edu

Peide D. Ye − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0001-8466-9745; Email: yep@purdue.edu

Authors

Chang Niu − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0003-3175-7164

Mingyi Wang − *School of Industrial Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

Zhuocheng Zhang − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

Gang Qiu − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

Yixiu Wang − *School of Industrial Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

Dongqi Zheng − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0002-1665-352X

Pai-Ying Liao − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States; Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.4c02352

Author Contributions

P.D.Y. conceived and supervised the project. P.D.Y. and C.N. designed the experiments. M.W. and Y.W. synthesized the 2D Te under the supervision of W.W. C.N., Z.Z., G.Q., D.Z., and P.-Y.L. fabricated the devices. C.N. performed the magneto-transport measurements and analyzed the data. P.D.Y. and C.N. wrote the manuscript, and all the authors commented on it.

Notes

The authors declare no competing financial interest.

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