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ARTICLE

Indium–Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating

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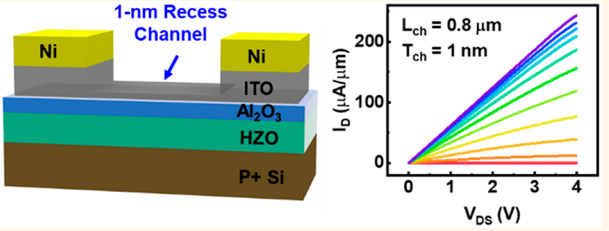
ABSTRACT: In this work, we demonstrate high-performance indium–tin-oxide (ITO) transistors with a channel thickness down to 1 nm and ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ as gate dielectric. An on-current of 0.243 A/mm is achieved on submicron gate-length ITO transistors with a channel thickness of 1 nm, while it increases to as high as 1.06 A/mm when the channel thickness increases to 2 nm. A raised source/drain structure with a thickness of 10 nm is employed, contributing to a low contact resistance of 0.15 Ω·mm and a low contact resistivity of 1.1×10^{-7} Ω·cm^2. The ITO transistor with a recessed channel and ferroelectric gating demonstrates several advantages over 2D semiconductor transistors and other thin-film transistors, including large-area wafer-size nanometer thin-film formation, low contact resistance and contact resistivity, an atomic thin channel being immune to short channel effects, large gate modulation of high carrier density by ferroelectric gating, high-quality gate dielectric and passivation formation, and a large bandgap for the low-power back-end-of-line complementary metal-oxide-semiconductor application.



KEYWORDS: *indium–tin oxide, wide bandgap, oxide semiconductor, hafnium zirconium oxide, ferroelectric, ultrathin body*

The complementary metal-oxide-semiconductor (CMOS) scaling is the driving force of the progress in microelectronics technology. Transistors with an ultrathin semiconductor channel are well known to enhance the electrostatic gate control and the immunity to short channel effects and to further shrink the size of transistors in the integrated circuit. Therefore, two-dimensional (2D) van der Waals materials, as atomically thin semiconductors, have attracted wide attention as channel materials for next-generation microelectronic devices over the past decade.[1−11] However, there are three major limitations for 2D materials that limit the application of 2D materials as transistor channels in CMOS integrated circuits. The first limit is the high contact resistance in 2D transistors in general due to the existing Schottky barriers at metal/2D semiconductor interfaces and the lack of proper doping techniques in 2D materials.[3,4,7] The 2D semiconductor underneath source/drain contact metals is also atomically thin, which limits the current flow to the channel, resulting in a high access resistance. The second challenge is to grow large-area or wafer-scale single-crystal 2D semiconductors compatible with CMOS integration.[12] The third drawback is that it is fundamentally difficult to form high-quality gate dielectrics with low interface trap density on top of 2D materials, because there is no dangling bond on 2D surfaces and the conventional atomic layer deposition cannot be chemically initiated.[11]

Thin-film transistors (TFTs) with an oxide semiconductor channel, such as indium–gallium–zinc-oxide (IGZO), are widely studied for display applications. But there are very few studies that apply thin-film transistor technology for back-end-of-line (BEOL) CMOS digital applications. Indium–tin-oxide (ITO) is an n-type degenerate semiconductor with an optical bandgap of 3.5–4.3 eV and is frequently used as a transparent "metal" layer due to its very high electron doping introduced by Sn. The typical electron density of ITO as a transparent conductor is about 10^{20}–10^{21}/cm^3, which is usually too high as a transistor channel. ITO transistors were reported by forming a more semiconducting-type channel with an electron density of ~10^{19}/cm^3 and good current on/off ratio as a switch.[13−17] Ferroelectric gating was also reported to enhance the gate controllability.[13] Li *et al.* recently reported a high-performance ITO transistor with channel thickness down to 4 nm. An on-current (I_{ON}) exceeding 1 A/mm was achieved on a device with

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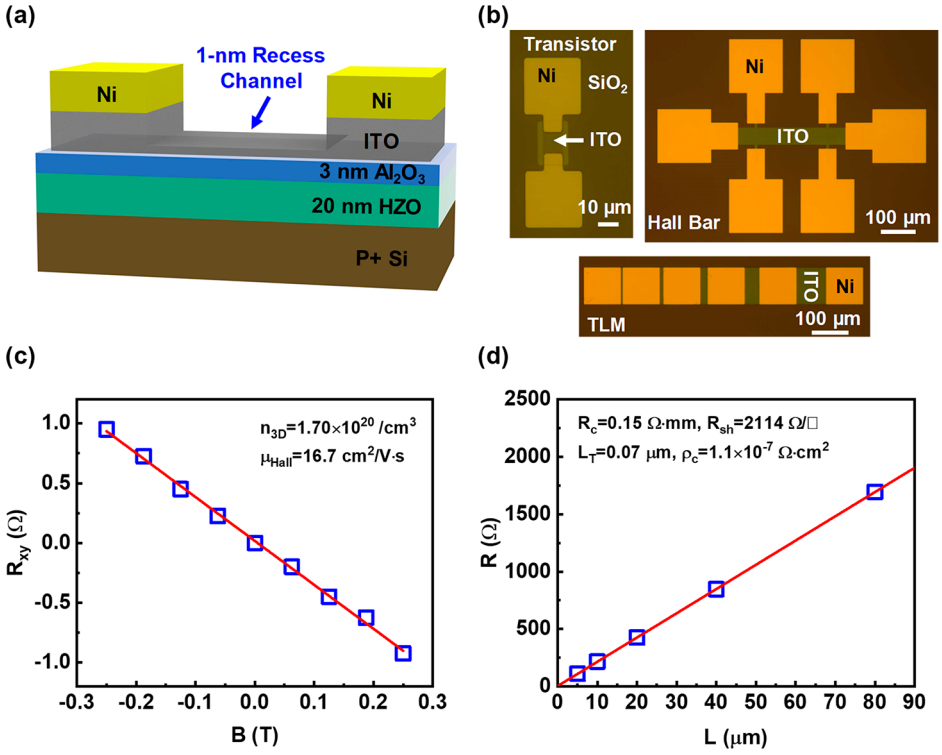

Figure 1. (a) Schematic diagram of an ITO transistor with a 1 nm thick recess channel. The gate stack includes p+ Si as gate electrode and 20 nm ferroelectric HZO/3 nm Al_2O_3 as gate insulator. Ni (80 nm) is used for source/drain electrodes. The thickness of ITO underneath the source/drain electrodes is 10 nm, while the thickness of the ITO channel is 1 or 2 nm, controlled by wet etching. (b) Photo images of the experimental ITO transistor, Hall bar, and TLM structures. SiO_2 (50 nm) is used under the source/drain pads to reduce the leakage current between gate and source/drain pads. (c) R_{xy} *versus* B field in the Hall measurement of 10 nm ITO with a floating gate. An electron density of 1.7×10^{20} /cm^3 and a Hall mobility of 16.7 cm^2/V·s are extracted. (d) TLM measurement of 10 nm ITO with Ni contacts. A low contact resistance of 0.15 Ω·mm and a low contact resistivity of 1.1×10^{-7} Ω·cm^2 are achieved.

a 10 nm thick ITO channel at a channel length of 200 nm, demonstrating that an ITO TFT can be a promising candidate for low-power high-performance device application.[16] Further reduction of ITO channel thickness is highly demanded to further improve the immunity to short channel effects for transistor scaling. Beyond ITO, scaled devices on W-doped In_2O_3 (IWO) or IGZO are also being investigated now.[18,19] More importantly, a TFT with oxide semiconductor as channel recently attracted revived interest since it can be applied in BEOL-compatible transistors for monolithic 3D integration.[20]

In this work, we report ITO transistors with a 1 and 2 nm thick channel and ferroelectric (FE) hafnium zirconium oxide ($HfZrO_2$ or HZO) as gate insulator. Highly doped ITO with a 3D carrier density (n_{3D}) of 1.7×10^{20}/cm^3 is employed, which enables a channel thickness (T_{ch}) scaling down to 1 nm. The high polarization charge density in FE HZO[21−25] enhances the gate controllability so that the high carrier density can be fully depleted. A raised source/drain structure is applied so that a low contact resistance (R_c) of 0.15 Ω·mm and a low contact resistivity (ρ_c) of 1.1×10^{-7} Ω·cm^2 are achieved. A high I_{ON} of 1.06 A/mm is achieved on the ITO transistor with T_{ch} = 2 nm and 0.243 A/mm with T_{ch} = 1 nm with submicron channel length. Therefore, high-performance ITO transistors with low contact resistance and ultrathin channel are obtained simultaneously, which overcomes fundamental challenges of 2D semiconductors. These results suggest ITO as a promising channel material for BEOL CMOS application.

RESULTS AND DISCUSSION

Figure 1(a) illustrates the schematic diagram of an ITO transistor with a recessed 1 nm thick channel and ferroelectric gating. The gate stack includes heavily boron-doped silicon (p+ Si, resistivity <0.005 Ω·cm) as gate electrode and 20 nm FE HZO/3 nm Al_2O_3 as gate insulator. Ni (80 nm) is used for source/drain electrodes. The thickness of ITO underneath the source/drain electrodes is 10 nm, while the thickness of the ITO channel is 1 or 2 nm. Figure 1(b) shows photo images of the fabricated ITO transistor, Hall bar, and transmission line model (TLM) structures, capturing the ITO channel, Ni electrodes, and SiO_2 for test pad isolation.

Figure 1(c) shows the R_{xy} *versus* B field in Hall measurement of 10 nm ITO with a floating gate at room temperature. From the Hall measurement, a bulk doping concentration n_{3D} of 1.7×10^{20} /cm^3 and a Hall mobility (μ_{Hall}) of 16.7 cm^2/V·s are determined. Without considering the surface states, we can estimate an n_{2D} of 1.7×10^{13}/cm^2 for a 1 nm channel at zero gate bias, which is about the right carrier density range to be modulated and controlled by an electrostatic gate, suggesting the recess channel can be used to enhance the on/off ratio. Figure 1(d) shows resistance (R) *versus* length (L) characteristics in the TLM measurement of 10 nm ITO with Ni contacts. An R_c of 0.15 Ω·mm, sheet resistance (R_{sh}) of 2114 Ω/□, and transfer length (L_T) of 0.07 μm are extracted by linear fitting of R with respect to L. A contact resistivity (ρ_c) of 1.1×10^{-7} Ω·cm^2 is achieved according to $L_T = \sqrt{\rho_c/R_{sh}}$. Due to the near-metallic

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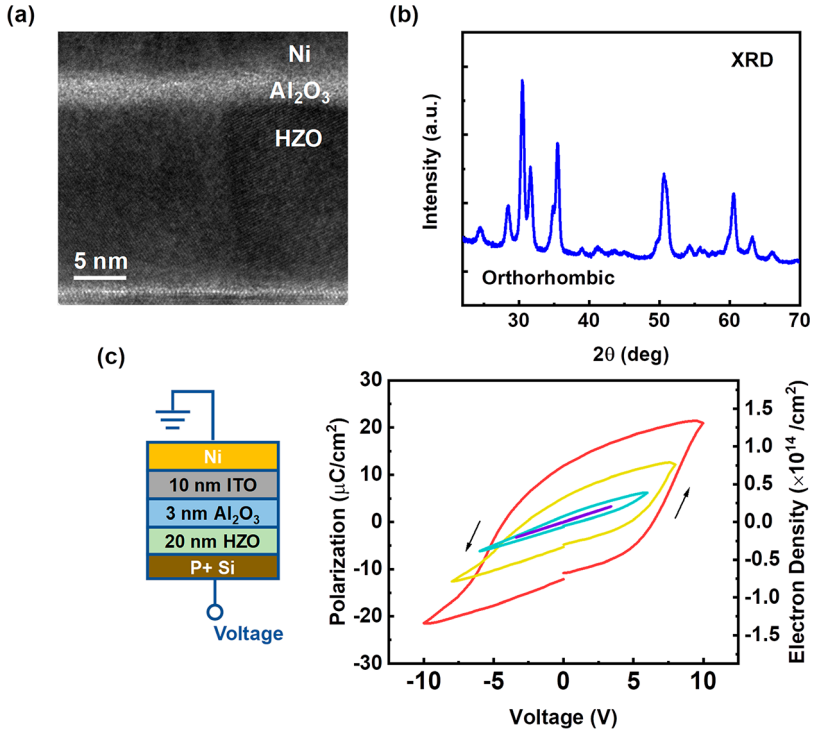

Figure 2. (a) TEM image of the Ni/Al_2O_3/HZO/Si stack, capturing amorphous Al_2O_3 and polycrystalline HZO. (b) XRD measurement of ferroelectric HZO, showing the HZO crystal contains an orthorhombic phase. (c) $P-V$ measurement of the p+ Si/20 nm HZO/3 nm Al_2O_3/10 nm ITO stack, showing clear ferroelectric polarization switching. The maximum polarization is greater than 20 μC/cm^2, corresponding to a 2D electron density over 10^{14}/cm^2, indicating 10 nm ITO has a carrier density over 10^{14}/cm^2, which is consistent with Hall measurement in Figure 1(c).

ITO characteristic, the obtained R_c and ρ_c are much better than those typically obtained from 2D van der Waals materials.[4,7,10]

Figure 2(a) shows a transmission electron microscopy (TEM) image of a Ni/Al_2O_3/HZO/Si stack, capturing the amorphous Al_2O_3 and polycrystalline HZO. Figure 2(b) shows the X-ray diffraction (XRD) spectrum of FE HZO, confirming the HZO crystal contains an orthorhombic phase, which leads to the ferroelectricity of HZO. Figure 2(c) shows the $P-V$ measurement of a 20 nm HZO/3 nm Al_2O_3 capacitor with 10 nm ITO as top electrode and p+ Si as the bottom electrode, where the voltage is applied to the p+ Si electrode. The high polarization and ferroelectric hysteresis loop confirm the ferroelectricity of this structure. The corresponding $C-V$ measurement at 1 kHz on the same device is shown in Figure S1 in the Supporting Information, showing a typical ferroelectric $C-V$ hysteresis loop. Capacitance at the negative voltage is lower than that at positive voltage because of the depletion of ITO as a degenerated semiconductor. Note that a maximum polarization over 20 μC/cm^2 corresponds to a 2D electron density (n_{2D}) over 10^{14} /cm^2. The $P-V$ measurement gives two clear indications except for the confirmation of ferroelectricity. The first is n_{2D} in 10 nm ITO is higher than 10^{14}/cm^2, which is consistent with the Hall measurement in Figure 1(c), suggesting a recessed channel is necessary for sufficient gate control. An ITO transistor with a T_{ch} of 10 nm cannot be switched off by both conventional gating and ferroelectric gating, as shown in Figure S3 in the Supporting Information. The second indication is that the HZO/Al_2O_3/ITO oxide/oxide interface has a relatively low interface trap density compared to the FE polarization density. So, it could achieve a gate control of n_{2D} over 10^{14}/cm^2, similar to ion-liquid gating. This gate control by ferroelectric polarization plays an important role in realizing the high-performance ITO transistor in this work.

Figure 3(a and b) show the I_D-V_{GS} and I_D-V_{DS} characteristics of an ITO transistor with a channel length (L_{ch}) of 0.6 μm and a T_{ch} of 2 nm, exhibiting an I_{ON} of 1.06 A/mm and on/off ratio over 6 orders of magnitude. I_D in the off-state is the result of gate leakage current, as shown in Figure S12, suggesting optimizing the gate stack can further improve the on/off ratio. The inset of Figure 3(a) is the AFM measurement of the 2 nm thick ITO channel. Figure 3(c and d) show the I_D-V_{GS} and I_D-V_{DS} characteristics of an ITO transistor with an L_{ch} of 0.8 μm and a T_{ch} of 1 nm, exhibiting an I_{ON} of 0.243 A/mm. The inset of Figure 3(c) is the AFM measurement of the 1 nm thick ITO channel. The I_{ON} values of ITO transistors with a channel thickness in the 1 to 2 nm range are significantly higher than most of the reported 2D transistors with reasonable on/off ratio.[1−11] The hysteresis in the I_D-V_{GS} curve in Figure 3(a and c) is the result of ferroelectric polarization and the minor hysteresis loop. To further understand this phenomenon, an ITO transistor with an L_{ch} of 3 μm and a T_{ch} of 2 nm is measured by applying different voltage sweep ranges. As shown in Figure S6 in the Supporting Information, the I_D-V_{GS} characteristics have a smaller hysteresis at a reduced voltage sweep range (from 15 to 4 V). The I_D-V_{GS} characteristics of ITO transistors with a T_{ch} of 1 and 2 nm and an L_{ch} from 40 μm down to 1 μm are summarized in Figure S7 and Figure S8 in the Supporting Information, showing similar characteristics to short channel devices except for channel length dependent on-current. Figure 3(e) shows I_{ON} *versus* $1/L_{ch}$ scaling metrics of an ITO transistor with a T_{ch} of 1 and 2 nm at V_{DS} = 4 V, suggesting channel length scaling can bring further performance benefit. The I_{ON} *versus* $1/L_{ch}$ scaling metrics follow a linear trend until 1 μm. Considering

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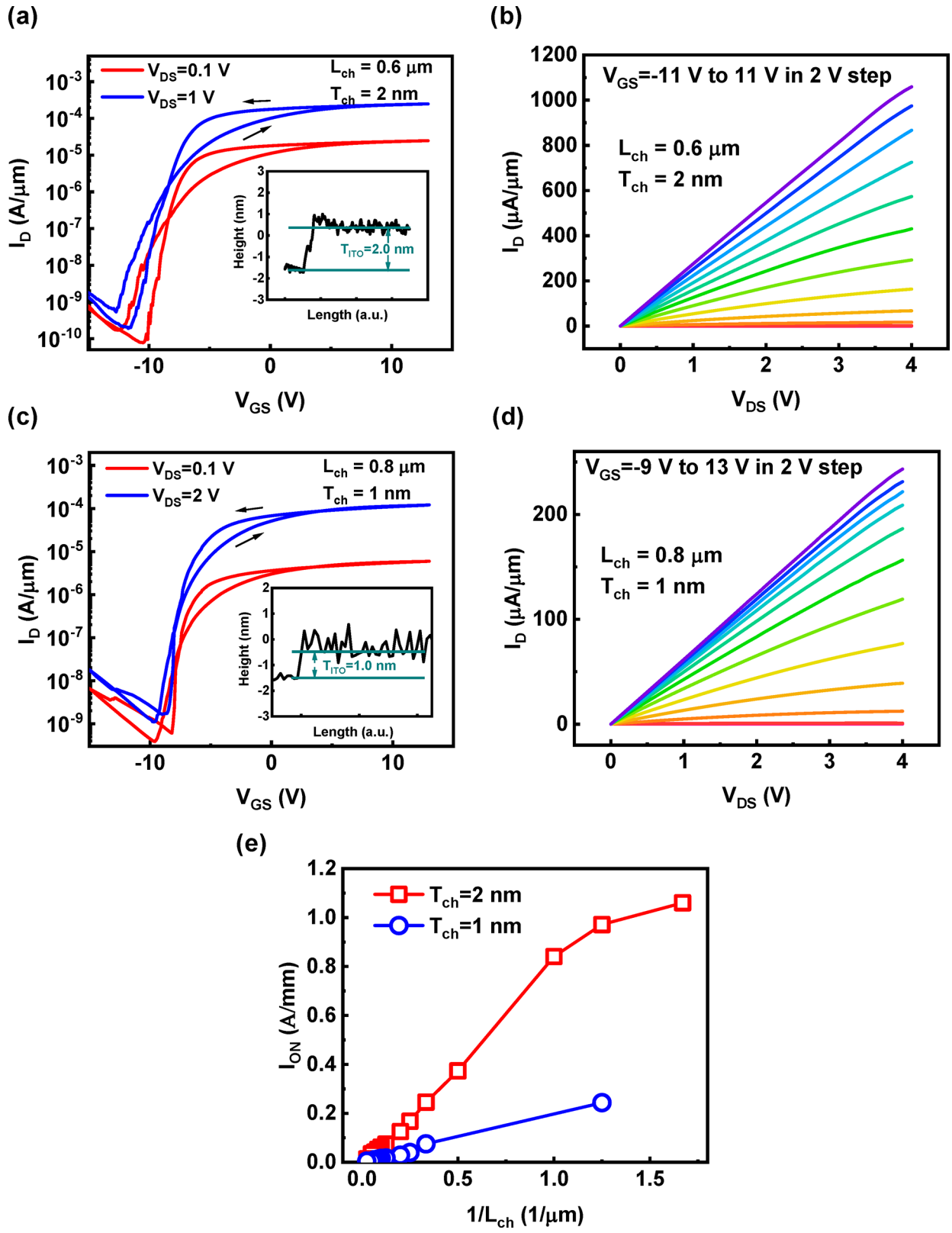

Figure 3. (a) I_D−V_{GS} and (b) I_D−V_{DS} characteristics of an ITO transistor with a channel length of 0.6 μm and channel thickness of 2 nm, exhibiting an on-current of 1.06 A/mm and on/off ratio over 6 orders. (c) I_D−V_{GS} and (d) I_D−V_{DS} characteristics of an ITO transistor with a channel length of 0.8 μm and channel thickness of 1 nm, exhibiting an on-current of 0.243 A/mm. (e) I_{ON} scaling metrics of ITO transistors with channel thicknesses of 1 and 2 nm at V_{DS} = 4 V.

the geometry screen length of ITO transistors[16] (λ = 3.3 nm for 2 nm ITO and λ = 2.4 nm for 1 nm ITO), the deviation from 1/L_{ch} scaling at the submicron channel is likely to be the result of mobility degradation by a self-heating effect, instead of short channel effects. Source/drain series resistance (R_{SD}) is extracted to be 0.14 and 0.15 Ω·mm for ITO transistors with a T_{ch} of 1 and

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2 nm, by linear fitting of on-resistance *versus* channel length at different V_{GS}, as shown in Figure S9 in the Supporting Information, which is even smaller than the value obtained from TLM measurements in Figure 1(d).

Figure 4 shows the effective mobility (μ_{eff}) of 1 and 2 nm ITO extracted from drain conductance (g_d) in I_D-V_{DS} characteristics,

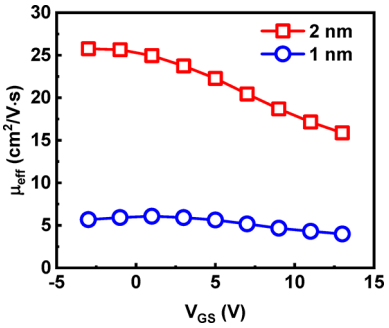

Figure 4. Effective mobility *versus* gate voltage, extracted from output conductance of ITO transistors. μ_{eff} values of 26.0 and 6.1 $cm^2/V\cdot s$ are achieved for 1 and 2 nm ITO.

where $\mu_{eff} = \frac{g_d L_{ch}}{W_{ch} Q_n}$ and Q_n is the channel mobile charge density and W_{ch} is the channel width. μ_{eff} values of 26.0 and 6.1 $cm^2/V\cdot s$ are achieved for 2 and 1 nm thick ITO, respectively. The mobility degradation with decreasing channel thickness is attributed to the increasing surface scattering, as also shown in the surface roughness study in Figure S2. Mobility could be improved by atomic layer deposition (ALD) surface passivation or reducing the surface roughness. The field-effect mobility (μ_{FE}) is extracted from transconductance (g_m) using $\mu_{FE} = \frac{g_m L_{ch}}{W_{ch} C_{ox} V_{DS}}$. μ_{FE} values of 27.0 and 6.5 $cm^2/V\cdot s$ are achieved for 2 and 1 nm thick ITO, which are consistent with effective mobilities. Carrier density can be estimated according to $I_D = n_{2D} q \mu E$, where n_{2D} is the 2D carrier density, q is the elementary charge, μ is the mobility, E is the source to drain electric field. According to this equation, the carrier density in 1 and 2 nm ITO channels can be calculated as shown in Figure S10. Carrier densities of 1 and 2 nm ITO are similar, with a maximum n_{2D} of about 0.8×10^{14} /cm^2. Such higher channel carrier density oxide/oxide interface far beyond the polar semiconductor interface and the enhanced modulation of carrier density with high on/off ratio is because of the strong ferroelectric polarization switching.

The recessed channel and ferroelectric gating device structure is critical to realize a high-performance and ultrathin body ITO transistor with several advantages compared to 2D semiconductors and low-doped ITO transistors: (i) Large-area wafer-size nanometer-thin ITO films can be formed by a conventional sputtering technique and the process temperature fulfills the BEOL requirement of lower than 350 °C. (ii) Thick and heavily doped ITO under source/drain electrodes contributes to the low contact resistivity and contact resistance. (iii) Heavily doped ITO enables channel thickness scaling down to 1 nm, comparable to atomic-scale single-layer or bilayer 2D van der Waals semiconductor channels. (iv) A 1 nm thick channel offers excellent immunity to short channel effects, which provides a clear route to further scale the device down to the sub-10 nm region with much higher device performance. (v) The high polarization density in the ferroelectric gate insulator provides sufficient gate modulation of the high carrier density in the ITO channel. (vi) ALD passivation and dielectrics can be applied to the ITO channel easily because it is a 3D material with a dangling bond on the surface being different from a 2D van der Waals surface. (vii) ITO offers a semiconductor bandgap as high as 3.5−4.3 eV with the potential for power electronics application. These advantages and the demonstrated high-performance transistors suggest ITO is a promising oxide channel material for BEOL CMOS applications.

CONCLUSION

In conclusion, high-performance ITO transistors with a 1 and 2 nm thick channel and ferroelectric gating are demonstrated. A high I_{ON} of 1.06 and 0.243 A/mm is achieved on ITO transistors with T_{ch} = 2 and 1 nm, respectively. A raised source/drain structure is employed so that a low contact resistance of 0.15 Ω·mm and low contact resistivity of 1.1×10^{-7} Ω·cm^2 are achieved. A low contact resistance and ultrathin channel are obtained simultaneously, which overcomes the fundamental limitations of 2D semiconductors. The advantages of the ITO transistor suggest ITO as a promising oxide channel material for BEOL CMOS applications.

METHODS

Device Fabrication. The device fabrication process started with an ALD of 20 nm HZO and 3 nm Al_2O_3 on a p+ Si substrate. The ALD HZO and Al_2O_3 were deposited at 200 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), $(CH_3)_3Al$ (TMA), and H_2O as the Hf, Zr, Al, and O precursors. The $Hf_{1-x}Zr_xO_2$ film with x = 0.5 was achieved by controlling the HfO_2:ZrO_2 cycle ratio to be 1:1. After the deposition of the HZO/Al_2O_3 stack, the samples were annealed at 500 °C in a N_2 environment for 1 min by rapid thermal annealing. ITO (10 nm) was deposited by RF sputtering from a 15 cm diameter target with a composition of 90 wt % In_2O_3 and 10 wt % SnO_2 and with a target-to-substrate distance of approximately 20 cm. The sputtering power was 650 W in an argon ambient with a working pressure of 2×10^{-3} Torr after achieving a base pressure of at least 2×10^{-6} Torr. A 4 min presputter was completed for surface contaminant removal, and the process was completed without supplemental heating. Device isolation was then performed by wet etching of ITO using a hydrochloric acid solution (HCl, 20%). SiO_2 (50 nm) was then deposited by e-beam evaporation for the isolation of source/drain pads, which can effectively reduce the leakage current and parasitic capacitance introduced by nonideal test pads. Ni (80 nm) was then deposited as source/drain electrodes. Channel recessing was done by wet etching using a diluted HCl solution (3.4%), so that the etch rate of ITO can be accurately controlled at the nanometer scale, where the etch rate is about 1 nm/s, as shown in Figure S1 in the Supporting Information.

Device Characterization. The thickness of the ITO was measured using a Veeco Dimension 3100 atomic force microscope system. Electrical characterization was carried out with a Keysight B1500 system with a Cascade Summit probe station.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.0c03978.

Additional details for the wet etching process and surface roughness, $C-V$ measurement of the gate stack, $I-V$ characteristics of ITO transistors without channel recess and with a dielectric gate insulator, minor loops in the ITO transistor with ferroelectric gating, channel length- and thickness-dependent $I-V$ characteristics, series resistance extraction, carrier density of the ITO channel, analysis on device variations (PDF)

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Author Contributions

P.D.Y. conceived the idea and supervised experiments. J.A. and R.A. did the ITO film sputtering. X.L. did the ALD deposition of HZO and Al_2O_3. M.S. performed the device fabrication, electrical measurement, and data analysis. C.N. and M.S. conducted the Hall measurement. S.D. provided critical technical inputs on the experiments. M.S. and P.D.Y. cowrote the manuscript, and all authors commented on it.

Notes

The authors declare no competing financial interest.

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