Supplementary Information for:

On the Ferroelectric Polarization Switching of Hafnium Zirconium Oxide in Ferroelectric/Dielectric Stack

Mengwei Si, Xiao Lyu, and Peide D. Ye*

School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States

* Address correspondence to: yep@purdue.edu (P.D.Y.)

1. Ferroelectric/Dielectric Stack with Internal Metal

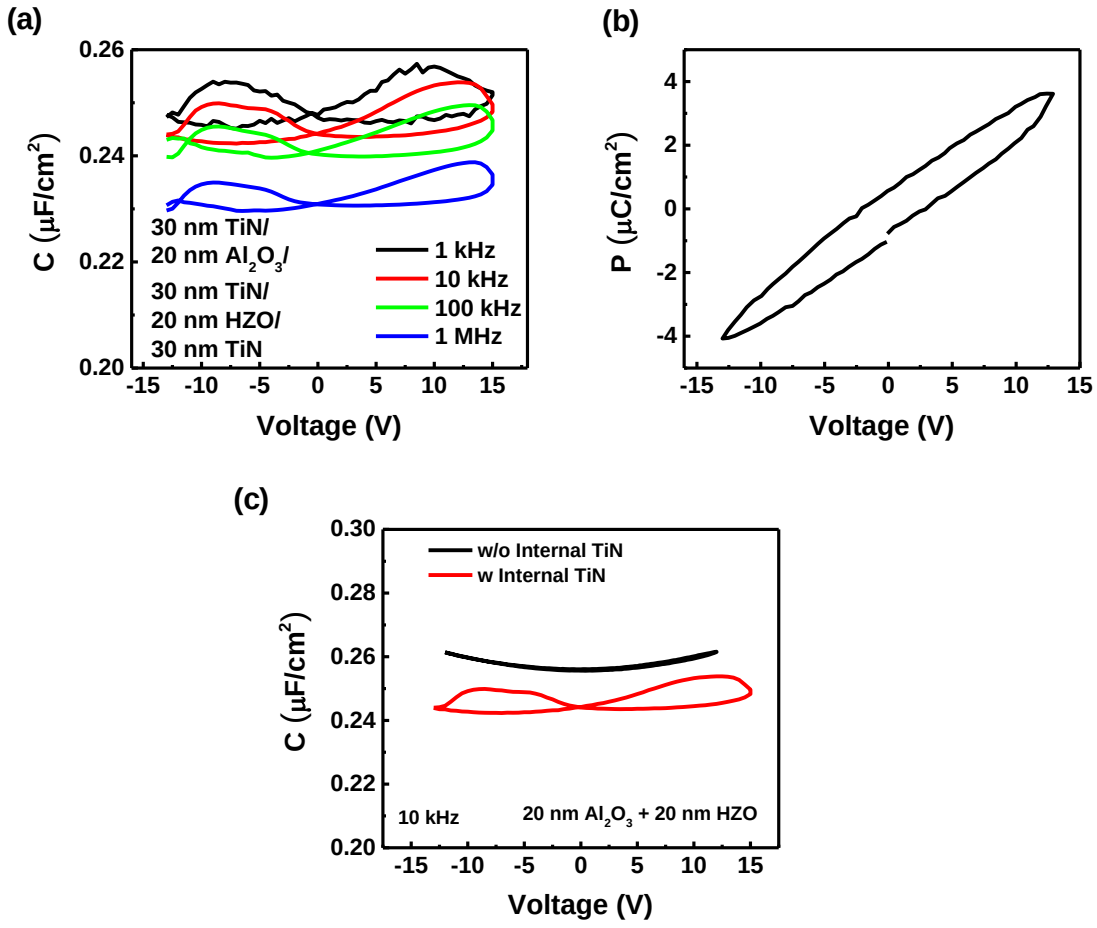

Figure S1. (a) C-V measurement and (b) P-V measurement on a type D capacitor with 20 nm Al_2O_3 and 20 nm HZO. (c) C-V measurements comparison of a type C and a type D capacitor with 20 nm Al_2O_3 and 20 nm HZO.

Fig. S1(a) shows the C-V measurement of a type D capacitor with 20 nm HZO, 20 nm Al_2O_3 and 30nm TiN in between, measured from 1 kHz to 1 MHz. The two signature capacitance peaks in the C-V hysteresis loop are observed. Fig. S1(b) shows the P-V measurement of a type D capacitor with 20 nm HZO and 20 nm Al_2O_3, where a weak ferroelectric hysteresis loop is achieved. Fig. S1(c) shows the comparison of C-V measurements of type C and type D capacitors with 20 nm HZO and 20 nm Al_2O_3. Although same thicknesses of HZO and Al_2O_3 are used, a type D capacitor with 30 nm TiN exhibits weak ferroelectricity in C-V and P-V

characteristics, suggesting that the charge in the internal metal can assist the ferroelectric switching process, in great contrast to the result from a type C capacitor. Fig. S1(c) concludes the FE/DE stacks with internal metal and without internal metal are physically very different. If the internal metal gate becomes much larger than the capacitor area by design or it is externally connected to metal wires through vias or the internal metal gate is physically connected to the measurement equipment, the required balanced charges can be provided even externally. All these facts are extremely important to understand and interpret the experimental observation related to Fe-FETs and NC-FETs.

2. Interfacial Coupling in Ferroelectric/Dielectric Stack

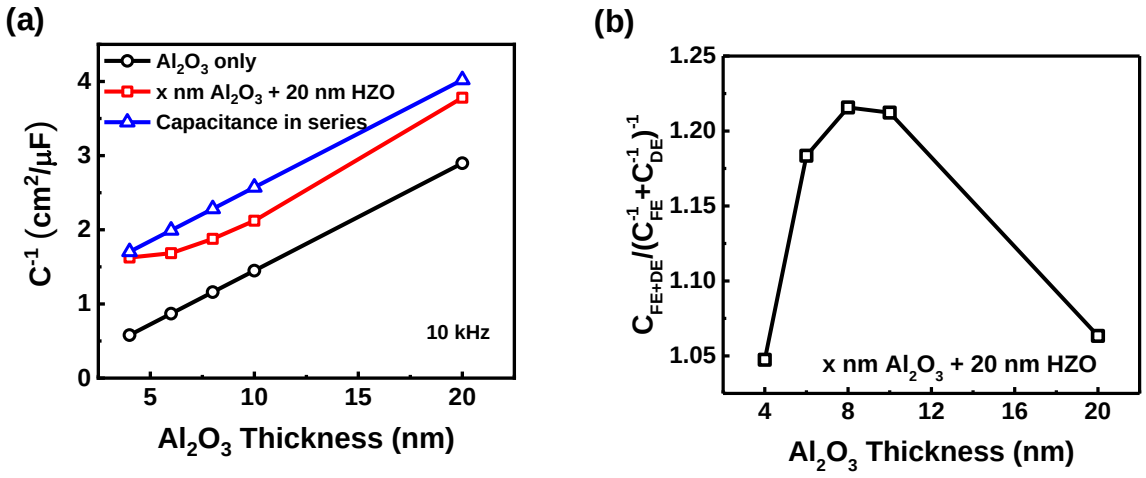

Figure S2. (a) Capacitance^{-1} of type C capacitor versus Al_2O_3 thickness, by both experimental measurements (red squares) and calculated total capacitance (blue triangles). The calculated total capacitance in series is based on the experimental measurements of type A and type B capacitors, using the maximum capacitance in the measured C-V curves. The capacitance values of measured type A capacitors with different Al_2O_3 thicknesses are presented as black circles. (b) The ratio of experimental capacitances of type C capacitor over capacitance in series versus different Al_2O_3 thickness.

Fig. S2(a) shows the capacitance^{-1} versus Al_2O_3 thickness characteristics of three types of capacitors, Al_2O_3 only (type A), Al_2O_3/20 nm HZO stack (type C) and the capacitance value of measured Al_2O_3 (type A) and HZO (type B) capacitors in series. Experimentally, capacitance of type C capacitor is lower than type A capacitor with same Al_2O_3 thickness. No obvious QSNC effect is observed in HZO material system. But a capacitance enhancement of type C capacitor is observed to be larger than the capacitance value in series, as shown in Fig. S2(b). Over 20% capacitance enhancement is observed with 8 and 10 nm Al_2O_3/20 nm HZO stack. This result shows from another aspect that the FE/DE stack with internal metal and without internal metal are physically very different. It demonstrates the existence of interfacial coupling[1-6] between the Al_2O_3 layer and HZO layer. This interfacial coupling effect can improve the equivalent oxide

thickness of FE/DE gate stack. The static capacitance enhancement by negative capacitance effect ($C_{TOT} > C_{DE}$) is not directly achieved in this slow measurement. The intrinsic quasi-static negative capacitance phenomenon might be masked by the charge trapping and de-trapping.[10] So it is not conclusive to claim the existence of negative capacitance or not in this work using HZO as the ferroelectric stack.

3. DC Enhancement in Fe-FET

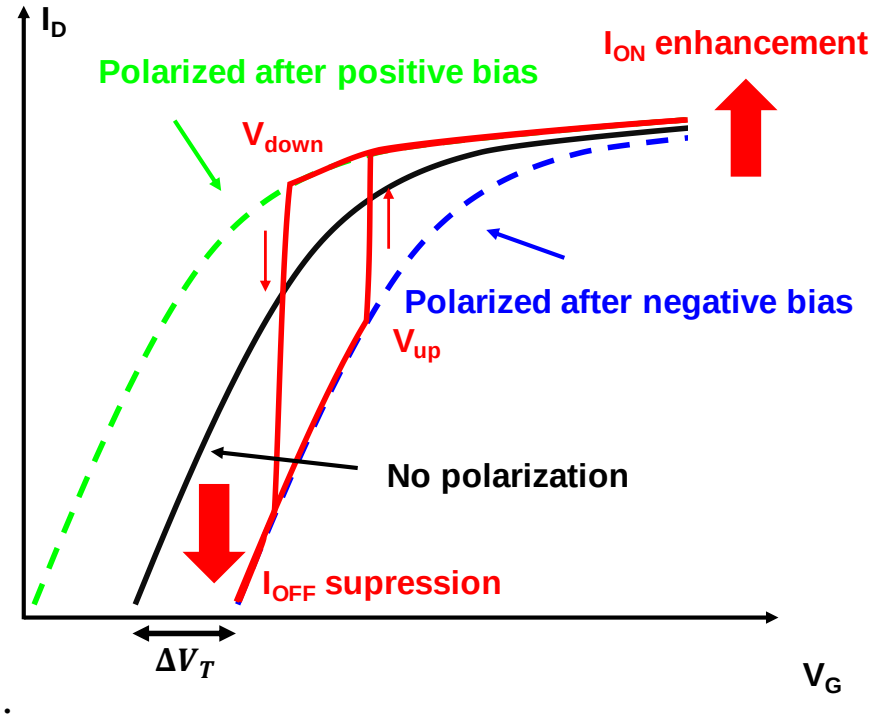

Figure S3. (a) Illustration of DC enhancement of a ferroelectric-gated FET.

It is clear that ferroelectric polarization switching can lead to the sub-60 mV/dec subthreshold slope (SS) in ferroelectric-gated transistors. But hysteresis in transfer characteristics is unavoidable, if not considering charge trapping process. Note that the concept of transient NC effect in Fe-FETs[7-9] is fundamentally different from the concept of QSNC effect in NC-FETs. But it is unclear whether performance benefit is achievable or not with a hysteretic and sub-60 mV/dec device. Here, the authors want to emphasize that ferroelectric polarization switching and polarization charge in Fe-FETs can offer DC enhancement (I_{OFF} reduction and I_{ON} enhancement simultaneously), with the existence of manageable hysteresis and without incorporating QSNC explanation. All transient effects of ferroelectric dynamic polarization switching[10–15] are negligible in DC condition discussed in this work. Meanwhile, the hysteresis might not have serious impact in logic circuits if it is controlled in between zero voltage and half of the supply

voltage (V_{DD}). Thus, this work addresses an important fact that ferroelectric field-effect transistors can offer DC enhancement from the perspective of ferroelectric polarization switching only. The potential of using ferroelectric-gated transistor for low-power logic applications is limited by the speed of the devices.

In a CMOS logic circuit, a lower off-state current (I_{OFF}) and higher on-state current (I_{ON}) is preferred. The DC enhancement here is defined as at the same I_{OFF} and a given supply voltage (V_{DD}), the transistor can have higher I_{ON}. Whether a small hysteresis exists or not is not important if lower I_{OFF} and higher I_{ON} can be achieved simultaneously. For circuit applications, hysteresis window of the devices should be controlled less than half of the V_{DD}. As shown in Fig. S3, the black line is the transfer characteristics of the baseline FET without ferroelectric polarization. If a high gate voltage is applied, the transfer curve shifts to the left as the green curve. If a low gate voltage is applied, the transfer curve shifts to the right as the blue curve. The amount of threshold voltage shift (ΔV_T) is determined by the remnant polarization, the capacitance of dielectric layer (C_{DE}) and the ratio of ferroelectric capacitor area (A_{FE}) and the dielectric capacitor area (A_{DE}) (assuming the existence of an internal metal layer). Note that the conclusion is still valid in FE/DE stack without internal metal, but the area ratio of A_{FE} and A_{DE} becomes one. The transfer characteristics of the Fe-FET switches between the polarization up and polarization down transfer curves and the switching voltages (V_{up}, V_{down}) are determined by the coercive voltages. The coercive voltages can be tuned by the thickness of the FE layer, so V_{up} and V_{down} can be tuned accordingly. Therefore, if we plot the full bi-directional transfer characteristics, as the red line in Fig. S3, a reduction in I_{OFF} and an enhancement in I_{ON} are achieved simultaneously. This exactly shows the DC enhancement can be achieved using a Fe-FET structure. The difficulty in realization of such performance is that the P_r in conventional

ferroelectric insulator material is so high that the hysteresis window become too large for logic applications. However, by using a DE layer for capacitance matching and using an internal metal gate to modulate the area ratio of A_{FE} and A_{DE} if it is needed, we can effectively reduce the hysteresis window, achieve DC enhancement in Fe-FET.

Such experimental structure and experimental results were already reported in our previous publication with A_{FE}/A_{DE} ~ 100, as shown in Ref. 16. It is a MoS_2 ferroelectric-gate FET with internal metal gate structure. Subthreshold slope (SS) of 37.6 mV/dec in forward sweep and SS of 42.2 mV/dec in reverse sweep are achieved. More importantly, a clear I_{ON} enhancement is achieved with same I_{OFF} so that this is an obvious DC enhancement. From the perspective of ferroelectric polarization switching, such DC enhancement can be explained without invoking QSNC concept.

REFERENCES

(1) Sun, F. C.; Kesim, M. T.; Espinal, Y.; Alpay, S. P. Are Ferroelectric Multilayers Capacitors in Series? *J. Mater. Sci.* **2016**, *51*, 499–505.

(2) Tsang, C. H.; Chew, K.-H.; Ishibashi, Y.; Shin, F. G. Structure of Interfaces in Layered Ferroelectrics of First and/or Second Order Transition. *J. Phys. Soc. Jpn*. **2004**, *73*, 3158–3165.

(3) Dawber, M.; Lichtensteiger, C.; Cantoni, M.; Veithen, M.; Ghosez, P.; Johnston, K.; Rabe, K. M.; Triscone, J.-M. Unusual Behavior of the Ferroelectric Polarization in $PbTiO_3/SrTiO_3$ Superlattices. *Phys. Rev. Lett*. **2005**, *95*, 177601.

(4) Zhou, Y. Enhancement of Dielectric and Ferroelectric Properties in Ferroelectric

Superlattices. *Solid State Commun.* **2010**, *150*, 1382–1385.

(5) Salev, P.; Mahayni, A.; Grigoriev, A. Polarization Coupling Transition in $BaTiO_3/PbZr_{0.2}Ti_{0.8}O_3$ Ferroelectric Bilayers. *Phys. Rev. B* **2016**, *93*, 041423.

(6) Hoffman, M.; Pesic, M.; Slesazeck, S; Schroeder, U.; Mikolajick, T. On the stabilization of ferroelectric negative capacitance in nanoscale devices. *Nanoscale* **2018**, *10*, 10891.

(7) Khan, A. I.; Bhowmik, D.; Yu, P.; Kim, S. J.; Pan, X.; Ramesh, R.; Salahuddin, S. Experimental Evidence of Ferroelectric Negative Capacitance in Nanoscale Heterostructures. *Appl. Phys. Lett.* **2011**, *99*, 113501.

(8) Appleby, D. J. R.; Ponon, N. K.; Kwa, K. S. K.; Zou, B.; Petrov, P. K.; Wang, T.; Alford, N. M.; O'Neill, A. Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature. *Nano Lett.* **2014**, *14*, 3864–3868.

(9) Gao, W.; Khan, A.; Marti, X.; Nelson, C.; Serrao, C.; Ravichandran, J.; Ramesh, R.; Salahuddin, S. Room-Temperature Negative Capacitance in a Ferroelectric-Dielectric Superlattice Heterostructure. *Nano Lett.* **2014**, *14*, 5814–5819.

(10) Hoffmann, M.; Max, B.; Mittmann, T.; Schroeder, U.; Slesazeck, S.; Mikolajick, T. Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. In *IEEE Intl. Electron Devices Meet.*; 2018; pp 727–730.

(11) Van Houdt, J.; Roussel, P. Physical Model for the Steep Subthreshold Slope in Ferroelectric FETs. *IEEE Electron Device Lett.* **2018**, *39*, 877–880.

(12) Kittl, J. A.; Obradovic, B.; Reddy, D.; Rakshit, T.; Hatcher, R. M.; Rodder, M. S. On the Validity and Applicability of Models of Negative Capacitance and Implications for MOS Applications. *Appl. Phys. Lett.* **2018**, *113*, 042904.

(13) Kim, Y. J.; Park, H. W.; Hyun, S. D.; Kim, H. J.; Kim, K. D.; Lee, Y. H.; Moon, T.; Lee,

Y. B.; Park, M. H.; Hwang, C. S. Voltage Drop in a Ferroelectric Single Layer Capacitor by Retarded Domain Nucleation. *Nano Lett*. **2017**, *17*, 7796–7802.

(14) Saha, A. K.; Datta, S.; Gupta, S. K. "Negative Capacitance" in Resistor-Ferroelectric and Ferroelectric-Dielectric Networks: Apparent or Intrinsic? *J. Appl. Phys.* **2018**, *123*, 105102.

(15) Obradovic, B.; Rakshit, T.; Hatcher, R.; Kittl, J. A.; Rodder, M. S. Ferroelectric Switching Delay as Cause of Negative Capacitance and the Implications to NCFETs. In *VLSI Tech. Dig.*; 2018; pp 51–52.

(16) Si, M.; Jiang, C.; Su, C.; Tang, Y.; Yang, L.; Chung, W.; Alam, M. A.; Ye, P. D. Sub-60 mV/Dec Ferroelectric HZO MoS_2 Negative Capacitance Field-Effect Transistor with Internal Metal Gate: The Role of Parasitic Capacitance. In *IEEE Intl. Electron Devices Meet.*; 2017; pp 573–576.