Highly Robust All-Oxide Transistors Toward Vertical Logic and Memory

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***Abstract*—In this work, we report atomic-layer-deposited (ALD) based all-oxide transistors toward vertically stacked high-density logic and memory for 3-D integration. This structure utilizes thick degenerated ALD In_2O_3 as the conducting gate, and ALD In_2O_3 thin film itself serves as source/drain contacts to the ALD In_2O_3 channel without metal contacts and gate formation. The all-oxide field-effect transistors (AOFETs) not only survived under high-temperature annealing over 400 °C but also gained a boosted ON-/OFF-ratio over 10^7 with subthreshold swing (SS) close to 60 mV/dec at room temperature. AOFETs present high uniformity and very robust reliability with a threshold voltage instability (ΔV_{TH}) of −5 and −50 mV under positive bias stress (PBS) and negative bias stress (NBS) tests for 10^4 s. The vertical AOFETs (V-AOFETs) demonstrate good gate modulation from sidewall In_2O_3 with thickness as well as gate length ($T_{IO,g}$) of 10 nm, achieving ON-/OFF-ratio over 10^5 and maximum current (I_{max}) over 160 μA/μm. Vertical all-oxide ferroelectric FETs (V-AO-FeFETs) show a memory window (MW) of 1.85 V, with endurance and retention extended to 10^{12} cycles and ten years at room temperature, respectively. These findings illustrate that the vertical-channel all-oxide devices based on ALD oxide semiconductors (OS) are promising candidates for future high-density logic and memory applications in 3-D integration.**

***Index Terms*—All-oxide field-effect transistor (AOFET), atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, ferroelectric field-effect transistor (FeFET), oxide semiconductor (OS), vertical-channel transistor.**

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I. Introduction

THE memory wall problem has bottlenecked the development of artificial intelligence (AI) hardware due to limited capacity and data transfer bandwidth. Promising strategies to overcome this challenge, including near-memory and in-memory computing, demand new memory solutions offering high bandwidth [1], [2]. Thus, these solutions must combine high density and high speed, and be capable of compact integration with high-density logic circuits. Vertical stacking of memory cells and integration with peripheral circuits in the z-direction is one of the most promising solutions. A prime example of this approach is 3-D NAND or V-NAND technologies, which have achieved flash memory cells stacked over 300 layers with vertical channel configuration in 2023 [3]. Despite very high density, NAND technologies face challenges of low speed and limited write/read cycles, which make NAND-based memory unsuitable as the main memory for AI big models. In contrast, mainstream dynamic random access memory (DRAM) and emerging ferroelectric field-effect transistors (FeFETs) have simple cell structure, high speed, and high endurance, making them a strong candidate for the AI's main memory [4], [5], [6], especially if high-density DRAM or FeFETs can be achieved by vertical stacking in the z-direction. Although vertical-channel DRAM and FeFETs have been demonstrated in conventional semiconductors, such as poly-Si and Si/SiGe [7], [8], [9], [10], [11], [12], they usually suffer from challenges including less-ideal sidewall uniformity, a variation on doping profile, high thermal budgets and metal diffusion under high-temperature treatment. In contrast, atomic-layer-deposited (ALD) oxide semiconductors (OS), such as In_2O_3 and $InGaZnO_x$ (IGZO), have been recently noticed as a very suitable channel material for monolithic3-D integration [13], [14], [15], [16], [17], [18], [19], [20], [21], attributing to their good 3-D conformality, wafer-scale uniformity, high current level, low leakage, high bias stability, and with CMOS and back-end-of-line (BEOL) compatibility [22], [23], [24], [25], [26], [27], [28], [29]. While most reports on vertical OS FETs include a metallization process, by replacing conventional elementary metal or nitride metal gate electrodes with thick degenerated In_2O_3, both yield and reliability can be enhanced because of the absence of metal

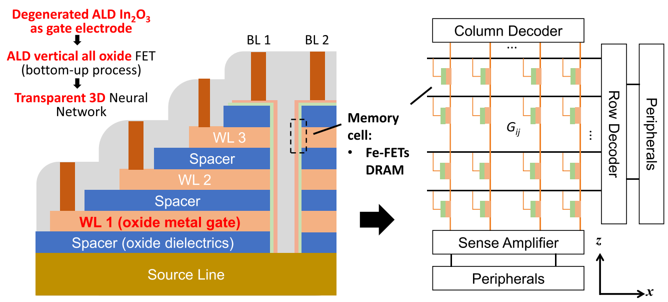

Fig. 1. Motivation of this work: a 3-D vertical array of ALD all-oxide transistors using thick and degenerated ALD In_2O_3 as conducting gate electrodes for the word lines in a vertical array. This design features an all-oxide structure based on ALD. The spacer uses an ALD oxide insulator, and the channel semiconductor uses OS with ultrahigh uniformity and 3-D conformality. Such a process simplifies the fabrication process, enables a very high-density memory cell array, and enhances reliability against metal diffusion.

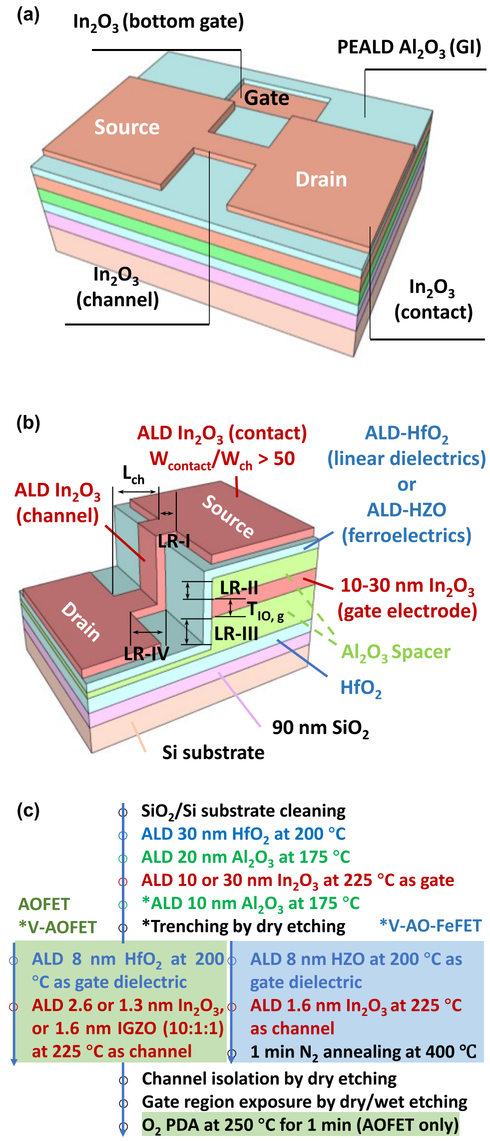

Fig. 2. (a) Schematic device structure of an ALD-based AOFET In_2O_3 bottom-gate thin-film transistor with back gate structure. To ensure a contact-to-channel contrast, the $W_{contact}/W_{ch}$ ratio is over 50. (b) Three-dimensional device schematic of an ALD vertical all oxide FET using HfO_2 as the gate dielectric, or Fe-FET using HZO as GI. LRs: link regions. LR-II and LR-III are link regions from vertical spacer with weak electrostatic control from sidewall In_2O_3 gate; LR-I and LR-IV are link regions from planar In_2O_3 with weaker gate modulation for LR-I and weakest modulation for LR-IV. (c) Fabrication process flow of AOFETs, V-AOFETs, and V-AO-FeFETs based on ALD In_2O_3. The steps with asterisk are special for vertical structures.

diffusion and a great simplification of the process. Meanwhile, the fabricated all-oxide transistors will also be a promising candidate for 3-D neuron networks (NN) in flexible electronics and sustainable electronics, as shown in Fig. 1.

In this work, we report ALD-based all-oxide transistors toward 3-D vertical integration, using degenerated ALD In_2O_3 as conducting gate, and ALD In_2O_3 itself as contact to channel without gate and contact metallization. Such fabricated all-oxide FETs (AOFETs) withstand post-deposition annealing (PDA) in O_2 at 400 °C or more and show high uniformity and enhancement of gate control with ON-/OFF-ratio over 10^7 and subthreshold swing (SS) close to 60 mV/dec at room temperature. All-oxide devices also present robust bias stability with a threshold voltage instability (ΔV_{TH}) of −5 and −50 mV under positive bias stress (PBS) and negative bias stress (NBS) tests. Vertical AOFETs (V-AOFETs) demonstrate effective gate modulation from the sidewall 10 nm degenerated In_2O_3 gate electrode with ON-/OFF-ratio > 10^5 and I_{max} > 160 μA/μm. ALD vertical all-oxide FeFETs (V-AO-FeFETs) exhibit a memory window (MW) of 1.85 V, with a high endurance extended to 10^{12} cycles and long retention extended to ten years at room temperature. This work was originally presented at the 2024 Symposium on VLSI Technology, and this article is an extended version of the article [30].

II. Experimental and Simulation

Fig. 2(a) shows the 3-D device schematic of a planar AOFET with plasma-enhanced ALD (PE-ALD) Al_2O_3 as the gate insulator (GI), and degenerated ALD In_2O_3 of 30 nm as a global back gate. No metal contact is defined, instead, the source/drain and channel of an AOFET are defined by a high contrast between contact width ($W_{contact}$) and channel width (W_{ch}). With $W_{contact}/W_{ch}$ greater than 50, ensures a much higher contrast in the number of modes in the contact region ($M = Wk_F/\pi$, where M is the number of modes, k_F is the Fermi vector and W is the width) [31]. Fig. 2(b) shows the 3-D device schematic of a V-AOFET using ALD HfO_2 as GI or a V-AO-FeFET using ALD $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as GI, with degenerated ALD In_2O_3 of 10 or 30 nm as the sidewall gate electrode to modulate the vertical channel. The definition of source/drain and channel in vertical devices is the same as in AOFETs. The channel length (L_{ch}) is defined as the distance of contact edges projected to the 2-dimensional xy plane.

Fig. 2(c) illustrates the fabrication process flow of AOFETs, V-AOFETs, and V-AO-FeFETs. First, HfO_2 of 30 nm as an adhesion layer to passivate the surface and enhance the quality of the following ALD thin film was deposited by ALD at 200 °C on solvent-cleaned 90 nm SiO_2/p$^+$ Si substrate, followed by Al_2O_3 of 20 nm grown by ALD at 175 °C as the base spacer. Next, In_2O_3 of 30 or 10 nm was deposited by ALD at 225 °C as a back gate electrode for planar AOFETs or sidewall gate electrodes for V-AOFETs and V-AO-FeFETs. 10 or 30 nm thick In_2O_3 is a degenerated semiconductor and very conducting, suitably used as a gate electrode. Next, for vertical devices, Al_2O_3 of 20 nm was grown by ALD at 175 °C as the top spacer, forming an Al_2O_3-In_2O_3-Al_2O_3 stack, followed by dry etching to create a 40-nm deep trench for conformal deposition of ALD In_2O_3 as a vertical channel. These two steps special for vertical structures are highlighted with an asterisk. Next, GI and channel semiconductors were deposited in sequence. For AOFETs and V-AOFETs, Al_2O_3 of 5 nm deposited by PEALD and HfO_2 of 8 nm deposited by ALD at 200 °C serve as the GI, respectively. In_2O_3 of 2.6 and 1.3 nm was deposited subsequently by ALD at 225 °C as the channel for AOFETs and V-AOFETs, respectively. For V-AO-FeFETs, HZO of 8 nm was grown by ALD at 200 °C as the ferroelectric GI followed by In_2O_3 of 1.6 nm using ALD as the channel semiconductor. The whole In_2O_3-HZO-In_2O_3 structure on the sidewall was annealed subsequently in N_2 at 400 °C for 1 min to form a ferroelectric phase in HZO. For ALD precursors, PEALD Al_2O_3 uses $Al(CH_3)_3$ (TMA) and O_2 plasma with the plasma power of 300 W as Al and O precursors, separately; ALD HZO uses $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr) and H_2O as Hf, Zr and O precursors, respectively; ALD In_2O_3 uses $(CH_3)_3$ In (TMIn) and H_2O as Al and O precursors, respectively.

After material preparation, channel isolation and definition of source/drain and channel were patterned by e-beam lithography and etched by reactive ion etching (RIE), followed by gate pad exposure by RIE. Finally, a PDA in the O_2 atmosphere at various temperatures is applied to tune the threshold voltage (V_{TH}) and improve the oxide-to-oxide interface quality of the devices.

The dc and ultrafast electrical characterizations at room temperature were performed in a Cascade probe station in an atmosphere under N_2 ambient. DC characterization uses the Keysight B1500A system, and the ultrafast characterization uses the Agilent B1530A system with waveform generator/fast measurement units for the reliability test of FeFETs. The temperature-dependent characterization (10–295 K) was performed in a Lakeshore CRX-VF cryogenic probe station. The threshold voltages are determined by the linear extrapolation at maximum transconductance ($g_{m,max}$) method from transfer characteristics.

TCAD modeling is utilized for electrical simulations using the Sentaurus device simulator, which self-consistently solves the Poisson equation along with the current continuity equations. The density gradient model was used to account for the quantum confinement at nanoscale dimensions and the thin layer mobility model for ultra-scaled channel thickness.

III. Results and Discussion

A. All-Oxide Field-Effect Transistors

To assess the feasibility and potential impact on the performance of the all-oxide process, planar AOFETs were investigated as a reference. Fig. 3(a) shows the transfer characteristics in logarithmic scale at V_{DS} of 0.1 and 1.0 V of 30 planar AOFETs randomly picked from four 5 × 5 mm dies, with W_{ch} of 1 μm, L_{ch} of 2 μm, channel thickness (T_{ch}) of 2.6 nm, and without PDA treatment. A set of typical I_{DS}–V_{GS} characteristics at V_{DS} of 0.1 and 1.0 V from a single device are also plotted in linear scale. Devices show an ON-/OFF-ratio of 10^6 at V_{DS} of 1 V. The OFF-state I_{DS} is primarily from gate-to-drain leakage because of the large overlap area between the contact pad and the back gate. The high ON-/OFF-ratio demonstrates the strong electrostatic control from a thick In_2O_3 gate over a thin In_2O_3 channel via GI. The good linearity in the ON-state also illustrates the feasibility of ALD-based all-oxide transistors using a metal-free source/drain process and with degenerated ALD In_2O_3 as the gate electrode. Thirty devices randomly measured also show a low device-to-device variability for an all-oxide process. However, an AOFET without PDA treatment still suffers from a deeply negative V_{TH}, and a large SS. Fig. 3(b) shows the evolution of transfer characteristics of AOFETs at V_{DS} of 0.1 V, with PDA treatment in O_2 atmosphere for 1 min at various temperatures from 400 °C to 490 °C. An AOFET with W_{ch} of 1 μm, L_{ch} of 2 μm, and T_{ch} of 2.6 nm shows a positive V_{TH} shift over 1 V and reduced SS under high-temperature PDA treatment over 400 °C. An AOFET shows an enhancement on the ON-/OFF-ratio for two orders of magnitude to over 10^7 at V_{DS} of 0.1 V, with PDA of 400–450 °C. The reduction in the ON-/OFF-ratio with PDA of 490 °C is because of GI degradation with higher leakage. The transistors present a reduction in maximum current I_{max} under high-temperature PDA, which is mainly because of an increase in V_{TH}. While the ON-current I_{ON} at V_{GS}–V_{TH} of 1 V degrades slightly, which rules out the possibility of severe degradation of contact resistance. However, there is a minor degradation

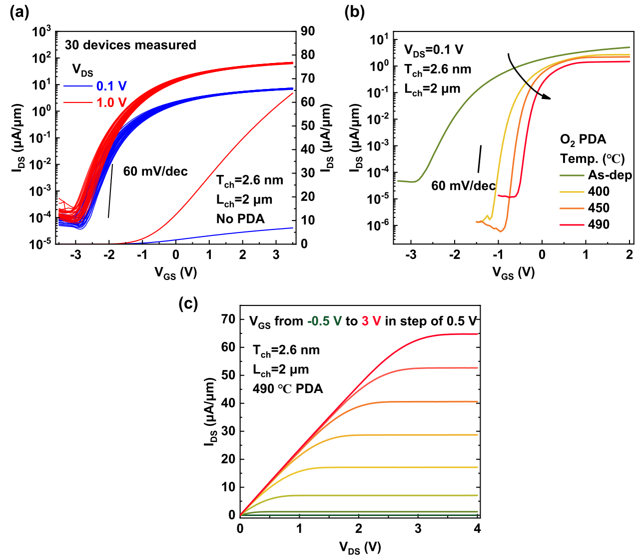

Fig. 3. (a) I_D–V_{GS} characteristics at V_{DS} of 0.1 and 1.0 V of 30 planar AOFETs randomly picked from four 0.5 × 0.5-cm dies, with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm and without PDA treatment. Thirty AOFETs are randomly picked from four 0.5 × 0.5-cm dies. (b) Evolution of I_{DS}–V_{GS} characteristics of AOFETs with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm, and with various PDA treatment conditions for no PDA, PDA at 400 °C, 450 °C, and 490 °C. (c) I_D–V_{DS} characteristics of an AOFET with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm, and PDA at 490 °C.

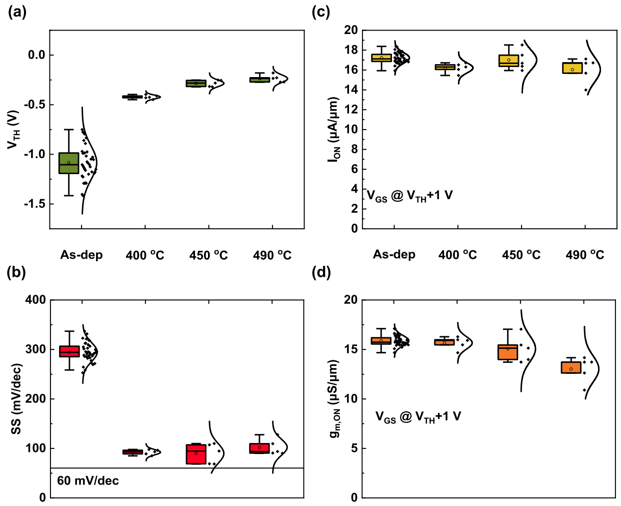

Fig. 4. Statistical plots of (a) V_{TH}, (b) SS, (c) I_{ON} at V_{GS} of $V_{TH}+1$ V, and (d) $g_{m,ON}$ at V_{GS} of $V_{TH}+1$ V for AOFETs with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm, and with various PDA treatment condition as a comparison. PDA conditions: no PDA (as deposited), and PDA at a temperature from 400 °C to 490 °C.

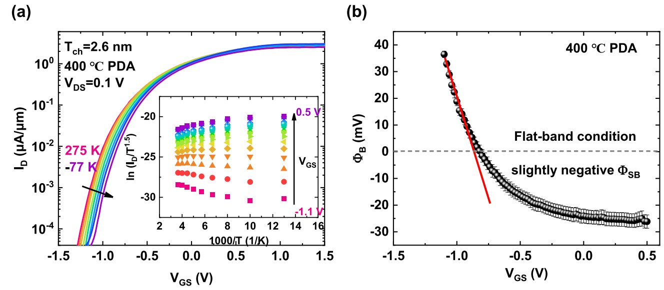

Fig. 5. (a) Temperature-dependent I_D–V_{DS} characteristics of an AOFET with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm, and PDA at 400 °C, from 275 to 77 K. Inset: Arrhenius plot of $\ln(I_D/T^{1.5})$ versus $1/T$ at different gate biases. (b) Extracted Φ_B as a function of V_{GS} from the slope of the Arrhenius plot at each V_{GS}. Φ_{SB} is extracted at flat-band condition.

of contact resistance (R_c) with a drop of charge density or lowering E_F level after O_2 treatment [29]. Fig. 3(c) shows the output characteristics of planar AOFETs with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm, and PDA at 490 °C. The device shows a good saturation behavior with $I_{D,SAT}$ of 67 μA/μm at V_{DS} of 4 V and V_{GS} of 3 V.

Fig. 4(a)–(d) presents the statistical distribution of V_{TH}, SS, I_{ON} at V_{GS} of $V_{TH}+1$ V and ON-state transconductance ($g_{m,ON}$) at V_{GS} of $V_{TH}+1$ V, respectively, demonstrating a comparison of various PDA conditions for AOFETs with W_{ch} of 1 μm, L_{ch} of 2 μm, T_{ch} of 2.6 nm. PDA conditions are listed as no PDA (as deposited) and PDA in O_2 environment from 400 °C to 490 °C. The V_{TH} of AOFETs shifts positively and approaches 0 V (enhancement mode) with a big reduction in deviation with high-temperature PDA in O_2. SS also drops significantly from over 300 to approaching 60 mV/dec with tighter distribution after high-temperature PDA in O_2. Although O_2 treatment decreases charge density without gating, the ON-state performance of AOFETs does not degrade significantly. Both I_{ON} and $g_{m,ON}$ only have less than a 10% reduction with an increase in deviation. This demonstrates a process-robust degenerated In_2O_3 gate electrode and metal-free source/drain contacts, implying the superiority of the all-oxide process over the metallization process for building OS-TFTs under high-temperature treatment, due to the absence of interface degradation from metal diffusion. The flattening in transfer curves and transconductance collapse in high V_{GS} may be due to the access resistance between the source/drain pad and channel with different number of modes.

ALD In_2O_3 with Ni metal contact features a very low R_c approaching the quantum limit, because of a negative Schottky barrier (Φ_{SB}) induced by surface accumulation [32]. In an AOFET, the probe tips are directly in contact with a wide-area In_2O_3 pad as a contact. Although the robustness of devices is significantly enhanced with the all-oxide process compared to the metallization process, the extent to which the contact quality is degraded, particularly under high-temperature annealing, remains unclear. Fig. 5(a) plots the temperature-dependent transfer curves from 275 to 77 K of an AOFET with T_{ch} of 2.6 nm and PDA at 400 °C, at V_{DS} of 0.1 V. The AOFET shows a continuously positive V_{TH} shift. The inset of Fig. 5(a) shows the Arrhenius plots of $\ln(I_D/T^{1.5})$ versus $1/T$ at various gate biases [29]. At a relatively high-temperature range (from 295 to 150 K), the Arrhenius plots are linear with a slope, which undergoes a gradual transition from negative at lower gate voltages to positive at higher V_{GS}. The dependence of effective barrier height (Φ_B) on V_{GS} can be extracted from the slope of the Arrhenius plot at each V_{GS} using the following equation, as shown in Fig. 5(b):

$$I_D = A^*_{2D} T^{1.5} \exp\left(-\frac{\Phi_B}{k_B T}\right). \tag{1}$$

From Fig. 5(b), the Φ_{SB} is determined to be slightly negative at flat-band conditions, where the gate-dependent Φ_B first deviates from a linear dispersion as Φ_B evolves from positive to negative. This illustrates a robustly good contact quality for an AOFET even without S/D metallization and with high-temperature annealing. It is worth noting that (1) is based on the thermal emission model of electrons over a barrier. Thus, the barrier extraction is invalid when the barrier height is negative. However, the extraction of barrier and linear extrapolation in the positive range is still valid in Fig. 5(b). Besides, the deviation from the linearity at lower temperatures and the positive slope at high V_{GS} bias in the Arrhenius plot, as shown in the inset of Fig. 5(a), suggests the presence of a negative Schottky barrier.

Reliability is a crucial factor for whatever potential applications of AOFETs. Fig. 6(a) and (b) presents the evolution of I_D–V_{GS} curves of AOFETs at V_{DS} of 50 mV, with PDA at 490 °C under instability tests of PBS under gate stress bias ($V_{G,stress}$) of 3 V and NBS under $V_{G,stress}$ of −3 V for 10^4 s at 25 °C, respectively. Under the PBS test, the transfer curves show a negligible shift, with a ΔV_{TH} of only −5 mV for 10^4 s. While in the NBS test, ΔV_{TH} degrades faster for −50 mV. The small V_{TH} instability, especially under positive overdrive conditions, comes from the annealing of the donor-like traps under high-temperature O_2 treatment [28],

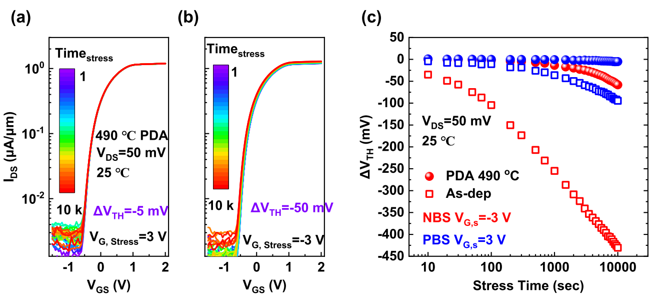

Fig. 6. (a) Evolution of transfer curves at V_{DS} of 50 mV of an ALD AOFET with PDA at 490 °C under (a) PBS with $V_{G,stress}$ of 3 V and (b) NBS with $V_{G,stress}$ of −3 V for 10^4 s. (c) Time evolution of ΔV_{TH} of AOFETs with no PDA and PDA at 490 °C under PBS and NBS for 10^4 s.

demonstrating a high reliability of the oxide-oxide-oxide gate-stack in AOFETs. Fig. 6(c) shows the extracted ΔV_{TH} over stress time for AOFETs with and without high-temperature PDA in O_2 at 25 °C. AOFETs obtain a significant improvement for both PBS and NBS performance from PDA. These results imply the AOFETs, featuring a novel oxide-oxide-oxide MOS gate-stack, are a good candidate for a highly robust vertical structure.

B. Vertical All-Oxide FETs

The study on the vertical structure started with V-AOFETs for high-density logic applications with the device structure shown in Fig. 2(b). Fig. 7(a) shows the high-resolution transmission electron microscopy (HRTEM) with the energy dispersive x-ray spectroscopy (EDS) mapping for the cross section view of an ALD-based V-AOFET with In_2O_3 channel thickness ($T_{IO,ch}$) of 1.3 nm and In_2O_3 gate thickness ($T_{IO,g}$) of 10 nm. From both HRTEM and EDS mapping, it is clear to see the 10 nm In_2O_3 gate, as evident with the thick red layer in EDS mapping image, between two Al_2O_3 spacer layers, which can control the atomically thin In_2O_3 channel, as evident with the thin red conformal layer in EDS mapping, on the side wall through the 8 nm HfO_2 gate dielectric, as evident with blue conformal layer. This illustrates a vertical all-oxide structure using the conformality nature of ALD. The In_2O_3 region was broadened in the EDS image due to indium diffusion by an intense electron beam. A thick ALD Al_2O_3 layer is encapsulated on top to protect the structure under focus ion beam (FIB) sample preparation.

Fig. 7(b) presents a typical transfer characteristic of a V-AOFET with $T_{IO,ch}$ of 1.6 nm, L_{ch} of 16 μm, and $T_{IO,g}$ of 10 nm, at V_{DS} of both 0.1 and 1.0 V for logarithmic scale, and V_{DS} of 0.1 V for linear scale. Both experimental and simulation results are shown in logarithmic scale with good agreement in both sub-threshold and linear regions at V_{DS} of 0.1 and 1.0 V. The device exhibits an ON-/OFF-ratio greater than 10^5, illustrating an effective electrostatic control from degenerated ALD In_2O_3 gate electrode over sidewall GI on the ALD In_2O_3 vertical channel. Compared with the transfer characterization of a planar AOFET as shown in Fig. 4(a), a V-AOFET has a lower ON-state current level and shows saturation with a reduction of g_m when the gate bias is high. Other than a

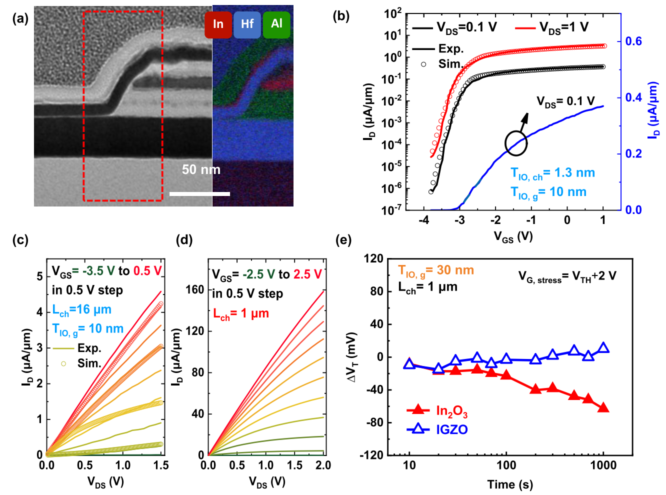

Fig. 7. (a) HRTEM cross section image with EDS mapping of an ALD V-AOFET with $T_{IO,g}$ of 10 nm. A thick ALD Al_2O_3 layer is encapsulated on top to protect the structure under FIB preparation. (b) Experimental and simulated transfer characteristics of a V-AOFET with L_{ch} of 16 μm, $T_{IO,ch}$ of 1.3 nm, and $T_{IO,g}$ of 10 nm. (c) Experimental and simulated output characteristics of the same V-AOFET as (b) and (d) experimental output characteristics of a V-AOFET with L_{ch} of 1 μm, $T_{IO,ch}$ of 1.3 nm, and $T_{IO,g}$ of 10 nm. (e) Time evolution of ΔV_{TH} of V-AOFETs with L_{ch} of 1 μm and $T_{IO,g}$ of 30 nm based on In_2O_3 and IGZO under PBS test for 10^3 s with $V_{G,stress}$ of $V_{TH} + 2$ V.

relatively long L_{ch} of 16 μm to decrease the current level, the performance degradation is mainly because of the resistance of the link region on both sides of the V-AOFET, as illustrated in Fig. 2(b). Each link region resistance comprises two parts: one is the side wall vertical transistors on the two spacer layers (LR-II or LR-III), which has a less effective gate modulation due to a much lower gate-to-channel capacitance. Another is the planar resistance linked with source/drain pads (LR-I or LR-IV), which has very ineffective electrostatic control, especially on the downstream side of the vertical structure (LR-IV). At the ON-state, the resistance of the V-AOFET channel is much lower than that of the two link regions, where V_{DS} drops mostly in, thus the current level is pinned by link regions. While at the OFF-state with low V_{GS}, the V-AOFET turns off earlier than its link regions, so that the resistance of the V-AOFET is much higher than that of the link regions. Thus, the V_{TH} is determined by the active V-AOFET channel.

Fig. 7(c) and (d) shows the output characteristics of V-AOFETs with $T_{IO,ch}$ of 1.6 nm, $T_{IO,g}$ of 10 nm, and L_{ch} of 16 and 1 μm, respectively. Fig. 7(c) also includes the simulated I_D–V_{DS} results. In this work, the maximum current (I_{max}) achieved in a V-AOFET with L_{ch} of 1 μm is 160 μA/μm, much greater than that of the 4.5 μA/μm in a V-AOFET with L_{ch} of 16 μm. This enhancement implies that by reducing planar link regions through L_{ch} scaling, the ON performance can be significantly improved. Device simulation confirms the experimental observation and points out the stronger modulation of the link resistance on the source side (LR-I and II) versus the drain side (LR-III and IV) shown in Fig. 2(b) with the asymmetric source/drain by the nature of vertical device design.

TABLE I
BENCHMARK OF FE-HFO_2 BASED VERTICAL-CHANNEL FEFETS WITH VARIOUS CHANNEL SEMICONDUCTORS AND GATE MATERIALS

	Channel material	Gate metal	MW (V)	L_g (nm)	If Transparent	Endurance (cyc.)	Meas. Retention
This work	ALD In_2O_3	ALD In_2O_3	1.85	30	Yes	$>10^9$	$>10^3$ s
[9]	poly-Si	n poly-Si	2	50	No	$>10^4$	$>10^3$ s
[10]	n poly-Si	p poly-Si	3	50	No	10^5	$>3\times10^5$ s
[11]	SiGe	TiN/W stack	2.3	39.5	No	$>10^3$	$>10^4$ s
[18]	$InZnO_x$	TiN	2	100	No	$>10^8$	NA
[20]	InO_x	n^+ Si	1.3	50	No	$>10^4$	$>2\times10^3$ s

NA: Not applied

Reliability performance is also crucial for V-AOFETs, especially stacked in monolithic 3-D configurations. Besides annealing the devices in the O_2 atmosphere, doping In_2O_3 with Ga or Zn to form IGZO can also reduce the concentration and generation rate of donor-like traps, especially under PBS bias [33]. Fig. 7(e) shows the evolution of V_{TH} instability ΔV_{TH} over 10^3 s under PBS condition, with a V_{GS} overdrive of 2 V ($V_{G,stress} = V_{TH} + 2$ V) on V-AOFETs, highlighting a comparison between In_2O_3 and IGZO channel. V-AOFETs have $T_{IO,g}$ of 30 nm and L_{ch} of 1 μm, without PDA treatment. Compared with In_2O_3, the IGZO channel presents a higher stability under the same bias conditions. However, it comes with a cost of ON-state performance degradation, which is because the IGZO channel intrinsically has lower carrier concentration and higher resistance, resulting in a higher link region resistance of the IGZO channel, pinning ON-state current more than that in the In_2O_3 channel.

C. Vertical All-Oxide Ferroelectric FETs

Vertical-channel FeFETs are promising toward high-bandwidth memory with low power consumption. The vertical all-oxide structure can also enable high-performance Fe-FETs with a potentially low footprint, low thermal budget, and high reliability. In a traditional HZO-based FeFET using silicon or OS, at least one side of metal, including elementary metal such as W and Pt, or nitride metal such as TiN and WN, should serve as the capping layer to provide strain to stabilize the orthorhombic phase of HZO. But in this work, a metal-ferroelectric-semiconductor (MFS) structure with a novel oxide-oxide-oxide material configuration is achieved.

Fig. 8(a) demonstrates a typical bi-directional transfer characteristic at V_{DS} of 0.2 V of a V-AO-FeFET with $T_{IO,ch}$ of 1.6 nm, L_{ch} of 1 μm, W_{ch} of 1 μm, and $T_{IO,g}$ of 30 nm, and with PDA of O_2 at 300 °C. The device shows a counterclockwise hysteresis loop with a MW of 1.85 V. These results confirm the effective gate modulation on V_{TH} by ferroelectric polarization switching, which demonstrates a good and uniform ferroelectricity of the sidewall HZO sandwiched by thick In_2O_3 and thin In_2O_3 capping layers and annealed under 400 °C with BEOL compatibility. Fig. 8(b) and (c) shows the endurance and retention of a V-AO-FeFET on the same batch as Fig. 8(a), and with PDA on O_2 at 300 °C. In the endurance test, ultrafast erase and program pulse of −4 and 3.5 V are utilized to switch ferroelectric polarity in HZO, respectively, with rise/fall time (RT) of 200 ns and pulsewidth (PW) of 250 ns.

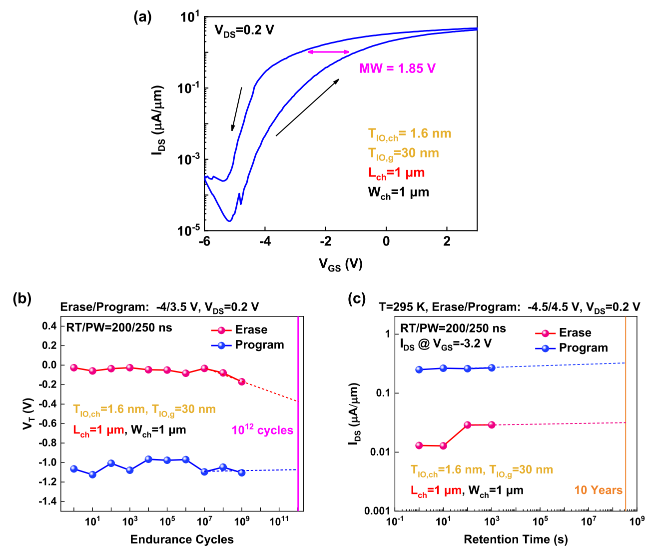

Fig. 8. (a) Bi-directional I_D–V_{GS} characteristics of an ALD V-AO-FeFET with W_{ch} of 1 μm, L_{ch} of 1 μm, $T_{IO,ch}$ of 1.6 nm, and $T_{IO,g}$ of 30 nm at V_{DS} of 0.2 V. (b) Endurance and (c) retention of the same batch of V-AO-FeFETs as (a) and with PDA on O_2 at 300 °C. The reliability test of all V-AO-FeFETs was performed at room temperatures using pulse and ultra-fast I–V scheme, and the PW and RT of each program and erase pulse are 250 ns and 200 ns, respectively.

V_{TH} is extracted from the ultra-fast I–V characterization to minimize measurement-induced V_{TH} shift [34]. The endurance performance was measured up to 10^9 cycles, maintaining a MW over 1 V, and without significant V_{TH} shift. A reduction of MW from 1.85 V in dc IV to 1 V in ultra-fast IV with program and erase pulses is primarily because of ultra-short pulse duration to switch domain polarity. The endurance cycle can be extended to 10^{12} cycles at room temperature. In the retention test, ultrafast erase and program pulse of −4.5 and 4.5 V are utilized to switch ferroelectric polarity in HZO, respectively. The retention time was measured to 1000 s and can be extended to ten years. Besides the high-quality oxide-oxide-oxide interface, the robust endurance and retention performance of V-AO-FeFETs also come from a high carrier or space charge concentration at a positive or negative bias of the ALD In_2O_3 channel which E_F pinned inside the conduction band, meeting the charge balance conditions required by HZO switches. It significantly lowers the depolarization field which is hard to realize in conventional semiconductor channels. These results also demonstrate the vertical structure supports the high reliability of the HZO-OS ferroelectric system. And because of the metal-free process, the V-AO-FeFETs likely avoid degradation from metal interdiffusion for long-term reliability when integrated with other circuit components.

Although vertical-channel FeFETs based on HZO were demonstrated in previous works using poly Si, Si/Ge, and OS as channel material, the V-AO-FeFETs in this work enable significant enhancements in reliability performance, especially in endurance, as highlighted in the benchmark in Table I. Moreover, the transparency and flexibility of OS and degenerated In_2O_3 gate expand the application field of V-AO-FeFETs. A current drawback of vertical structure is the degradation of ON-state performance due to the resistance from link regions. However, this issue can be mitigated by L_{ch} scaling, particularly when integrating V-AOFETs or V-AO-FeFETs in 3-D with multiple layers. In such a configuration, the resistance from the two planar link regions becomes less significant as its impact is diluted across multiple layers.

IV. Conclusion

In conclusion, this work demonstrates an ALD-based all-oxide structure with high robustness toward 3-D vertical integration. The thick degenerated ALD In_2O_3 are used as gate electrodes for both planar and vertical transistors for the first time. Additionally, In_2O_3 itself is used as a contact with a slightly negative Φ_{SB}. The total fabrication process flow is free from metallization and is both CMOS and BEOL compatible. The robust AOFETs after high-temperature PDA achieve ON-/OFF-ratio over 10^7, SS close to 60 mV/dec, and high bias stability with ΔV_{TH} less than $-5/-50$ mV for 10^4 s, demonstrating a high-quality oxide-oxide-oxide interfaces and an effective gate modulation from degenerated In_2O_3 gate. The V-AOFETs also demonstrate good electrostatic control from the sidewall In_2O_3 gate electrode with ON-/OFF-ratio over 10^5 and I_{max} over 160 μA/μm. V-AO-FeFETs exhibit a MW of 1.85 V, an endurance measured to 10^9 cycles and extended 10^{12} cycles, and long retention extended to ten years. This work demonstrates that vertical all-oxide devices are good candidates for memory and logic cells toward future 3-D high-density ICs.

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