First Demonstration of BEOL Wafer-Scale All-ALD Channel CFETs Using IGZO and Te for Monolithic 3D Integration

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***Abstract*—** In this work, we demonstrated for the first time Back-End-Of-Line (BEOL) compatible complementary field-effect transistors (CFETs) with wafer-scale all atomic-layer-deposited (ALD) channels for monolithic 3D integration. A p-type transistor based on Tellurium (Te)/Tellurium oxide (TeO_x) heterostructure was fabricated on top of an InGaZnO (IGZO) n-type transistor using a common gate structure. An excellent IGZO device performance was achieved with an on-current (I_{on}) of 1 mA/μm at V_{ds}=1 V in an enhancement-mode operation with a channel thickness (T_{ch}) of 2 nm. The uniform wafer-scale growth of p-type semiconductor Te was achieved by introducing methanol in ALD process. Transistor arrays were measured on a four-inch wafer, demonstrating good uniformity and yield based on statistical electrical characterization. The ALD CFET-inverters were fabricated and confirmed by cross-sectional scanning transmission electron microscopy (STEM). They exhibit good electrical performance with a high gain of 116.5 V/V and a large noise margin of 2.2V (88%) at V_{DD} = 5 V. The thermal budget of the entire ALD-CFET fabrication process is 225 ºC and BEOL compatible.

I. Introduction

In the rapidly evolving landscape of semiconductor technology, achieving higher performance while maintaining compatibility with existing manufacturing processes is paramount. BEOL-compatible CMOS technology for monolithic 3D integration emerges as a compelling solution for advancing chips with higher transistor densities, reduced power consumption, enhanced functionality, scalability, and cost efficiency. Recently, ALD InO_x-based oxide semiconductors (including Zn and Ga doping) [1] has garnered significant interest due to its ultrathin channel thickness, superior electrical performance [2], ultra-low contact resistance [3], and robust bias stabilities [4]. The wafer-scale conformal growth achievable through ALD at low processing temperatures positions ALD channel materials well as the promising candidates for BEOL monolithic 3D integrations.

CFETs (Fig. 1), integrated vertically to minimize the footprint of CMOS transistors along with BEOL compatibility, offer an alternative path for scaling semiconductor devices. Traditionally, the scalability of BEOL-compatible p-type semiconducting channel materials with wafer-scale production has been limited. This paper explores the use of ALD TeO_x/Te heterostructure [5, 6] as a novel p-type semiconductor channel, paired with ALD IGZO as a n-type semiconductor channel, to construct CFETs with wafer-scale BEOL compatibility.

We highlight this work as the first demonstration of BEOL-compatible CFETs with all ALD semiconducting channels (Fig. 2). We developed a stacking process of vertically integrated p-type Te channels on top of IGZO transistors paving the way for future monolithic 3D integration. The 2-nm-thick IGZO n-type transistors, post-stacking, exhibit excellent performance, with an on-current of 1 mA/μm at V_{ds} = 1 V and enhancement-mode operation. Using ALD TeO_x/Te heterostructure, p-type transistor arrays were fabricated and measured on a four-inch wafer, with statistical analysis of 300 devices demonstrating the uniformity of the ALD Te film. Furthermore, ALD-CFET inverters were fabricated and verified by cross-sectional STEM, featuring vertically-integrated channel-dielectric-metal-dielectric-channel stacks. These inverters show outstanding performance, with a gain of 116.5 V/V and a noise margin of 2.2V (88%) at V_{DD} = 5 V. Our work presents a new approach for BEOL CMOS development with CFET structure and novel channel materials.

II. Experiments

The ALD-CFET fabrication starts with top-gate IGZO n-type devices (Fig. 3). An 8-nm-thick ALD HfO_2 adhesion layer was deposited using $[(CH_3)_2N]Hf$ (TDMAHf) and H_2O at 200 ºC after the solvent cleaning of 90 nm SiO_2/Si substrate. The 2 nm IGZO (10:1:1) was deposited by ALD at 225 ºC using $In(CH_3)_3$, $(C_2H_5)_2Zn$, and $Ga_2(NMe_2)_6$ as precursors. The thickness of the IGZO layer is controlled by depositing 7 super-cycles which contains the sequential deposition of ZnO, Ga_2O_3, and 10 cycles of In_2O_3. 30 nm/20 nm Ni/Pd was deposited by e-beam evaporation as source/drain contact metals after channel isolation by dry etching. An 8-nm-thick HfO_2 top-gate dielectric for IGZO channel was deposited by plasma-enhanced ALD (PEALD) at 150 ºC, followed by the deposition of 20 nm/20 nm Ni/Pd as the common gate metal, which also serves as the gate for top-layer p-type transistors. An 8-nm-thick HfO_2 bottom-gate dielectric for Te channel was then deposited using PEALD at 150 or 200 ºC. ALD TeO_x/Te film was newly developed as a novel BEOL p-channel material so that it was investigated on different substrates: previously fabricated IGZO n-type transistors for CFETs, SiO_2 fin structures, and four-inch 90 nm SiO_2/Si wafer. ALD TeO_x was grown using $Te(OEt)_4$ and H_2O. ALD Te was grown using $Te(SiMe_3)_2$ (BTMS-Te), $Te(OEt)_4$, and MeOH. The growth temperature is optimized at 80 ºC. Optional via opening was performed using dry etching. 40 nm Ni was deposited as source/drain metal contacts followed by the channel isolation using dry etching.

Scanning electron microscope (SEM), high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), and energy dispersive x-ray spectroscopy (EDS) elemental mappings were used to characterize and confirm the CFET stack structure and material composition. The low temperature characterization was performed in a Lakeshore CRX-VF cryogenic probe station. The electrical characterization of transistors and inverters was measured with the Keysight B1500 system in a Cascade probe station.

III. Results and Discussion

The top-gate n-type IGZO transistors were characterized after the deposition of dielectrics for p-channel. Figs. 4 and 5 present the typical transfer and output characteristics of an enhancement-mode short-channel IGZO FET with a channel length (L_{ch}) of 100 nm, showing a threshold voltage (V_t) of 0.04 V determined by linear extrapolation method. At V_{ds} = 1 V, it achieves a high on-current (I_{on}) of 1 mA/μm and an I_{on}/I_{off} ratio of 10^{10}. Figs. 6 and 7 show the transfer and output characteristics of a long-channel device with L_{ch} of 1 μm, demonstrating good current saturation at high V_{ds}. The IGZO film thickness is 2 nm and the dielectric thickness of HfO_2 is 8 nm. Fig. 8 illustrates transfer curves of various channel lengths, with threshold voltage and subthreshold swing extracted and summarized in Fig. 9. At longer channel (0.5 to 1 μm) devices, the SS approaches 60 mV/dec, indicating a clean oxide (semiconductor) – oxide (dielectric) interface. The threshold voltage shifts positively with increasing channel length. Post-processing temperatures (150 or 200 ºC during deposition of the 8-nm-thick dielectric for p-channel) slightly affect the properties of the underlying n-type IGZO layer, with higher temperatures resulting in a lower threshold voltage for IGZO devices. After the process optimization, the p-channel fabrication has minor effect on n-channel devices in general.

Fig. 10 illustrates the fabrication process flow for TeO_x/Te p-type transistors. This heterostructure can be grown on various substrates, including IGZO n-type transistors. Detailed ALD sequences are shown in Fig. 11. The TeO_x layer acts as a connection between HfO_2 dielectric and the semiconducting Te, facilitating conformal wafer-scale growth. The introduction of MeOH provides precursor coverage by *in-situ* formation of TeH_2. Fig. 12 (a, b) shows the Raman spectrum of TeO_x and Te, respectively, revealing their material composition. Fig. 12 (c, d) shows the cross-sectional STEM image and EDS elemental mapping of TeO_x/Te grown on 3D SiO_2 fin structures fabricated by SEMATECH with a fin height of 180 nm and fin pitch of 130 nm. EDS elemental mapping confirms the conformal Te coating on the fin structure, highlighting the conformality and uniformity of the ALD process.

Fig. 13 shows the photograph of transistor arrays fabricated on a four-inch wafer with 14-nm-thick ALD TeO_x/Te heterostructure. The transfer curves of 300 devices with the channel length of 6 μm from transistor arrays of 52 dies on a four-inch wafer are presented in Fig. 14, indicating the consistent electrical performance across the whole wafer. Fig. 15 and 16 present the spatial color map of the transistor conductivity at V_{gs} = -60 V and the I_{on}/I_{off} ratio, respectively. The I_{on}/I_{off} ratio is about 10^3 across the wafer indicating the uniformity of the TeO_x/Te film and meanwhile a 0.35 eV narrow bandgap of Te film. Fig. 17 and 18 show the length-dependent transfer characterizations and scaling properties of p-type TeO_x/Te transistors fabricated on top of IGZO n-type transistors with 8-nm-thick HfO_2 as bottom gate at 33 K. The I_{on}/I_{off} ratio of Te transistors can be significantly increased to 10^6-10^7 at cryogenic temperatures. The contact resistance of these Te transistors is decent, higher than that of n-type contacts.

Furthermore, ALD-CFET inverters were fabricated with TeO_x/Te as the top p-FET and IGZO as the bottom n-FET, as illustrated in Fig. 19(a). The cross-sectional STEM image and EDS elemental mapping of the vertical material stack at the source/drain region are shown in Fig. 19(b). The two channels are separated by a shared metal gate and two dielectric layers of 8-nm-thick HfO_2, with a spacing of approximately 60 nm between p- and n-channels. Fig. 20 shows an SEM image of the top view of an ALD-CFET, with p-FET vertically stacked on top of n-FET. Fig. 21 depicts the voltage transfer characteristic (VTC) of the ALD-CFET at various V_{DD} from 1 V to 5 V, exhibiting a full-output-swing behavior. The mid-point voltage can be tuned by adjusting the threshold voltage, which is achievable by varying the channel thickness and doping concentrations. The inverter gain is extracted at different V_{DD} as shown in Fig. 22. A high gain of 116.5 V/V is achieved at V_{DD} = 5 V. Fig. 23 shows the butterfly curve of the ALD-CFET inverter, where a high noise margin of 2.2 V (88%) at V_{DD} = 5 V is extracted using the largest possible square method, demonstrating its potential for realizing SRAM. The large gain and noise margin indicates high-performance CMOS achievable by the ALD-CFETs. Table-1 benchmarks the state-of-the-art monolithic 3D CMOS inverters using oxide semiconductors and 2D materials [7-12]. Our work stands out as the first all ALD-CFET with a low process temperature of 225 ºC and a high gain of 116.5 V/V.

IV. Conclusion

In conclusion, this work demonstrates the first BEOL-compatible all ALD channel CFET with 60 nm p- and n-channels spacing using a common gate structure, high-performance enhancement-mode IGZO n-type transistors, wafer-scale growth of TeO_x/Te p-type channel material, and high-performance CFET inverter (116.5 V/V gain, 2.2V (88%) noise margin). Our work provides the promise for considering novel ALD channel materials as BEOL-compatible CMOS technologies for monolithic 3D integration.

Acknowledgment

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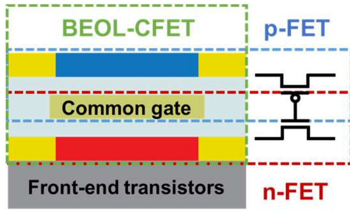

Fig. 1. Device schematic of a BEOL-CFET using a common gate structure.

Highlights of this work.

- First demonstration of BEOL all-ALD channel CFET using IGZO and TeO_x/Te.
- ALD-growth of wafer-scale TeO_x/Te p-type channel and wafer-scale device
- Enhancement mode IGZO top gate devices with 1 mA/μm on-current at V_{ds} = 1 V.
- CFET inverter with a high gain of 116.5 V/V and a high noise margin of 88%.

Fig. 2. Highlights of this work including BEOL IGZO and Te, wafer-scale ALD, CFET inverter demonstration.

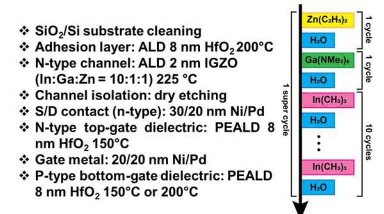

Fig. 3. Fabrication process flow of top-gate IGZO n-type transistor and ALD sequences.

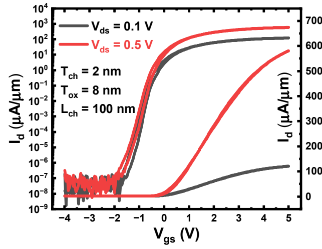

Fig. 4. Transfer characteristics of an IGZO FET with the L_{ch} of 100 nm at V_{ds}=0.1V and 0.5V.

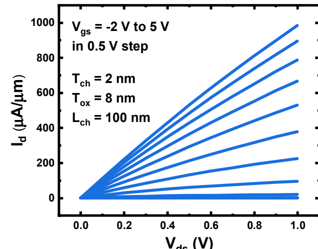

Fig. 5. Output characteristics of an IGZO FET with the L_{ch} of 100 nm, showing I_{on}=1mA/μm at V_{ds}=1V.

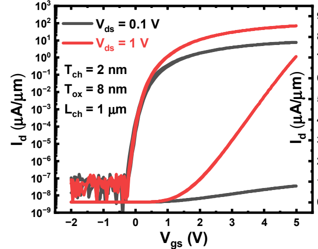

Fig. 6. Transfer characteristics of an IGZO FET with the L_{ch} of 1 μm at V_{ds}=0.1V and 1V.

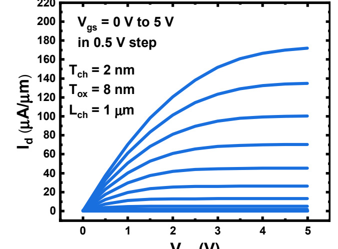

Fig. 7. Output characteristics of an IGZO FET with the L_{ch} of 1 μm, showing good current saturation.

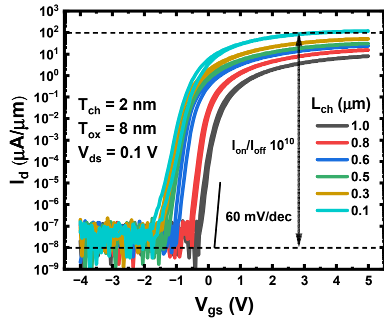

Fig. 8. Channel length-dependent transfer characteristics of IGZO FETs with 10^{10} I_{on}/I_{off} ratio.

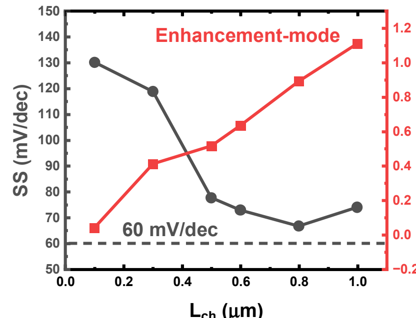

Fig. 9. Channel length-dependent subthreshold swing SS and threshold voltage V_t on the devices in Fig. 8.

- ❖ 90 nm SiO_2/Si substrate or 8 nm HfO_2 on top of IGZO n-type devices
- ❖ **P-type channel: ALD 15 nm TeO_x/Te 80 °C**
- ❖ **Via formation (optional)**
- ❖ **S/D contact (p-type): 40 nm Ni**
- ❖ **Channel isolation: dry etching**

Fig. 10. Fabrication process flow of bottom-gate TeO_x/Te p-type transistor on pre-defined structures or substrates.

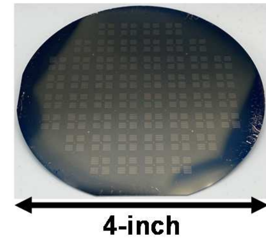

Fig. 13. Photograph of ALD-TeO_x/Te FET arrays fabricated on a four-inch Si/SiO_2 wafer.

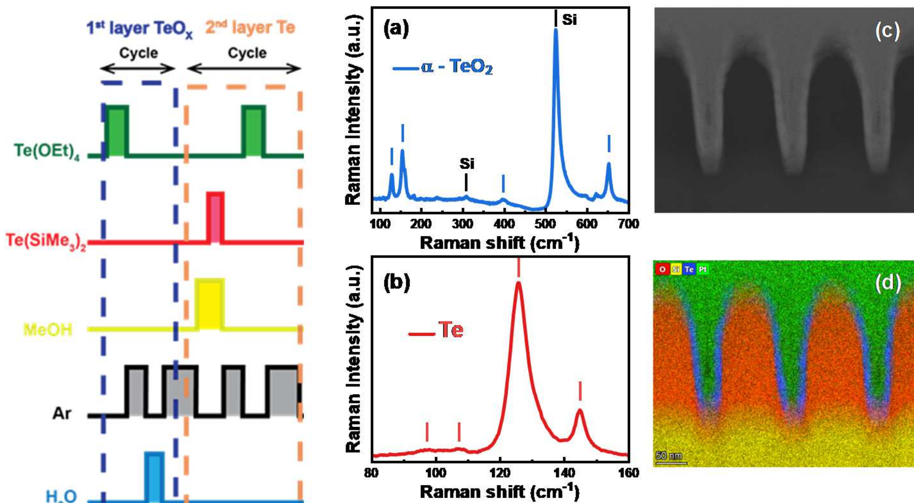

Fig. 11. ALD growth sequences of TeO_x and Te. The growth temperature is optimized at 80 ºC.

Fig. 12. The Raman spectrum of ALD TeO_x (a) and Te (b), showing the material composition. Cross-sectional HAADF-STEM image (c) and EDS elemental mapping (d) of ALD-TeO_x/Te films grown on Si fin structure with width of 45 nm and height of 180 nm, showing a conformal ALD grow process.

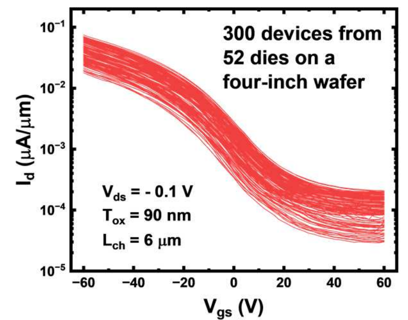

Fig. 14. Statistical electrical performance of 300 14-nm-thick ALD-TeO_x/Te FETs with L_{ch} = 6 μm. The gate dielectric is 90 nm SiO_2.

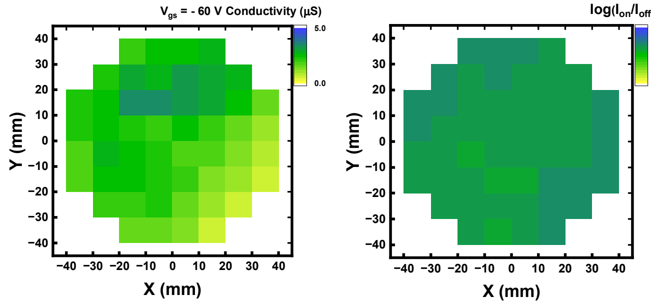

Fig. 15. Spatial mapping of conductivity at V_{gs}=-60V of 300 devices with the L_{ch} of 6 μm on a four-inch wafer.

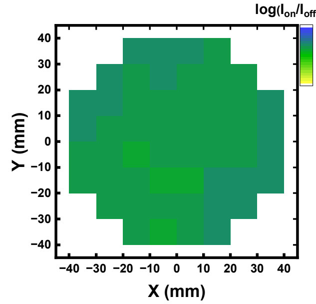

Fig. 16. Spatial mapping of I_{on}/I_{off} ratio of 300 devices with the L_{ch} of 6 μm on a four-inch wafer, showing uniform ALD growth.

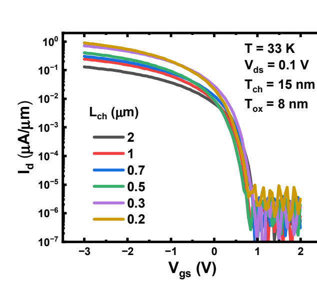

Fig. 17. Transfer characteristics of different channel length ALD-TeO_x/Te FETs measured at 33 K. The gate dielectric is 8 nm HfO_2.

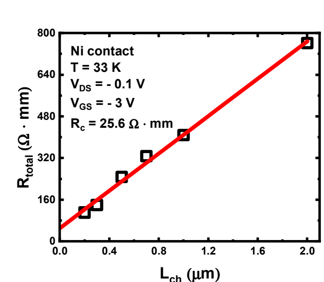

Fig. 18. Total resistance as a function of channel length at 33 K showing the scaling of Te p-type transistors.

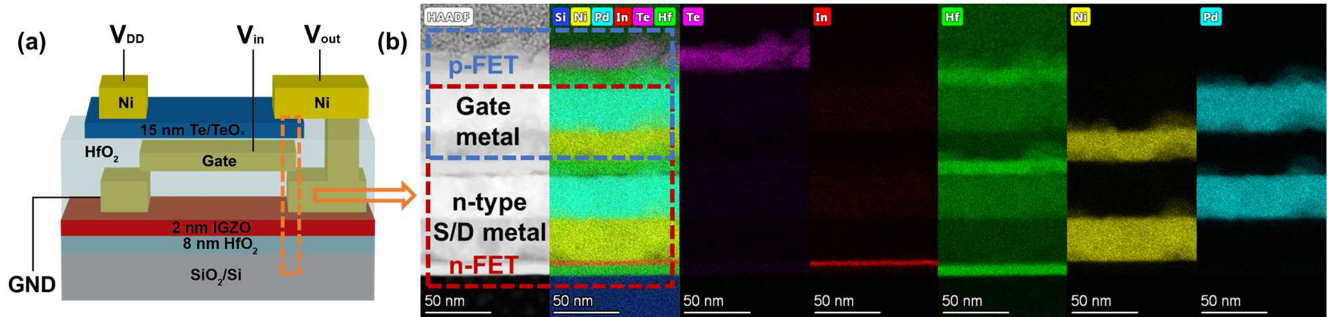

Fig. 19. (a) Structure schematic of an ALD-IGZO/Te CFET inverter. (b) Cross-sectional HAADF-STEM image and EDS elemental mapping of the ALD-IGZO/Te CFET structure at the S/D metal area showing the material stack. 2-nm-thick IGZO and 15-nm-thick TeO_x/Te are used as n-type and p-type channel material, respectively. The space between p and n channel separated by the gate metal layer and two dielectric layers is about 60 nm.

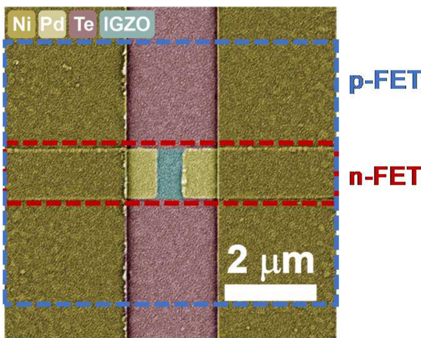

Fig. 20. Top view SEM image of ALD-IGZO/Te CFET, showing p-FET stacked on n-FET with shared metal gate.

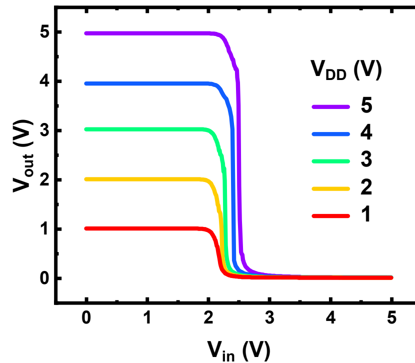

Fig. 21. Voltage transfer characteristics of a typical CFET inverter with different V_{DD}. n-type: L_{ch}=0.5μm, W_{ch}=1μm, p-type: L_{ch}=5μm, W_{ch}=10μm.

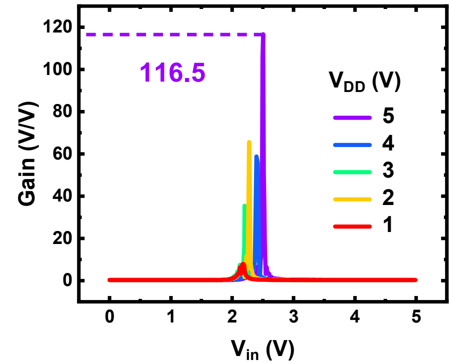

Fig. 22. The voltage gains at various V_{DD} extracted from Fig. 21. A high voltage gain of 116.5 V/V is demonstrated at V_{DD}=5V.

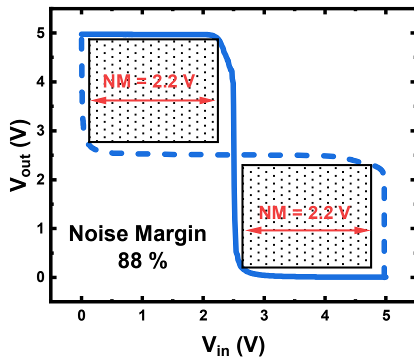

Fig. 23. Noise margin of the same CFET invertor as in Fig. 21. A large noise margin of 2.2V (88%) is achieved.

Table 1. Comparisons of state-of-the-art monolithic 3D CMOS inverters using oxide semiconductors and 2D materials as channels.

	This work	[7]	[8]	[9]	[10]	[11]	[12]
n-FET	IGZO	IGZO	In_2O_3	ZnO	IGZO	IGZO	MoS_2
p-FET	TeO_x/Te	Te	SeTe-TeO_x	Te	Poly-Si	SnO	WSe_2
Structure	CFET	Planar	Planar	Planar	CFET	Planar	CFET
Gain (V/V) (V_{DD})	116 (5 V)	75.2 (3 V)	1300 (20 V)	46 (3 V)	18 (1.4 V)	112 (10 V)	18 (3 V)
Process temperature (°C)	< 225	< 400	< 250	< 200	< 700	< 225	< 200
N-channel process	ALD	Sputter	Inkjet-printing	ALD	Sputter	Sputter	CVD
P-channel process	ALD	Sputter	Thermal evaporation	ALD	PECVD	Sputter	CVD