First Experimental Demonstration of 100 nm Inversion-mode InGaAs FinFET through Damage-free Sidewall Etching


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Abstract

The first well-behaved inversion-mode InGaAs FinFET with gate length down to 100 nm with ALD Al$_2$O$_3$ as gate dielectric has been demonstrated. Using a damage-free sidewall etching method, FinFETs with $L_{ch}$ down to 100 nm and $W_{fin}$ down to 40 nm are fabricated and characterized. In contrast to the severe short-channel effect (SCE) of the planar InGaAs MOSFETs at similar gate lengths, FinFETs have much better electro-static control and show improved $S.S.$, $DIBL$ and $V_T$ roll-off and less degradation at elevated temperatures. The SCE of III-V MOSFETs is greatly improved by the 3D structure design. The more accurate $D_{th}$ estimation from the $S.S.$ is also presented.

Introduction

With the continuous request of carrier transport boosting in CMOS devices, very recently, much progress has been made on achieving on-state performance of inversion-mode In-rich InGaAs MOSFETs using high-k gate dielectrics [1-4]. However, the off-state performance of InGaAs MOSFETs is far from satisfactory according to ITRS requirement. The short-channel effect (SCE) of InGaAs MOSFETs deteriorates more quickly than Si MOSFETs due to its nature of narrower bandgap and higher semiconductor dielectric constant [5]. In order to achieve better gate control capability, new structure design like FinFET demonstrated successfully in Si devices [6-10], is strongly needed for short-channel III-V MOSFETs. However, unlike Si, the dry etching of III-V semiconductor surface has been believed to be difficult and uncontrollable [7], especially related with surface damage and integration with high-k dielectrics. In this paper, we report for the first experimental demonstration of inversion-mode In$_{0.53}$Ga$_{0.47}$As tri-gate FinFET using damage-free etching and ALD Al$_2$O$_3$ as gate dielectric. The SCE is greatly suppressed in terms of subthreshold slope (SS), drain induced barrier lowering (DIBL) and threshold voltage ($V_T$) roll-off. Detailed analysis and comparison are performed on the FinFETs with channel length ($L_{ch}$) from 200 nm to 100 nm, fin width ($W_{fin}$) from 100 nm to 40 nm, and fixed fin height ($H_{fin}$) of 40 nm.

Experiments

Fig. 1 and Table 1 show the schematic cross section of the uniform device structure and the device fabrication flow. A 500 nm p-doped $2\times10^{18}$ cm$^{-3}$ InP layer, a 300 nm p-doped $2\times10^{16}$ cm$^{-3}$ and a 40 nm $2\times10^{16}$ cm$^{-3}$ In$_{0.53}$Ga$_{0.47}$As channel layer were sequentially grown by MBE on a 2-inch InP p$^+$ substrate. The heavily doped InP layer beneath the channel was chosen to prevent punch through and reduce substrate leakage because of its higher bandgap. Due to the non-optimized source/drain junctions, the heavily doped InP layer resulted in worsened junction leakage. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al$_2$O$_3$ layer was deposited at a substrate temperature of 300°C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of $1\times10^{14}$ cm$^{-2}$ at 20 keV through a 10 nm thick Al$_2$O$_3$ layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by rapid thermal anneal (RTA) at 600°C for 15 s in a nitrogen ambient. The reduction of activation temperature from 750°C to 600°C resulted in much improved S/D junction leakage while achieving similar activation efficiency. [5] A combined dry and wet etching was used to pattern the fin structures. HDPE BCl$_3$/Ar was used for dry etching while ZEP-520A electron-beam resist was used as a mask. A short dip of 3 seconds in diluted H$_2$SO$_4$:H$_2$O$_2$:H$_2$O solution was carried out immediately after the dry etching to remove the damaged surface layer. The resulted fin channels have a depth of 40 nm which can be seen from the last SEM image in Fig. 3. More sophisticated process is needed to make the fin side-walls perfectly vertical. A 5 nm Al$_2$O$_3$ film was regrown by ALD after removing the encapsulation layer by BOE solution and (NH$_4$)$_2$S surface preparation. After 400-500°C PDA process, the source and drain ohmic contacts were made by an electron-beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320°C for 30 s also in a N$_2$ ambient. The gate electrode was deposited by electron-beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 100 nm to 150 nm and fin widths from 40 nm to 100 nm. The final 3D device structure is shown in Fig. 2. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. A Keithley 4200 was used for MOSFET output characteristics. The combined dry and wet etching for the formation of fin channels results in damage-free sidewalls. It is verified by the carrier transport through the fin channels without any significant degradation, compared to the planar devices.

Results and Discussions

Fig. 4 shows the gate leakage current density ($J_g$) of 100 nm-long FinFET with $W_{fin}$ of 40 nm and 100 nm, compared to the planar device at $V_{ds}=0.8$V on-state. The $J_g$ of FinFETs...
increases more than one order of magnitude but still remains in the range of $10^{-4}$ A/cm$^2$, which is about 8-9 orders of magnitude smaller than the drain current. The 3D structure would generally result in higher gate leakage current mostly from the corner regions, where electric field line is mostly crowded. Although ALD dielectric should be quite conformal, corner regions could also be the weakest point of dielectric strength. The small degradation suggests that the 5 nm Al$_2$O$_3$ is good enough for this 3D structure and leaves room for further EOT reduction. Fig. 5 shows the typical output characteristics of a planar 100 nm-long MOSFET. It cannot be turned off at zero gate bias due to the SCE [5]. Fig. 6 depicts the well-behaved output characteristic of a FinFET with 40 nm $W_{\text{Fin}}$ at the same channel length. From the comparison, it clearly shows the FinFET has much better behaved output characteristics in terms of off-state while maintaining the on-state performance. Fig. 7 shows the total channel resistance for FinFETs with three different channel lengths. The $R_{\text{ch}}$ can be extracted to be ~1200 $\Omega$ $\mu$m as shown in the inset of Fig. 7.

Fig. 8 compares the transfer characteristics of a 100nm-long channel planar FET and FinFETs with $W_{\text{Fin}}$ of 40 nm and 100 nm. The FinFETs have better off-state performance over the planar one. The 40 nm $W_{\text{Fin}}$ device has the best electro-static gate control of the channel. The on-off ratio of FinFETs improves almost by two orders of magnitude over the planar one. The positive $V_T$ shift also suggests that the pinch-off characteristic for FinFET is better than the planar device. SS from the saturation region as well as DIBL are compared among FinFETs with 4 different $W_{\text{Fin}}$ from 40 nm to 100 nm and the planar FET in Fig. 9 and Fig. 10. The trend shows the device with narrower $W_{\text{Fin}}$ has better SS and DIBL as expected. The SS of FinFET with 100 nm channel length improves more than 34% percent and degrades much slower when channel length gets shorter. The DIBL is greatly reduced from 440 mV/V for the planar device to 180 mV/V for the FinFET at 100 nm gate length. Fig. 11 and Fig. 12 show the relation of SS and DIBL with the ratio of $W_{\text{Fin}}/L_{\text{ch}}$. Both SS and DIBL is roughly proportional to $W_{\text{Fin}}/L_{\text{ch}}$. It shows that further channel length scaling can be achieved by narrowing the fin width to avoid SCE. $V_T$ roll-off, another important metric for SCE is shown and compared in Fig. 13 among planar device, 40 nm $W_{\text{Fin}}$ and 100 nm $W_{\text{Fin}}$ devices, all with 100 nm channel length. $V_T$ is determined by 1 $\mu$A/ $\mu$m metrics at $V_{ds}=0.8$V. The 40 nm $W_{\text{Fin}}$ FinFET shows smallest $V_T$ roll-off, which is only 30% of the planar FET and the degradation of $V_T$ roll-off when channel length gets shorter is smaller compared with the planar FET.

At elevated ambient temperatures, Fig. 14 and Fig. 15 compare SS of the three FETs at $V_{ds}=0.05$V and $V_{ds}=0.8$V, respectively. The FinFETs have much better SS at varying temperatures. The fact that the channel surfaces of FinFET should be not better than the planar devices, if not worse after going through all the patterning and etching processes. It is clear that the SS is not only affected by interface trap density, but also by SCE. Simple estimation of interface trap density ($D_{it}$) from SS would result in gross overestimation of $D_{it}$. At the linear region, SS of FinFETs in Fig. 15 are lower than those from the planar FET, indicating that the interface properties of Al$_2$O$_3$/InGaAs on the etched sidewalls are not degraded much by the fin etching process, or $D_{it}$ on the sidewalls is not much larger than that on the planar structures. It verifies that the newly developed dry/wet etching process is damage-free and suitable for 3D III-V device fabrication. Fig. 16 and Fig. 17 show DIBL and $V_T$ roll-off of the three FETs at different temperatures. Unlike SS with strong dependence of $D_{it}$, DIBL and $V_T$ roll-off clearly show that FinFETs offer much better tolerance at raised temperatures. DIBL and $V_T$ of FinFETs with $W_{\text{Fin}}$=40 nm changed 60 mV/V and 0.2 V, compared to 175 mV/V and 0.48 V of the planar FET. Although $D_{it}$ can be simply estimated from SS at linear region in long-channel devices, it’s also possible to estimate the $D_{it}$ value by counting the SCE in short-channel devices. SS is found to be proportional with the ratio $W_{\text{Fin}}/L_{\text{ch}}$ from the experimental data as shown in Fig. 18. When $W_{\text{Fin}}/L_{\text{ch}}=0$, SCE is eliminated since the best electro-static control of the channel is achieved with the thinnest fin. By taking extrapolated SS at $W_{\text{Fin}}/L_{\text{ch}}=0$, more intrinsic SS can be obtained and used to estimate $D_{it}$ for deep-submicron InGaAs FinFETs. The upper limit of average $D_{it}$ on the top and sidewall surfaces in In$_{0.53}$Ga$_{0.47}$As FinFET is 1.7x10$^{12}$/cm$^2$-eV from the data in Fig. 18. The similar trend is also observed from the simple calculation of SS vs. $W_{\text{Fin}}/L_{\text{ch}}$ as a function of $D_{it}$. The result confirms that the newly developed dry/wet etching process produces damage-free InGaAs sidewalls and the high-k/3D InGaAs interface is comparable to the 2D case.

Conclusion

We have demonstrated the first well-behaved inversion-mode InGaAs FinFET with ALD Al$_2$O$_3$ gate dielectric. Detailed analysis of SS, DIBL and $V_T$ roll-off are carried out on FinFETs with $L_{\text{ch}}$ down to 100 nm and $W_{\text{Fin}}$ down to 40 nm. The SCE of planar InGaAs MOSFETs is greatly improved by the 3D structure design.

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References

Table 1 Fabrication process flow for inversion-mode high-k/InGaAs FinFETs. 10 nm Al₂O₃ acts as an encapsulation layer to protect the surface during implantation and the following activation. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. Dry etching was done by Panasonic E620 high density plasma etcher (HDPE).

1) NH₄OH surface treatment and ALD Al₂O₃ 10nm deposition
2) S/D patterning and Si implantation (20KeV / 1 × 10¹⁴/cm²)
3) Si implanted S/D activation using RTA (600°C 15s in N₂)
4) Fin patterning, dry etching by HDPE BCl₃/Ar using ZEP resist as mask and 3 sec dip in very diluted H₂SO₄:H₂O₂:H₂O solution
5) (NH₄)₂S treatment 5nm ALD re-growth
6) PDA: 400-500 °C 30s in N₂
7) S/D contact patterning and Au/Ge/Ni ohmic metal and 320°C anneal
8) Gate patterning, Ni/Au evaporation and lift-off
Fig. 7 $R_{\text{total}}$ of $W_{\text{Fin}}=80\text{nm}$ FinFETs with three different channel lengths from 150nm to 100nm. Inset: $R_d$ can be extracted around 1200 $\Omega \cdot \mu\text{m}$.

Fig. 8 Transfer characteristics of FinFETs and planar FET. Better electrostatic control of FinFETs reduces the SCE.

Fig. 9 Comparison of SS of FinFETs and planar FET. SS is greatly improved for the FinFETs.

Fig. 10 Comparison of DIBL of FinFETs and planar FET.

Fig. 11 SS vs $W_{\text{Fin}}/L_{\text{ch}}$ at both linear region and saturation region.

Fig. 12 DIBL vs $W_{\text{Fin}}/L_{\text{ch}}$ for the FinFET.

Fig. 13 Saturation $V_T$ roll-off of planar FET is suppressed by FinFETs with different $W_{\text{Fin}}$.

Fig. 14 Comparison of SS of planar FET and FinFETs at raised temperatures at $V_{\text{ds}}=0.8\text{V}$.

Fig. 15 Comparison of SS of planar FET and FinFETs at raised temperatures at $V_{\text{ds}}=0.05\text{V}$.

Fig. 16 Comparison of DIBL of planar FET and FinFETs at raised temperatures.

Fig. 17 Comparison of $V_T$ roll-off of planar FET and FinFETs at raised temperatures.

Fig. 18 Calculated SS vs $W_{\text{Fin}}/L_{\text{ch}}$ w/o SCE, which reflects the real SS degradation on Dit. The vertical shift between calculated values and the experimental values is due to the SCE.