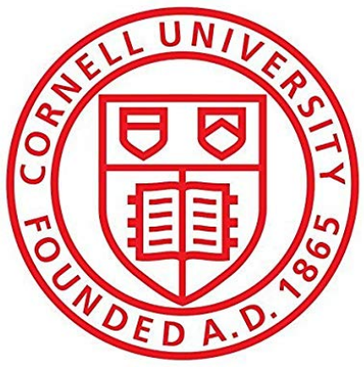
Towards High-speed Networking in the Post-Moore Era

Vishal Shrivastav

Ph.D. Thesis Defense

Cornell University 2020



Datacenters 101

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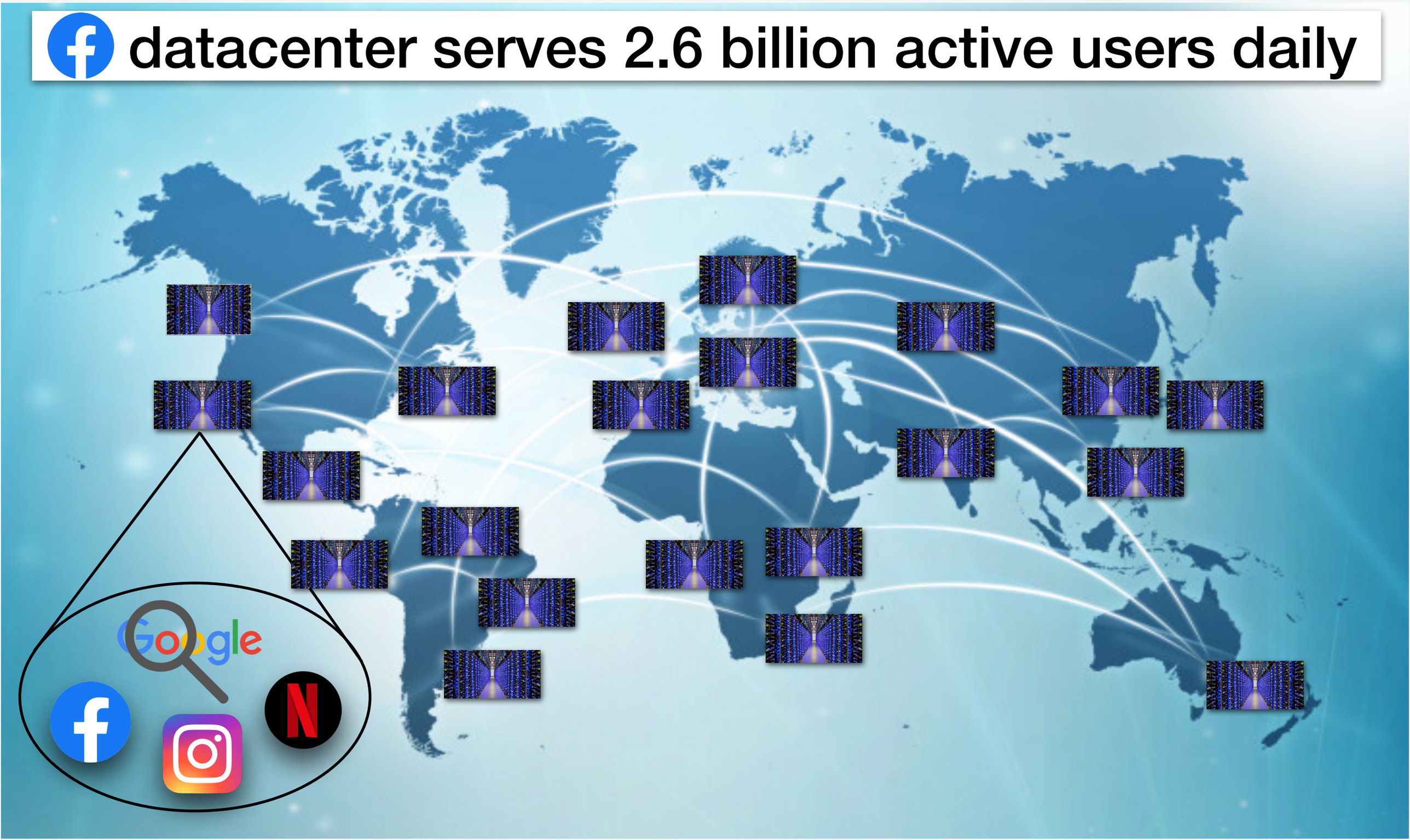
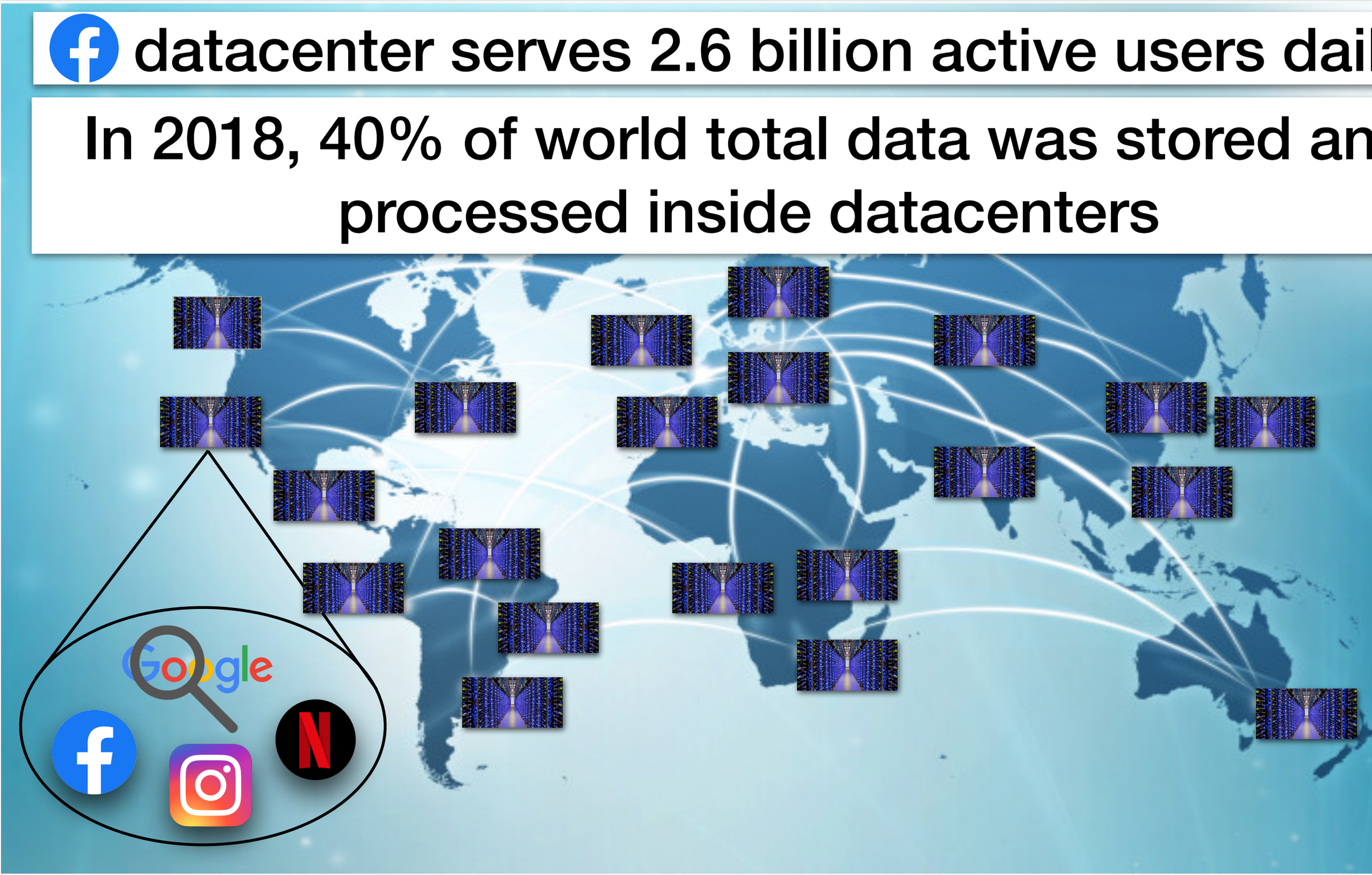


Datacenters 101

datacenter serves 2.6 billion active users daily

In 2018, 40% of world total data was stored and processed inside datacenters



Inside a Typical Datacenter

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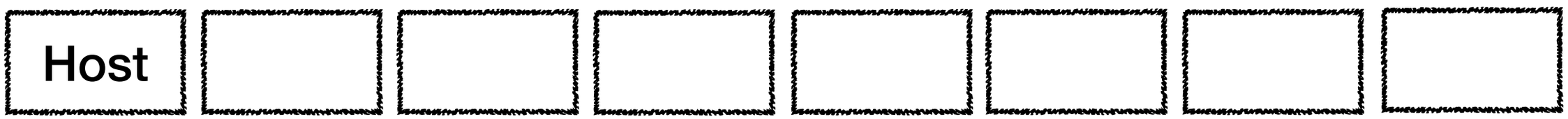

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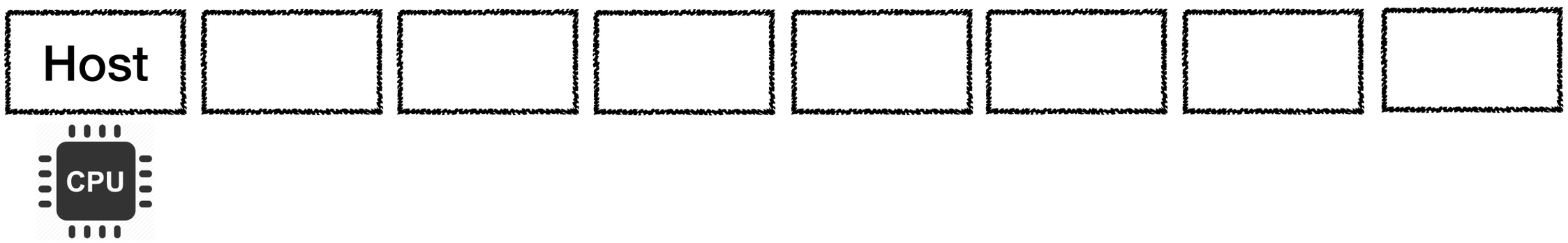

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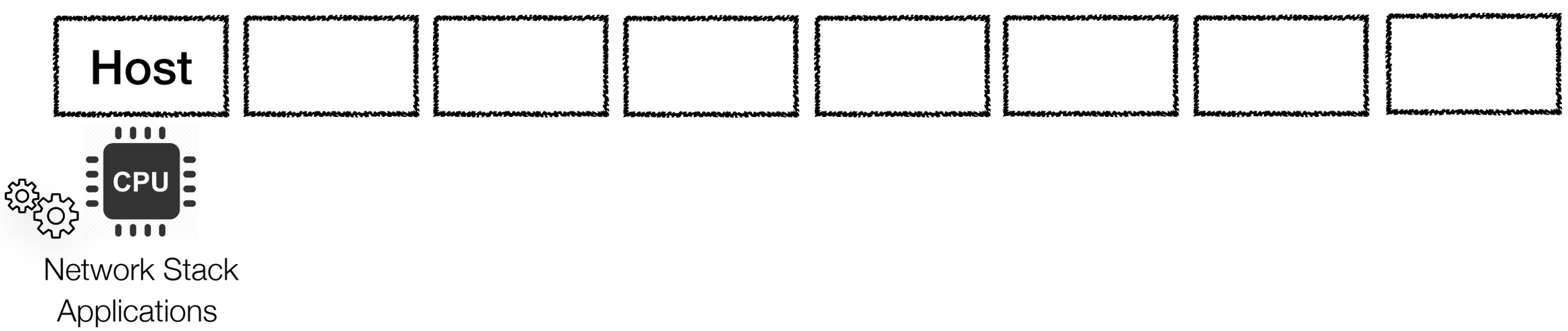

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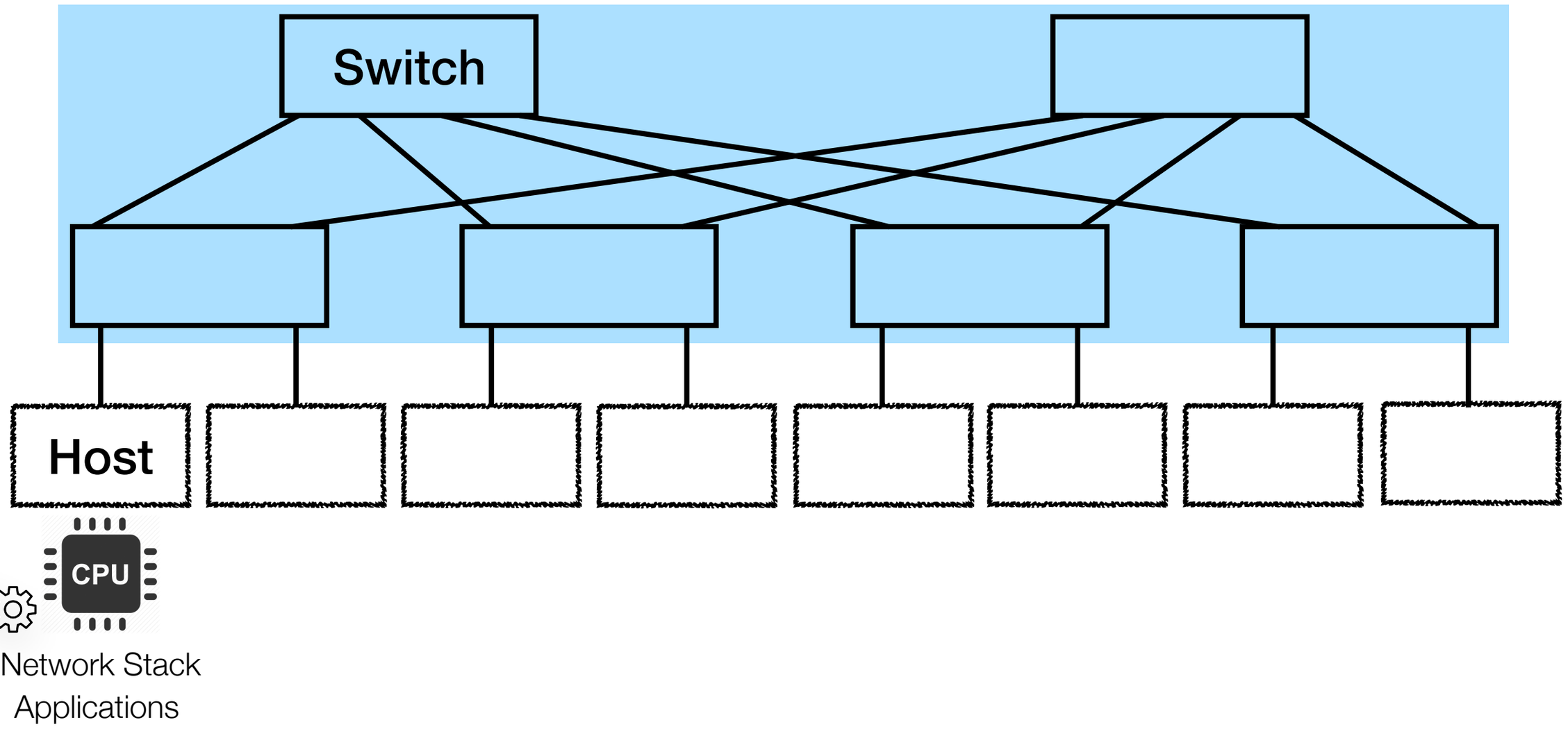

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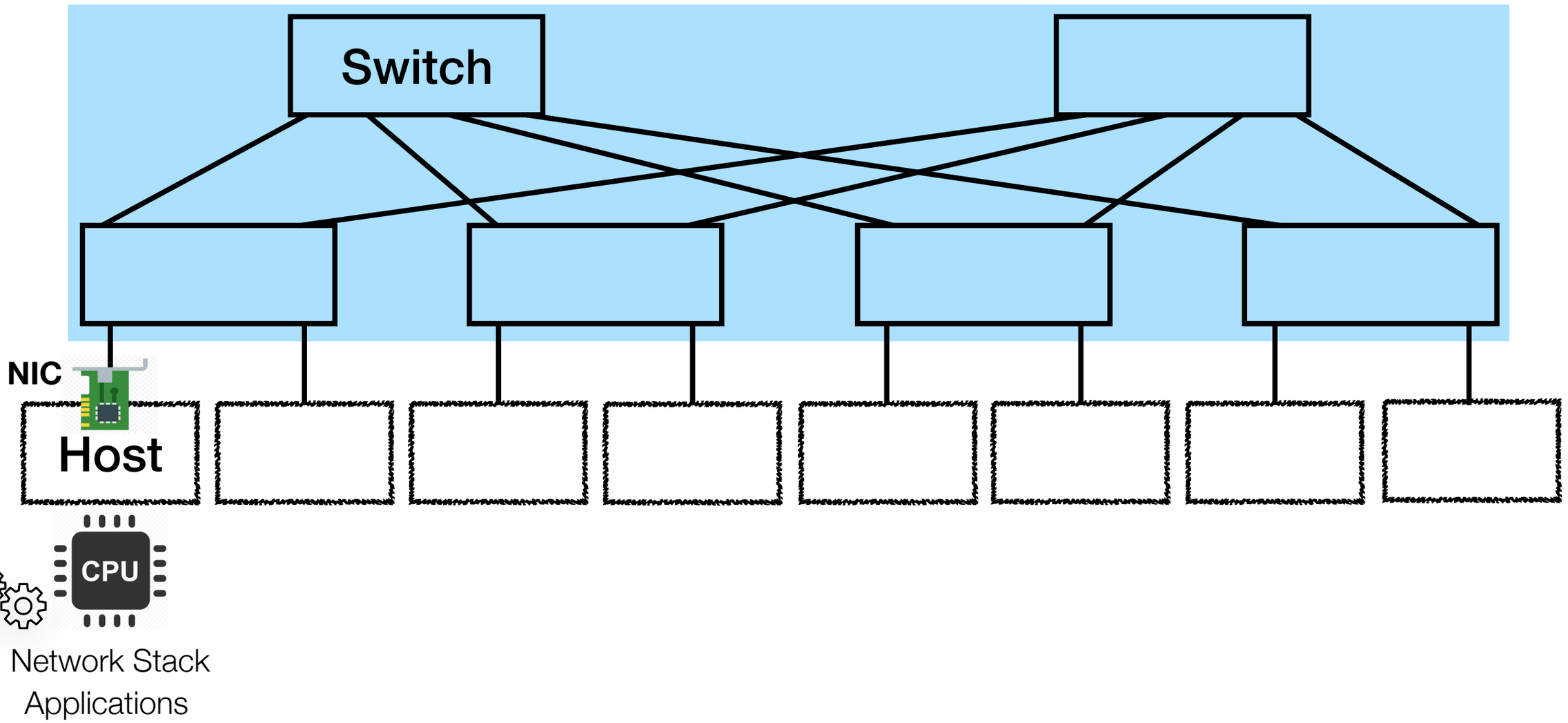

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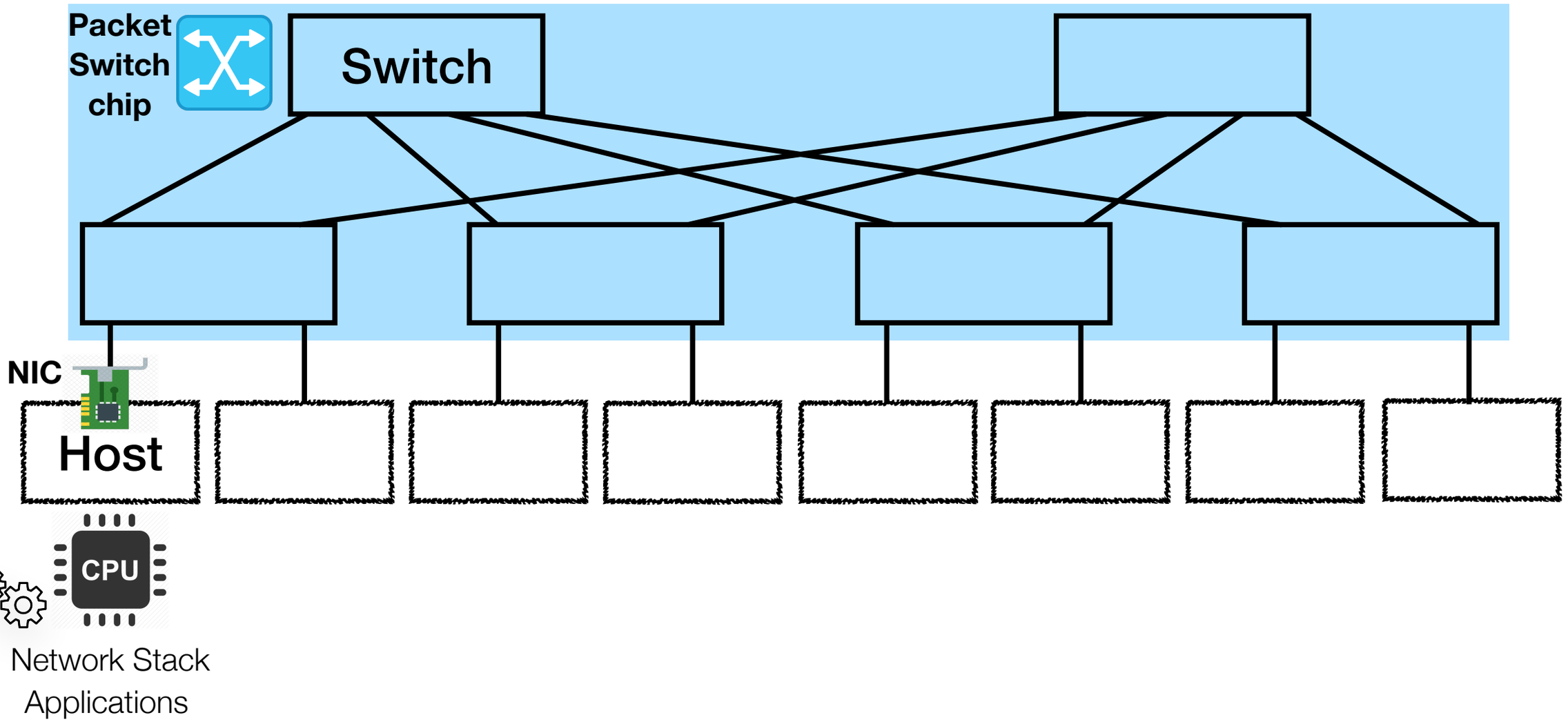

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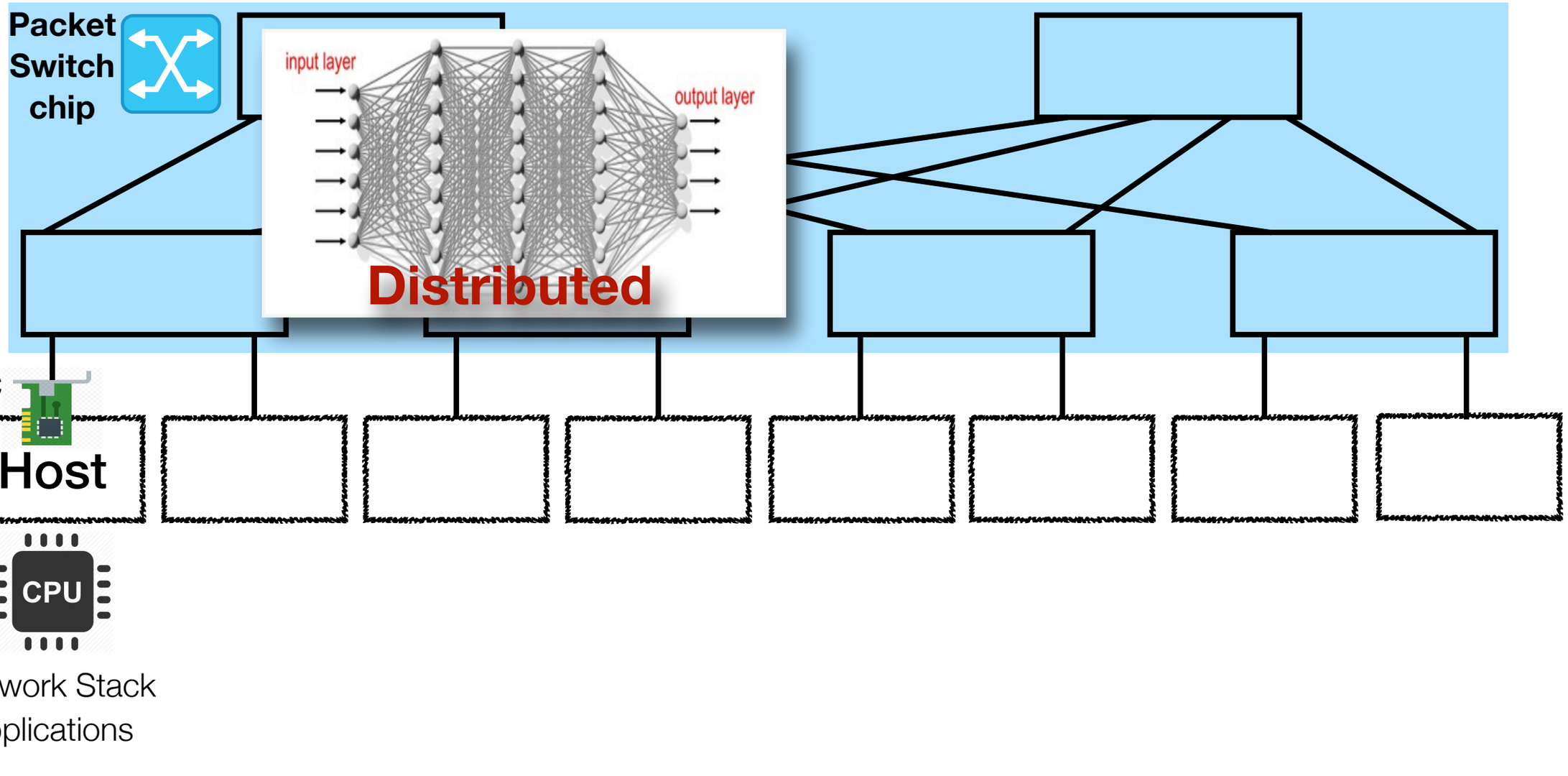

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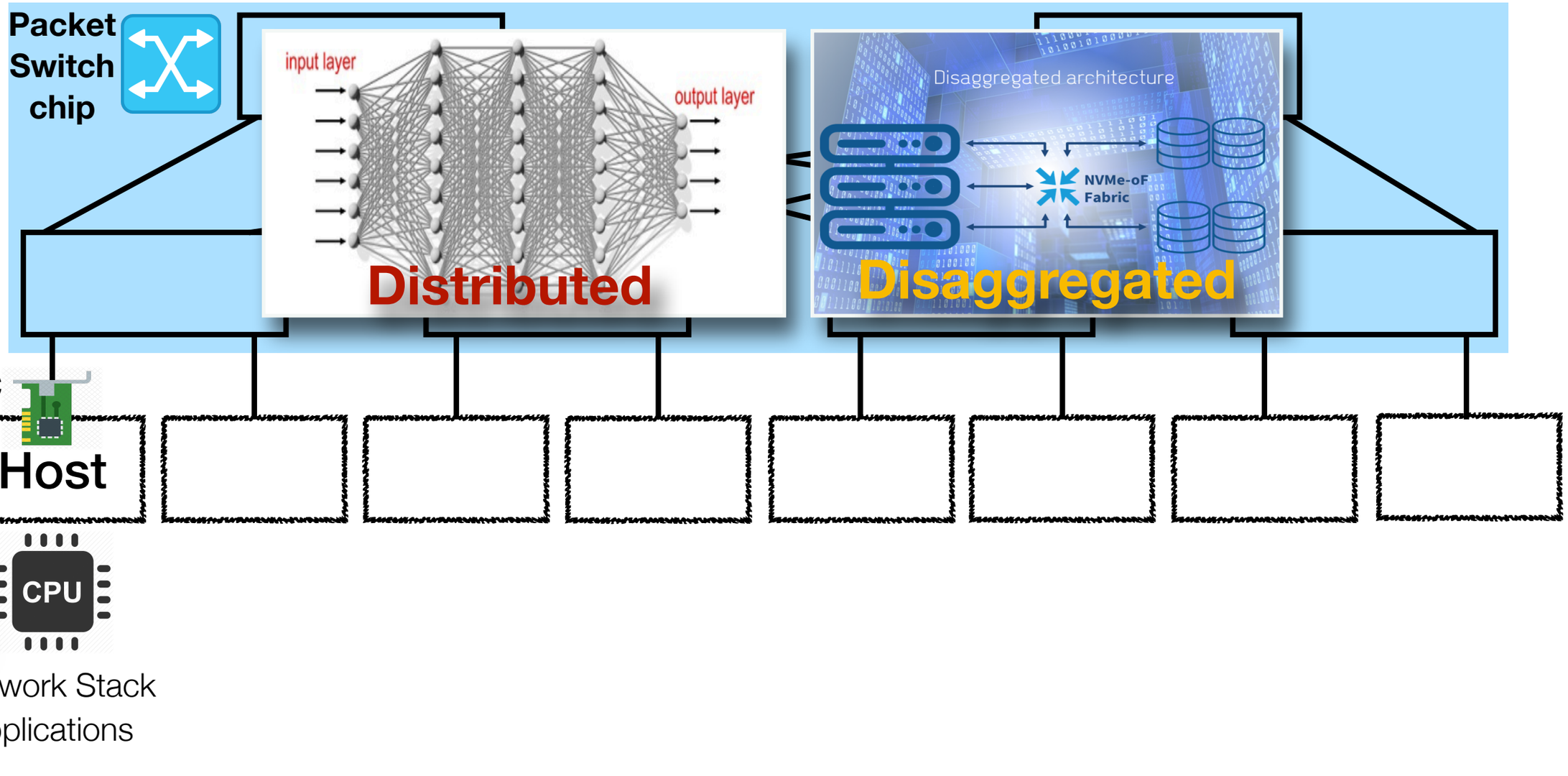

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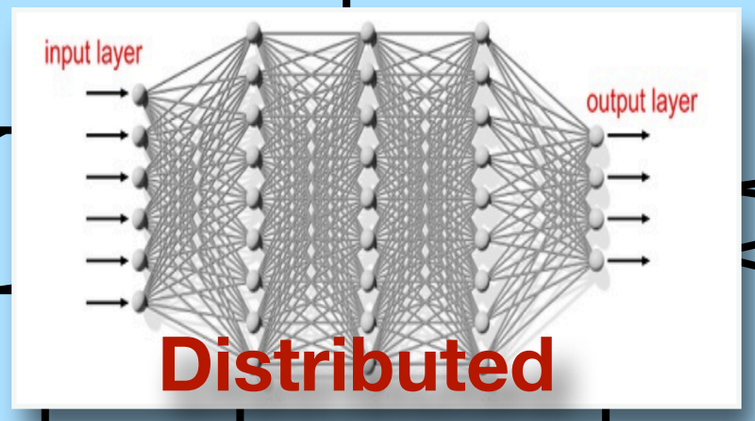
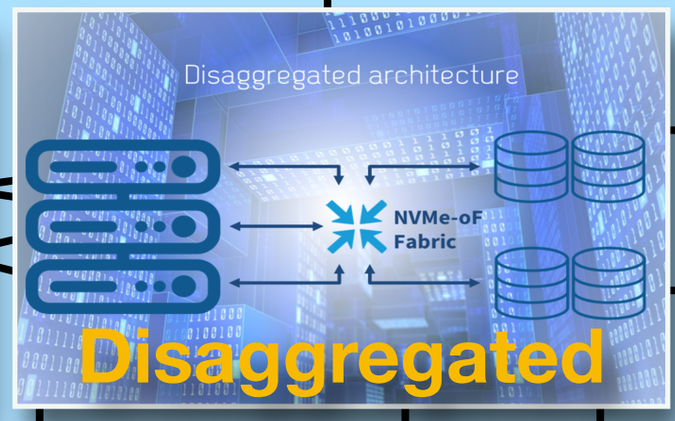
Bandwidth demand increasing **2x / year**

[Source: Google]

Packet Switch chip





NIC

Host

CPU

Network Stack

Applications

Link rate increasing **400x / 10 years**

[Source: Microsoft]

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Switch chip capacity increasing **2x / 2 years**
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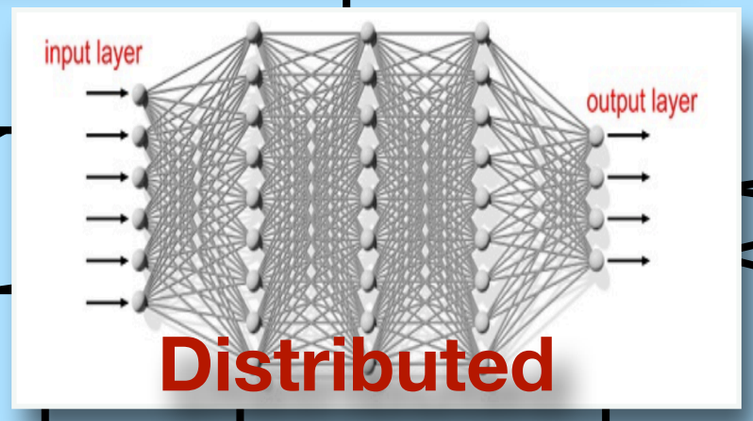

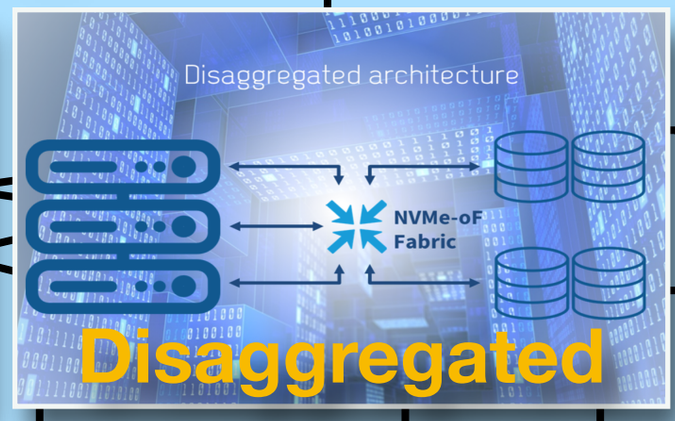

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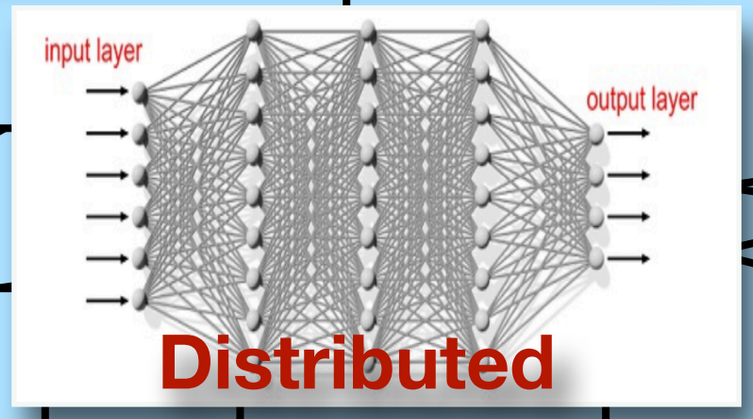

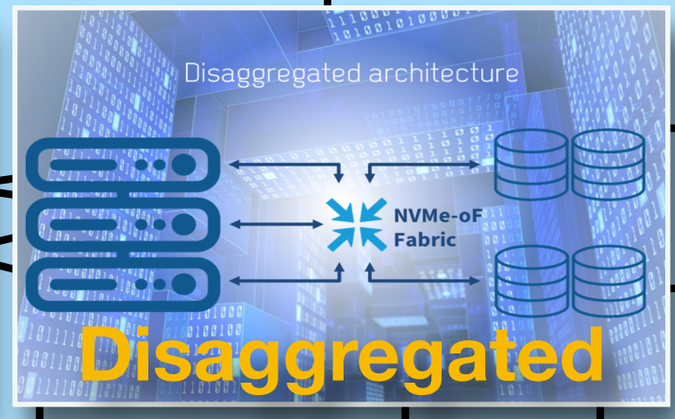

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Slowdown in Moore's Law
End of Dennard scaling

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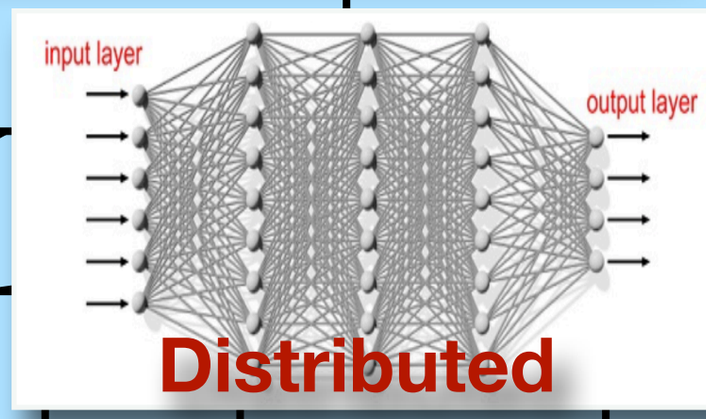

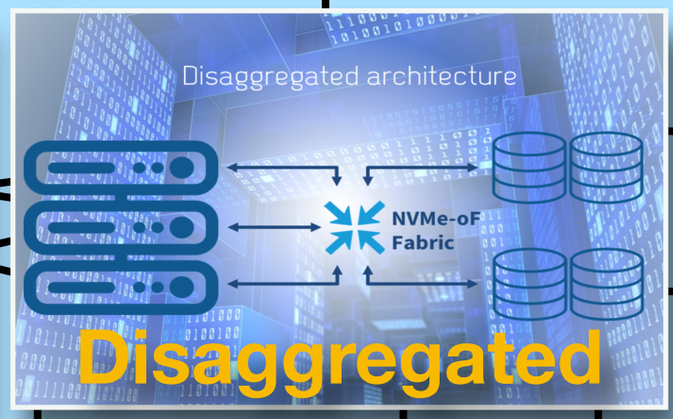

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Packet Switch chip

Switch

Distributed

Disaggregated

NIC

Host

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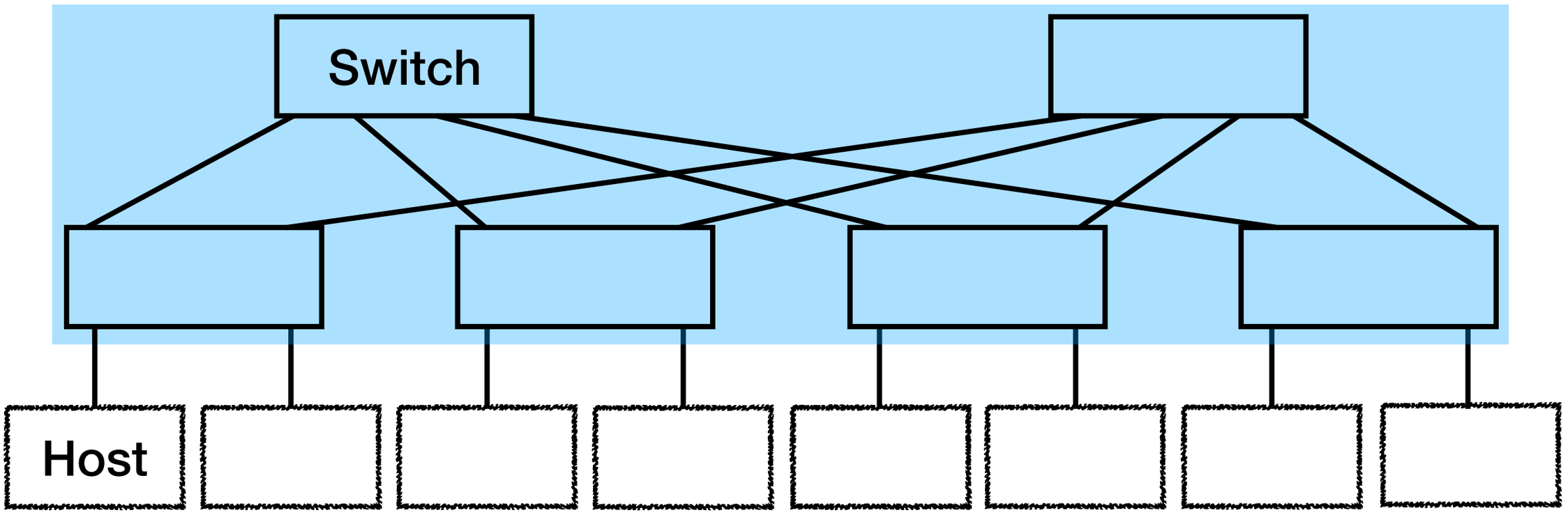
Big Research Question



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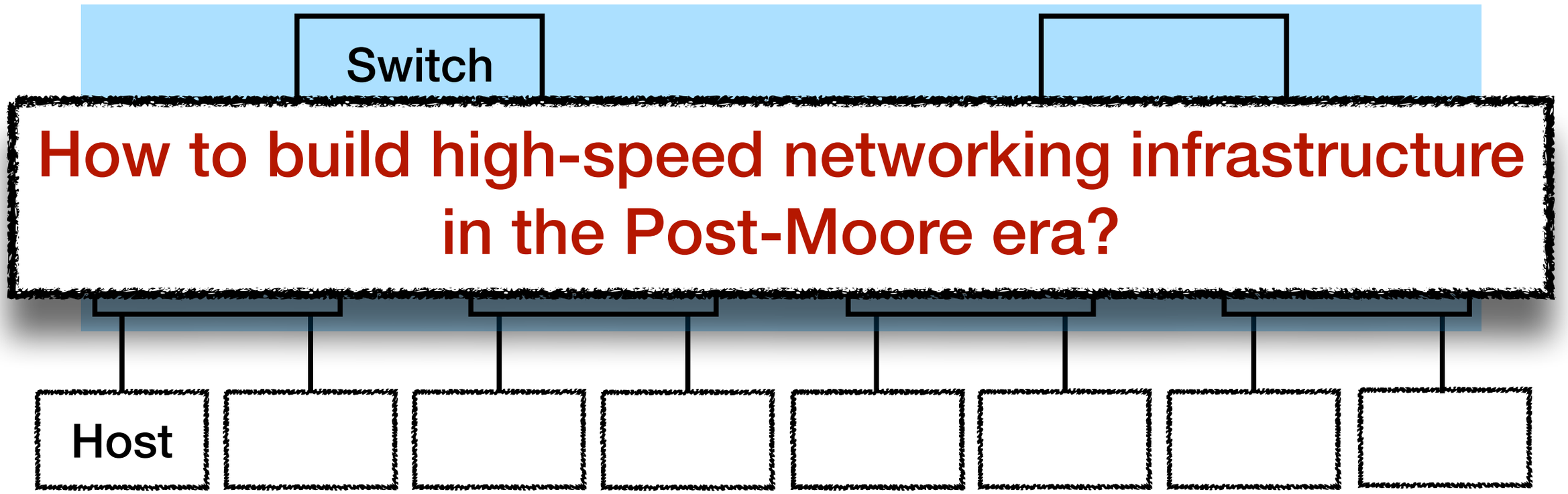

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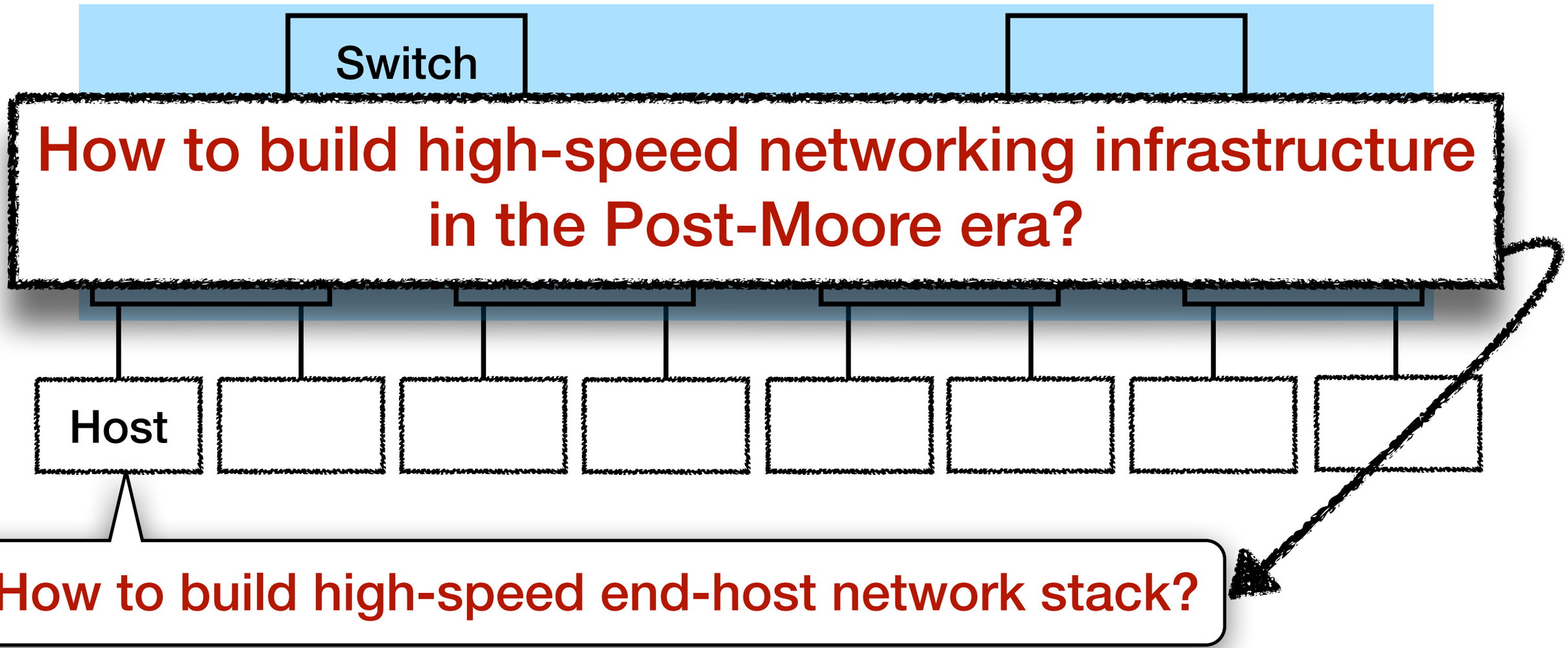

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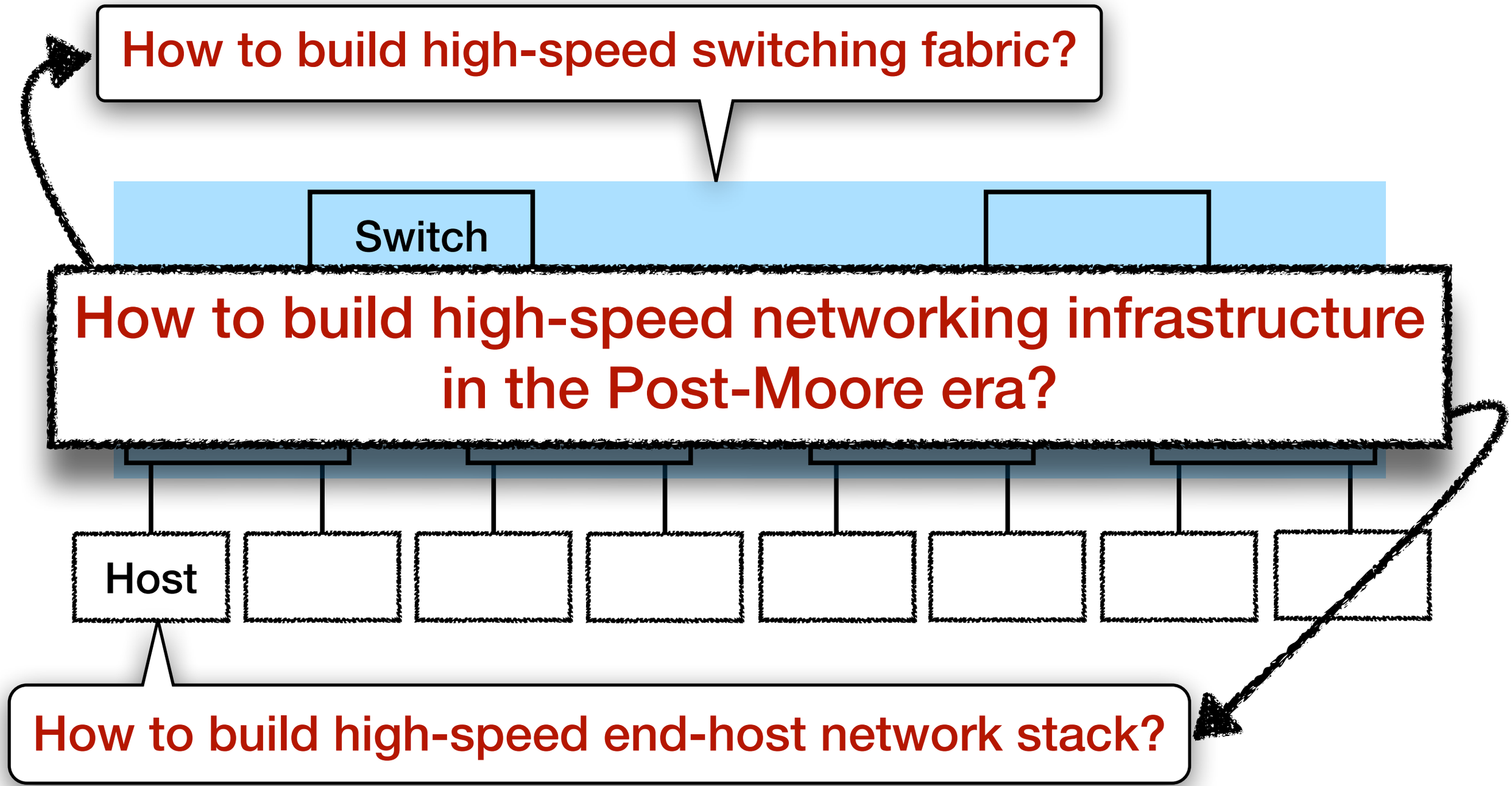
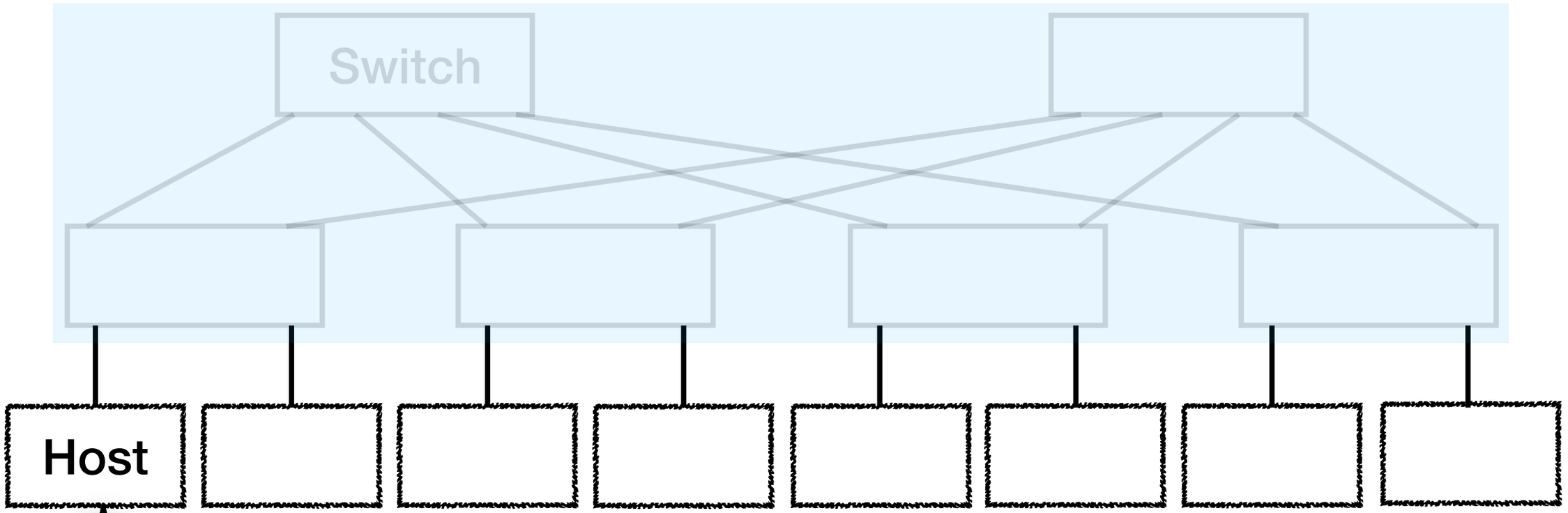


Part I : End-host Network Stack



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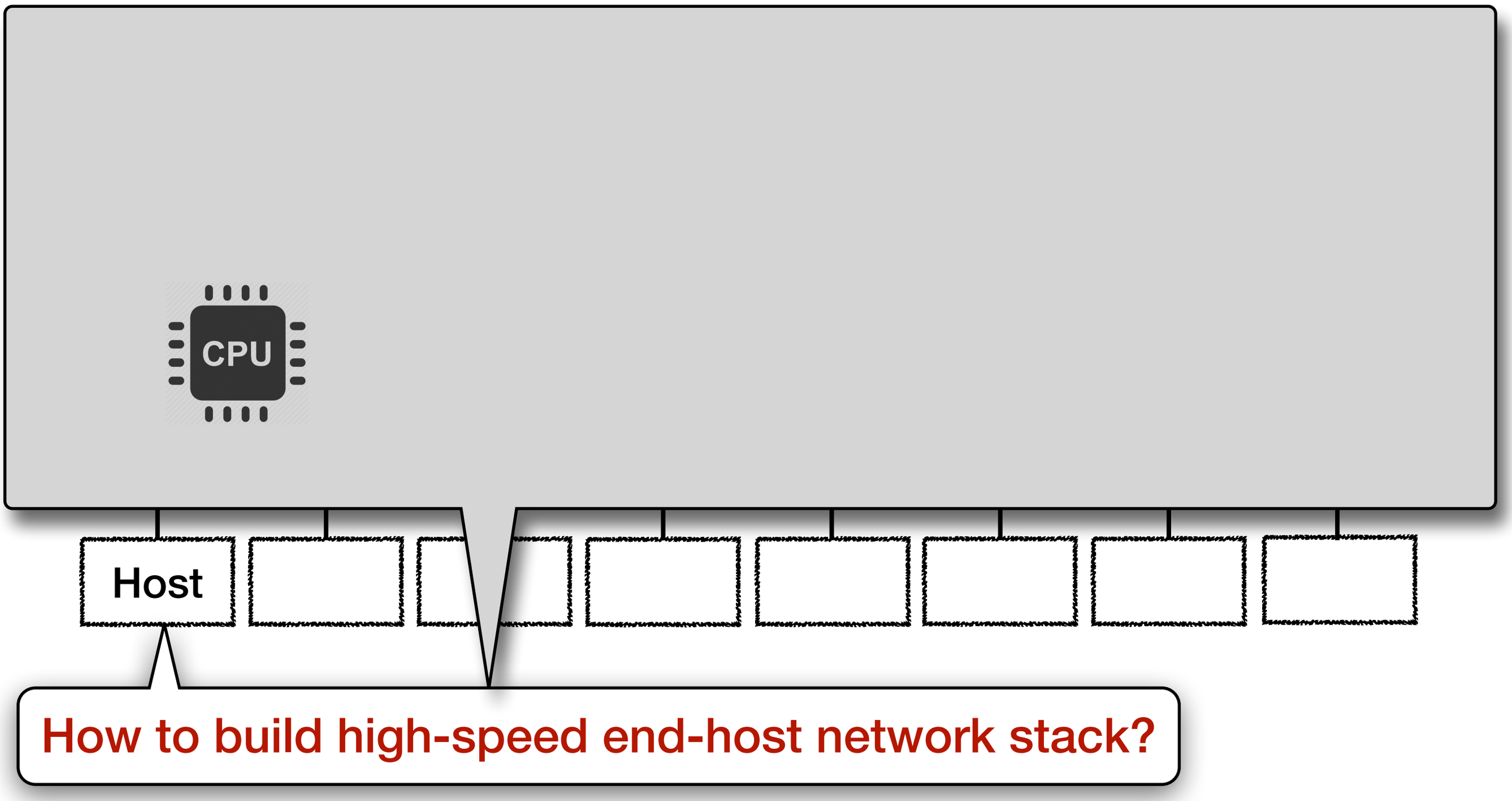

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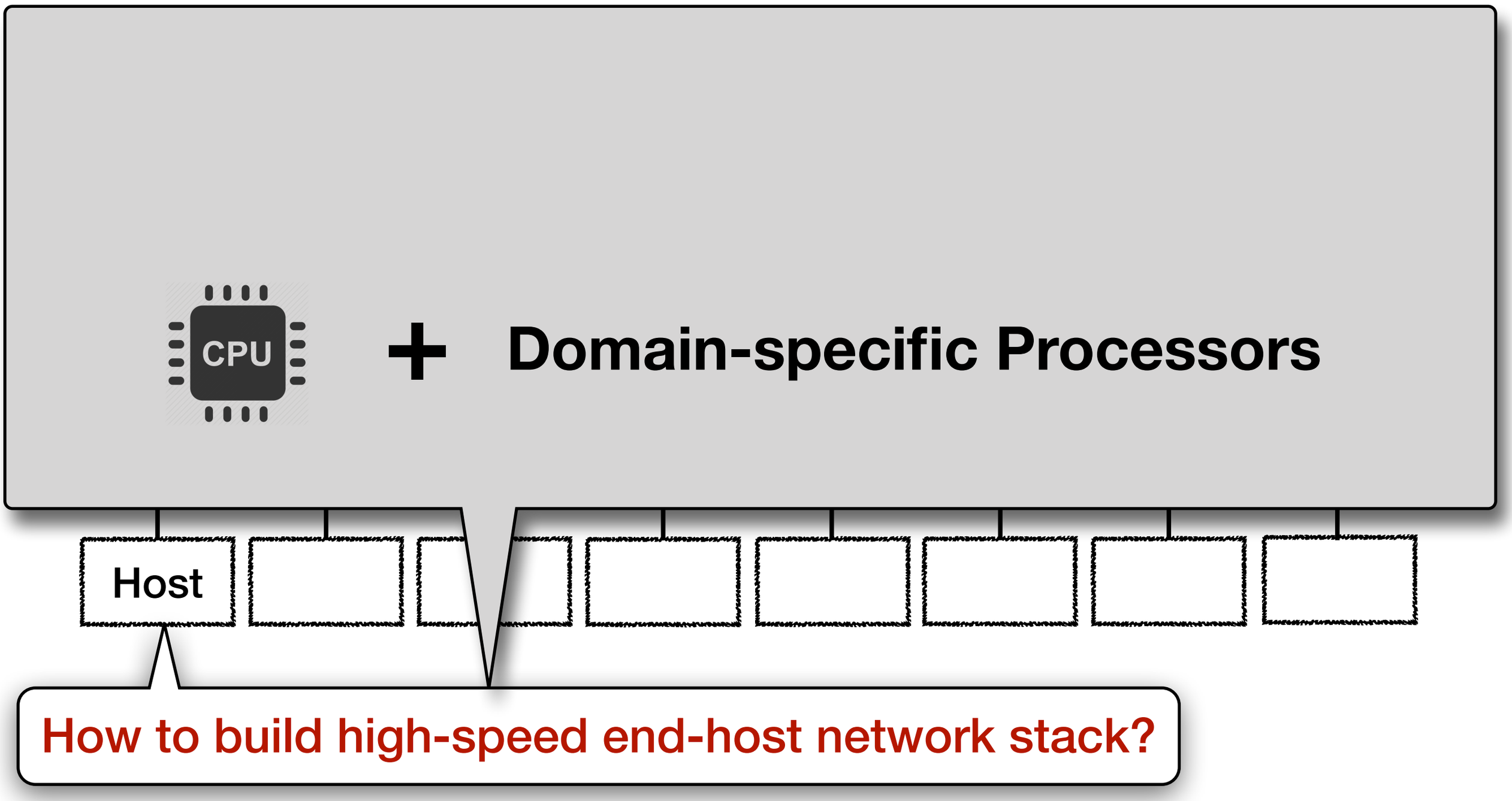

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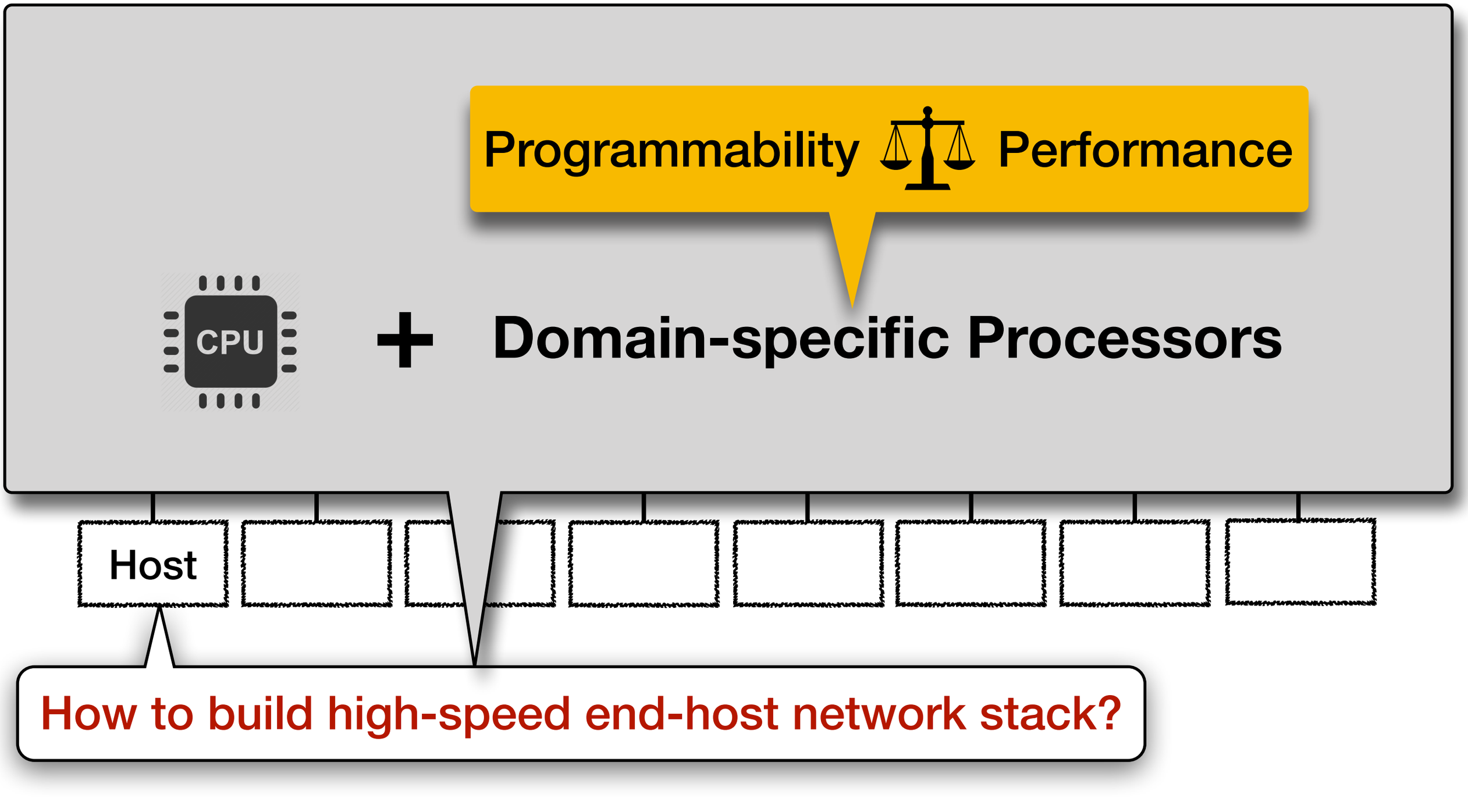
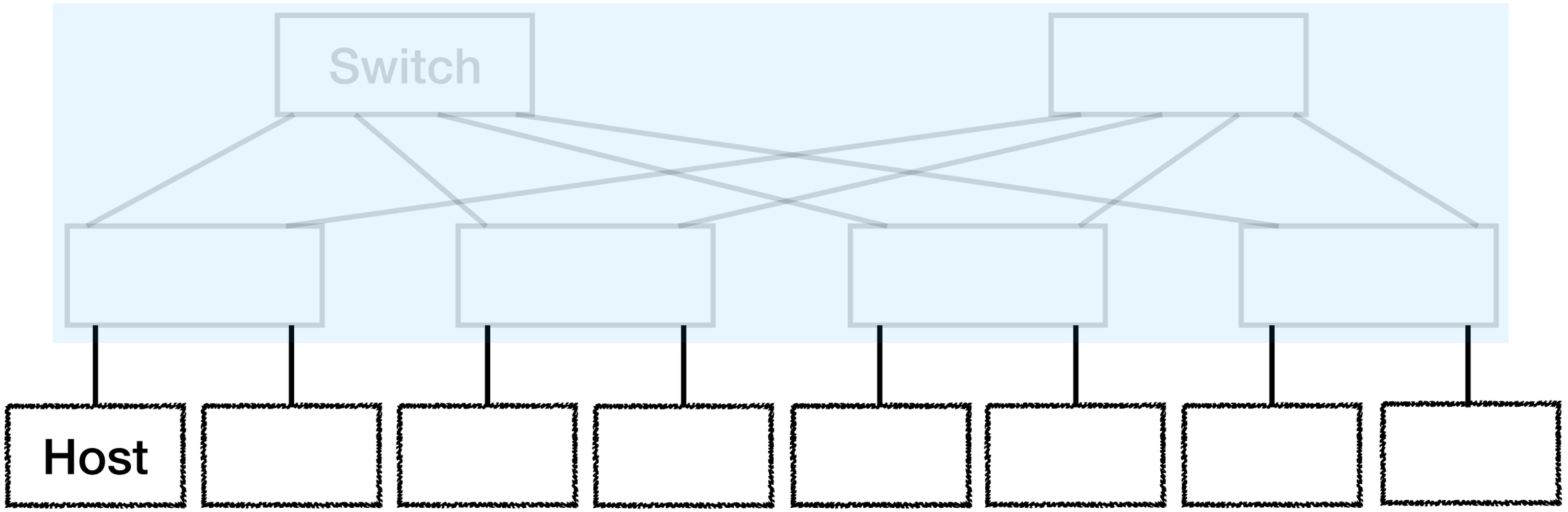


End-host Network Stack Operation : Packet Scheduling



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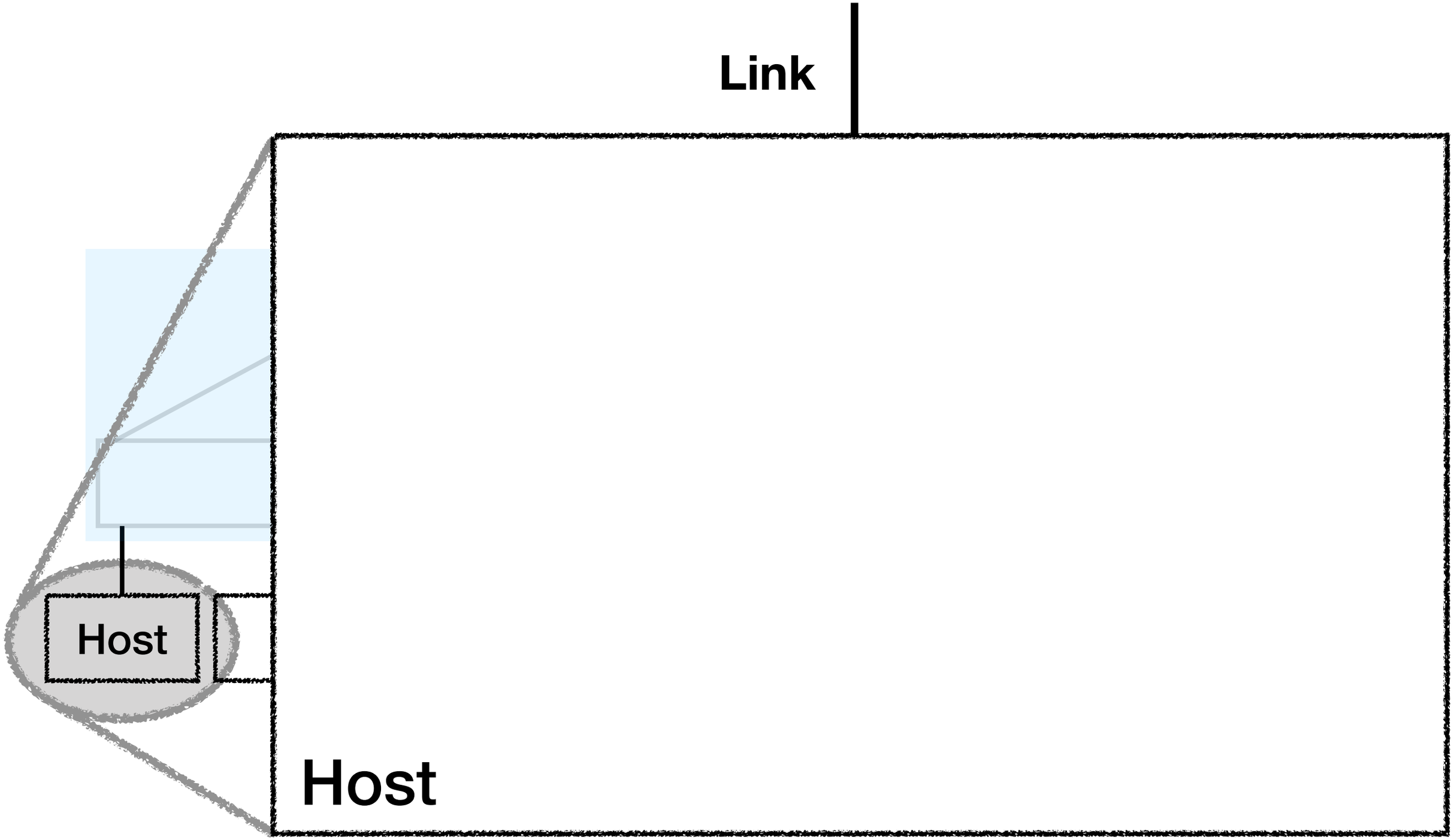

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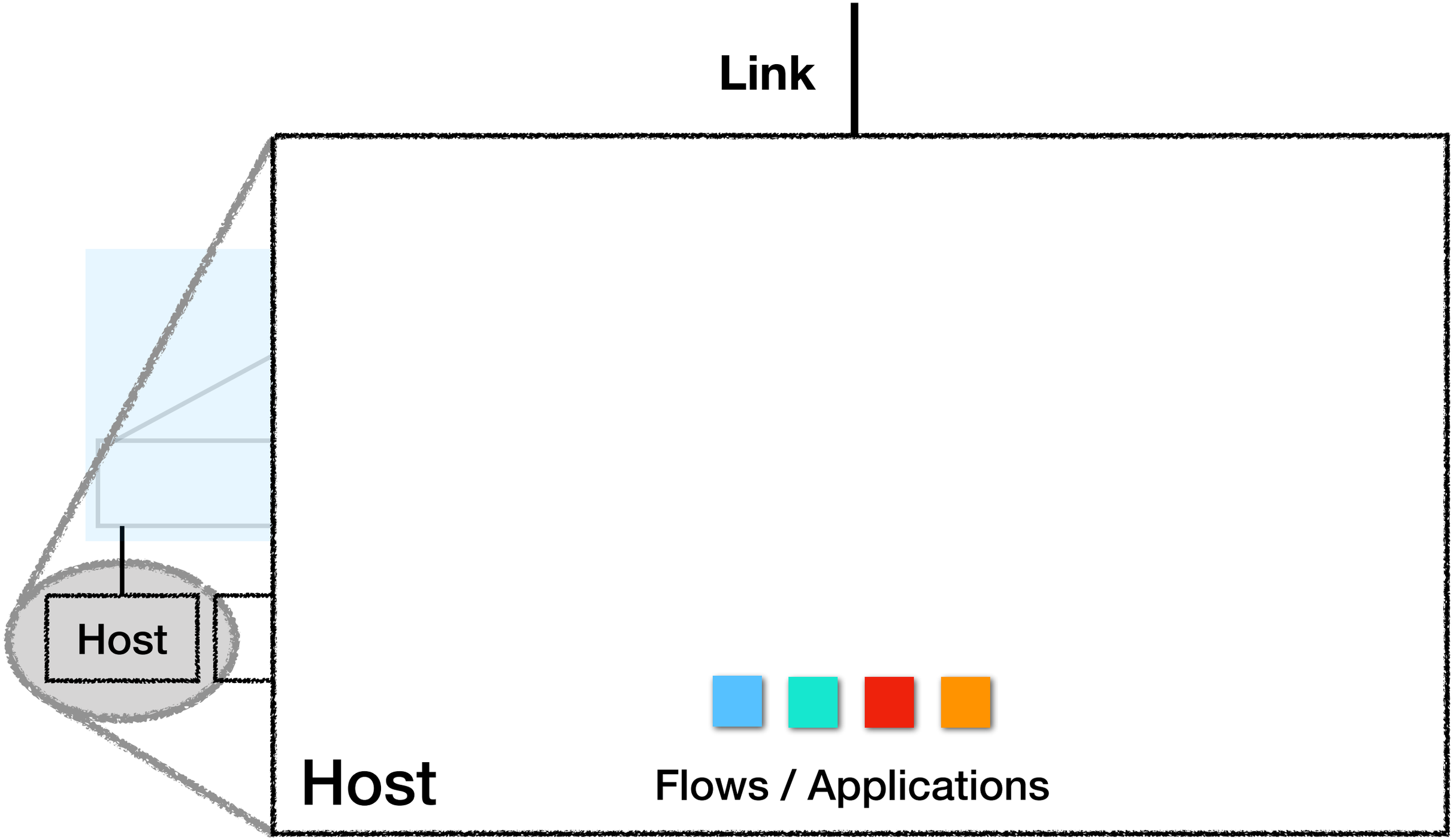

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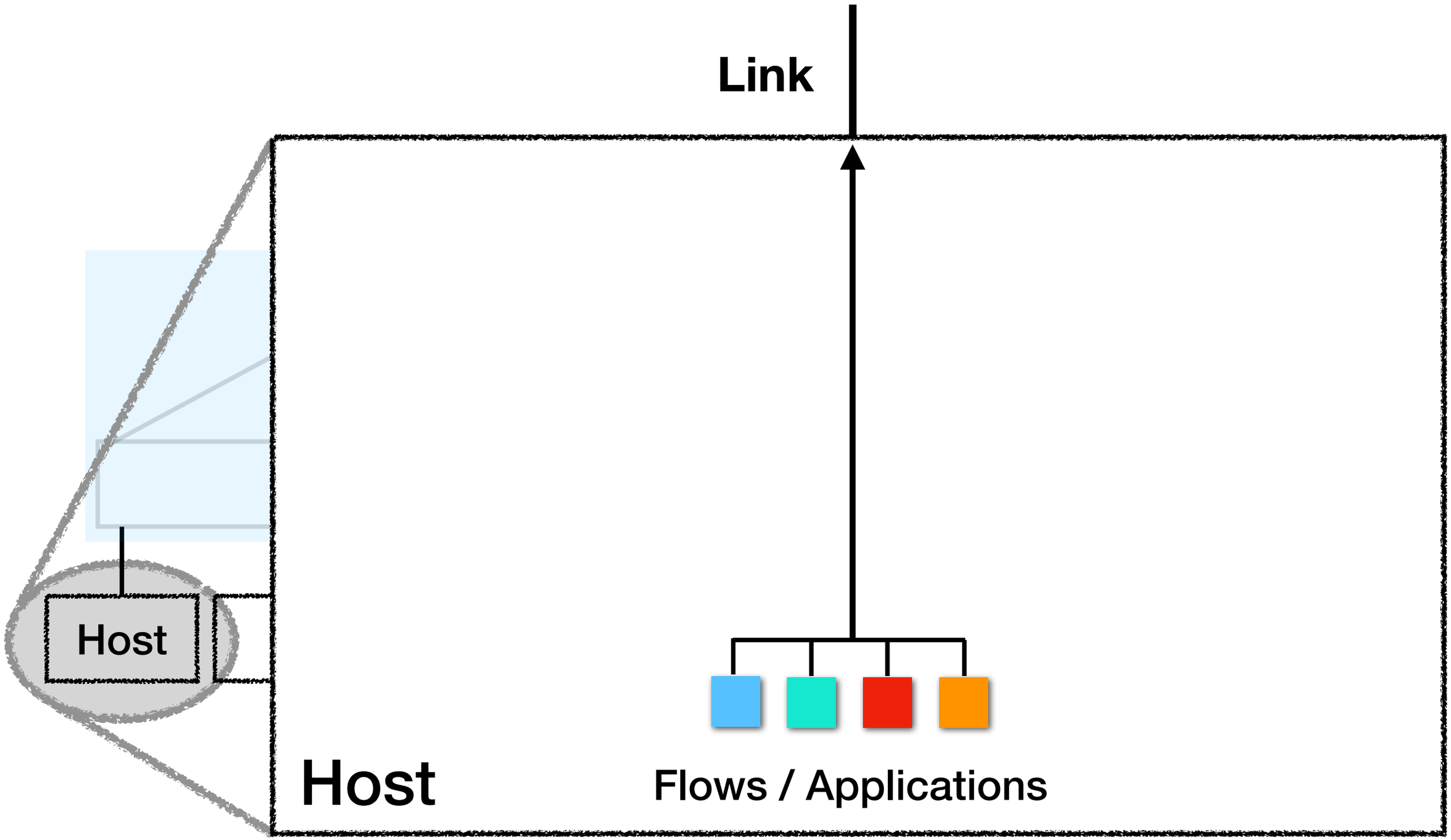

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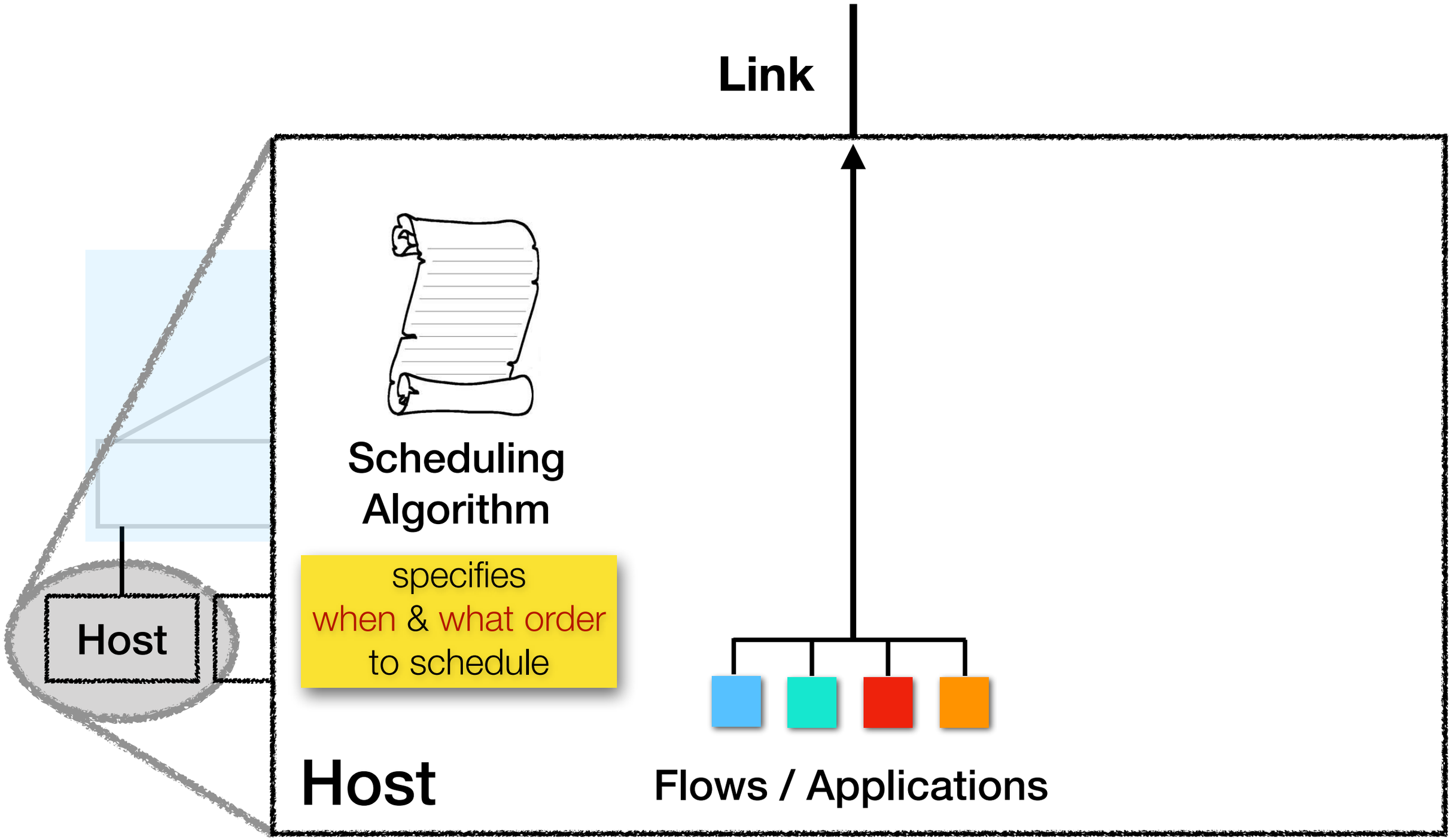

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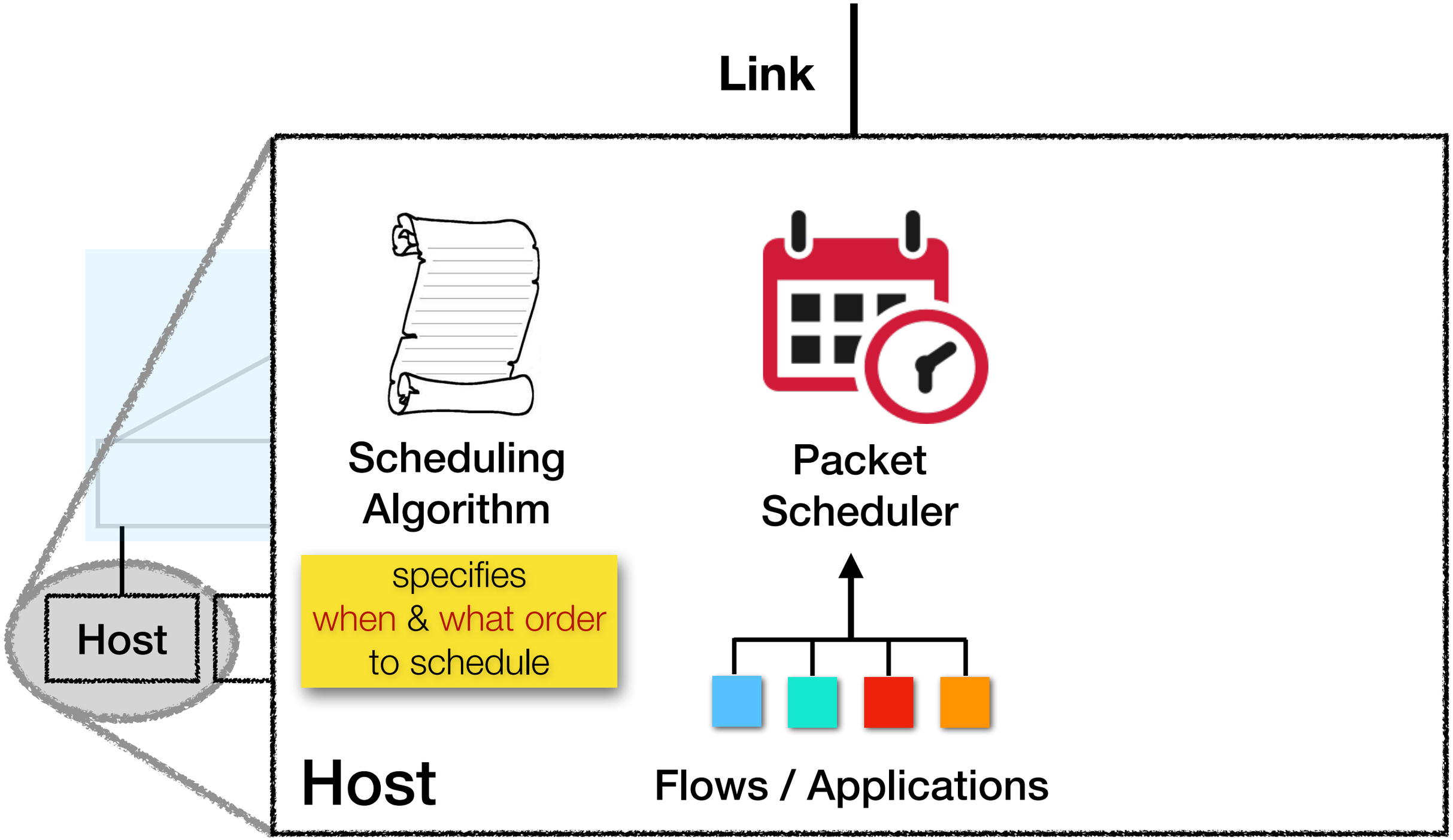

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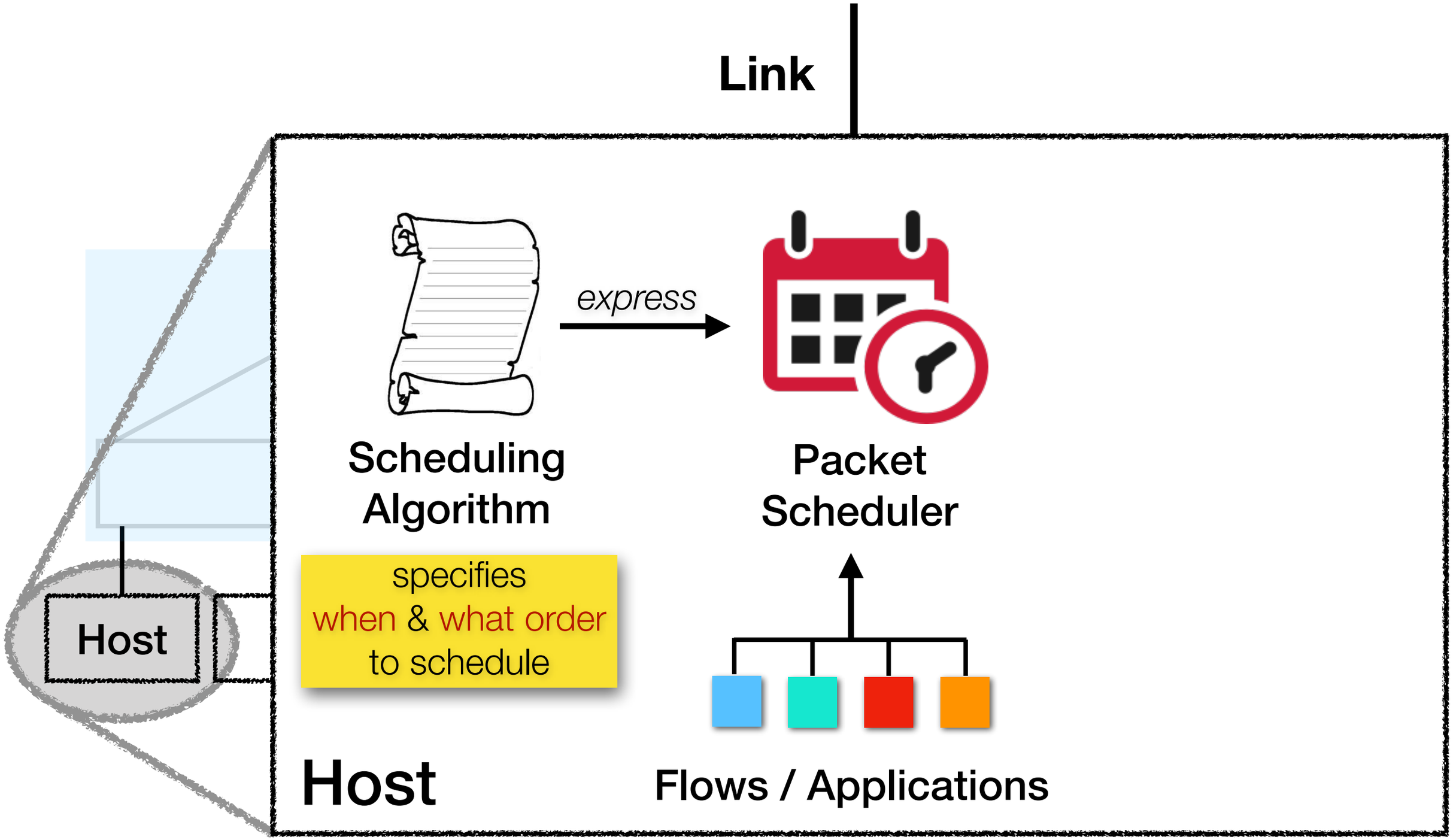

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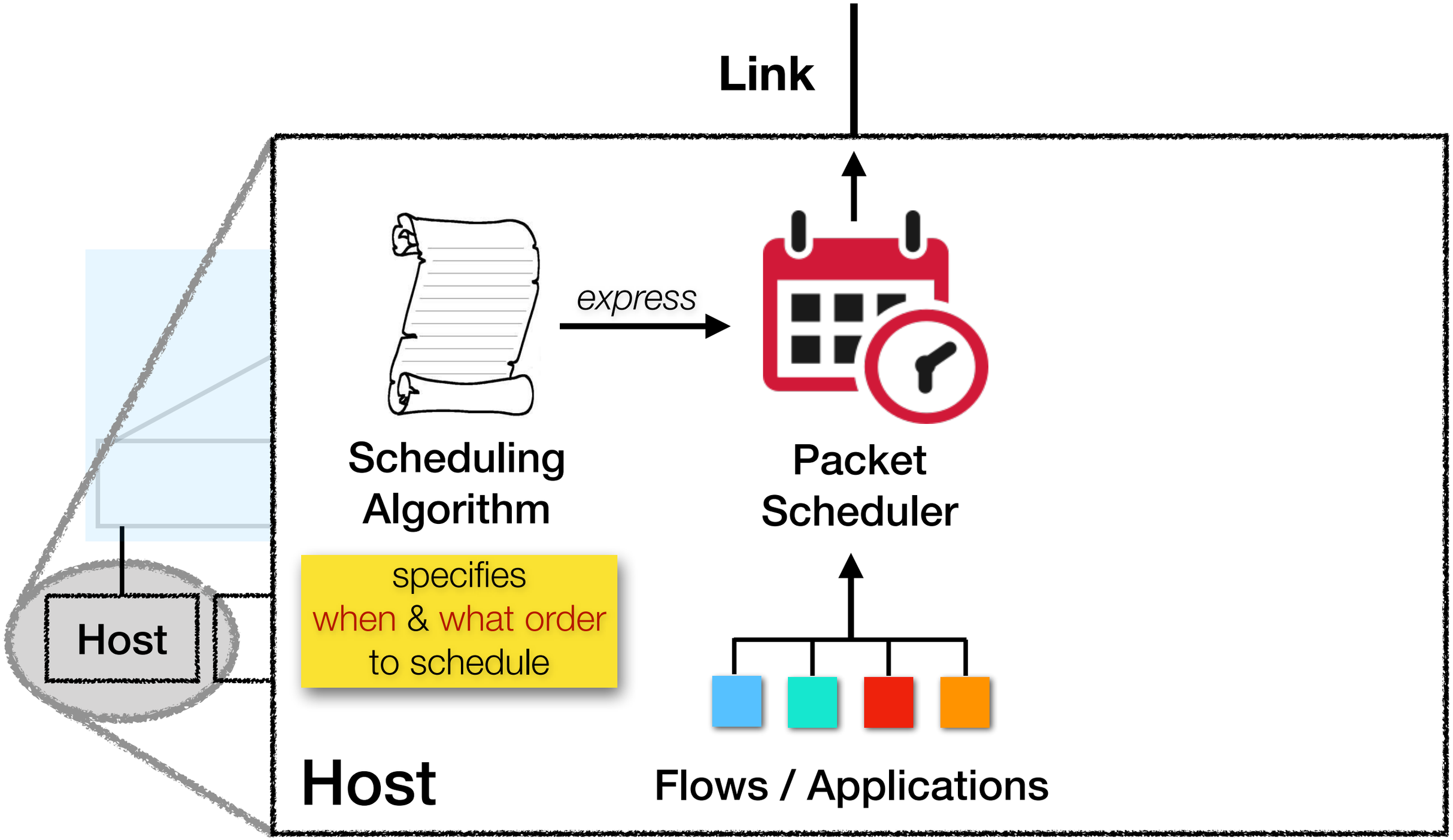

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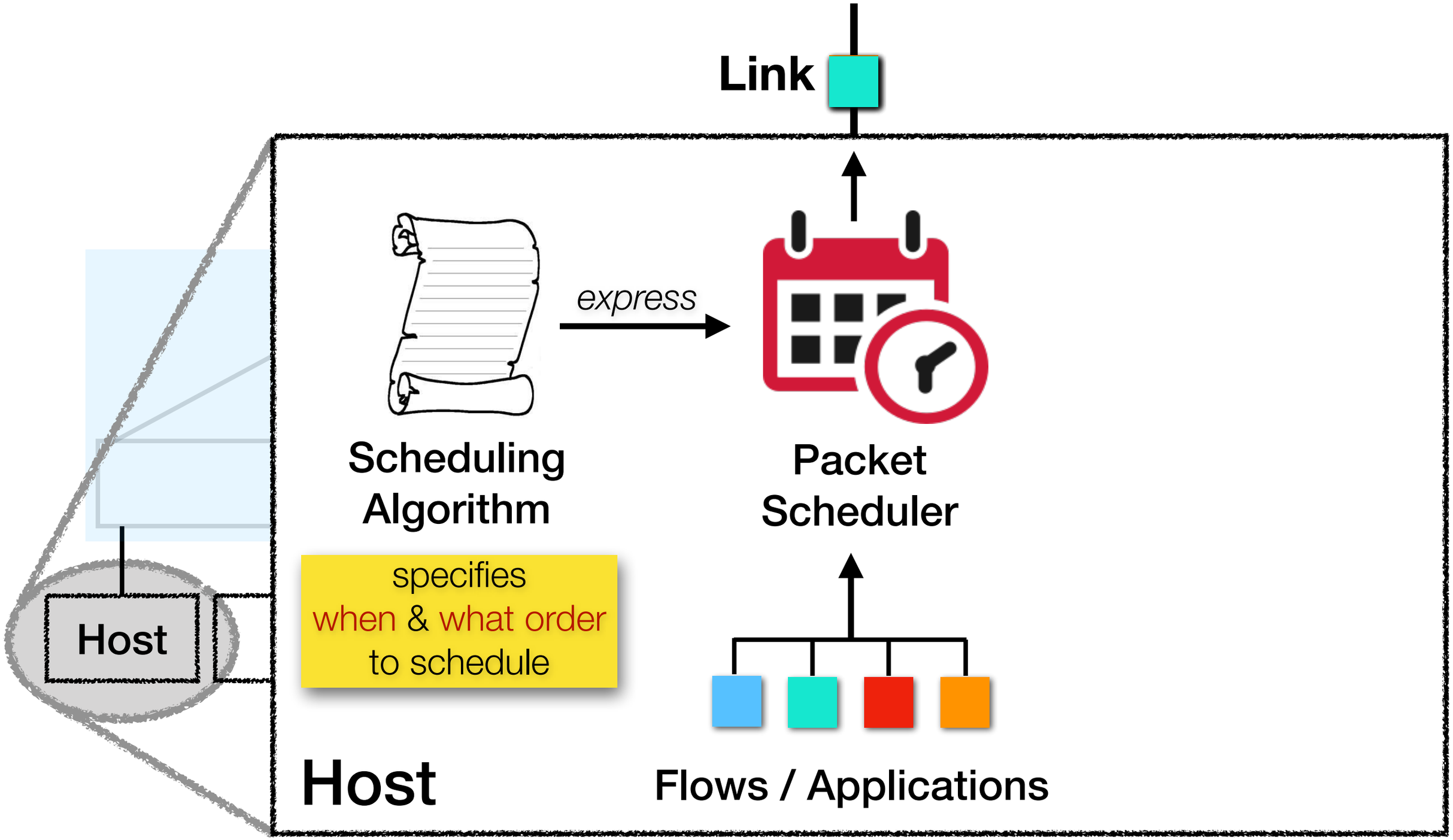

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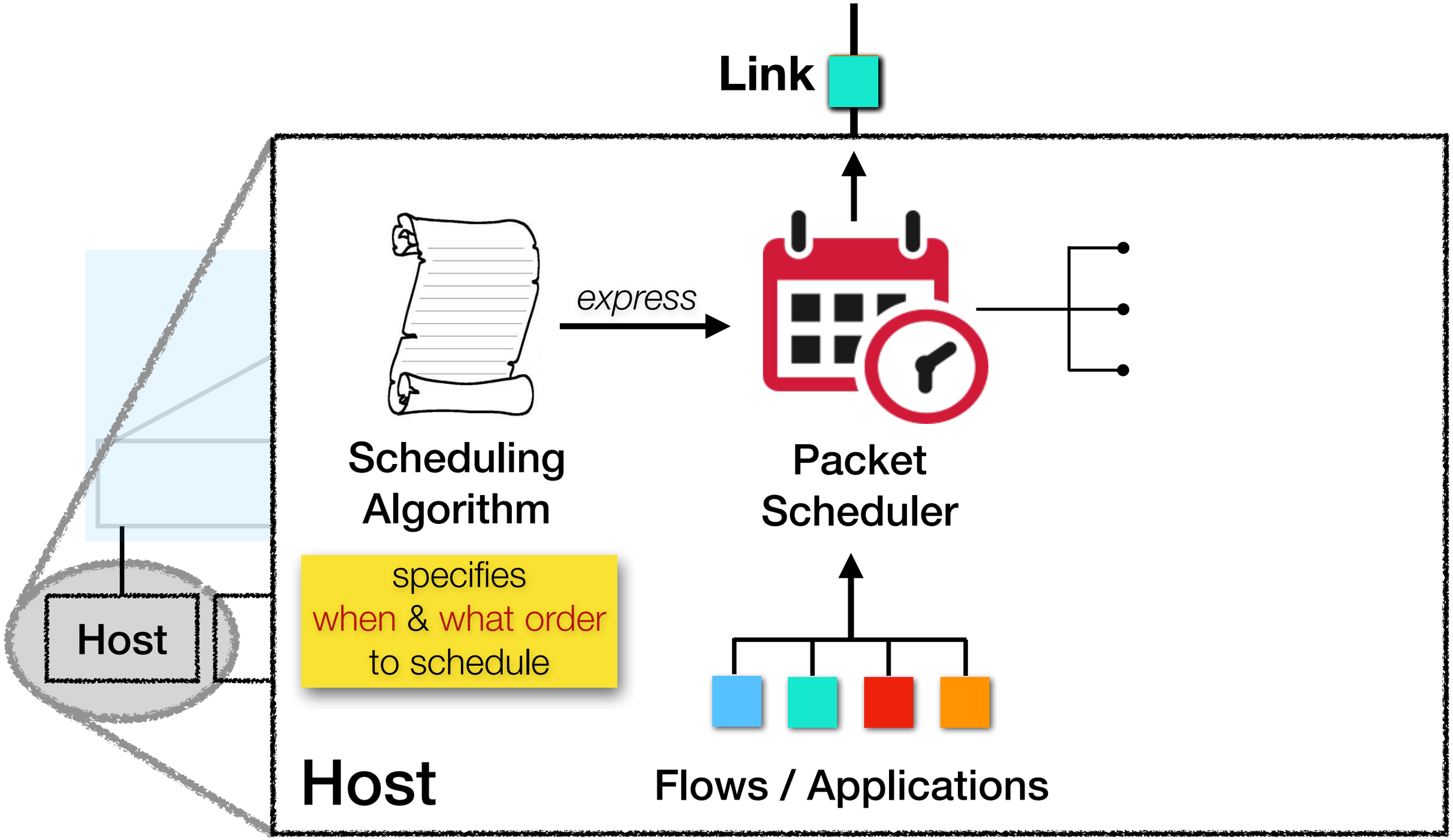

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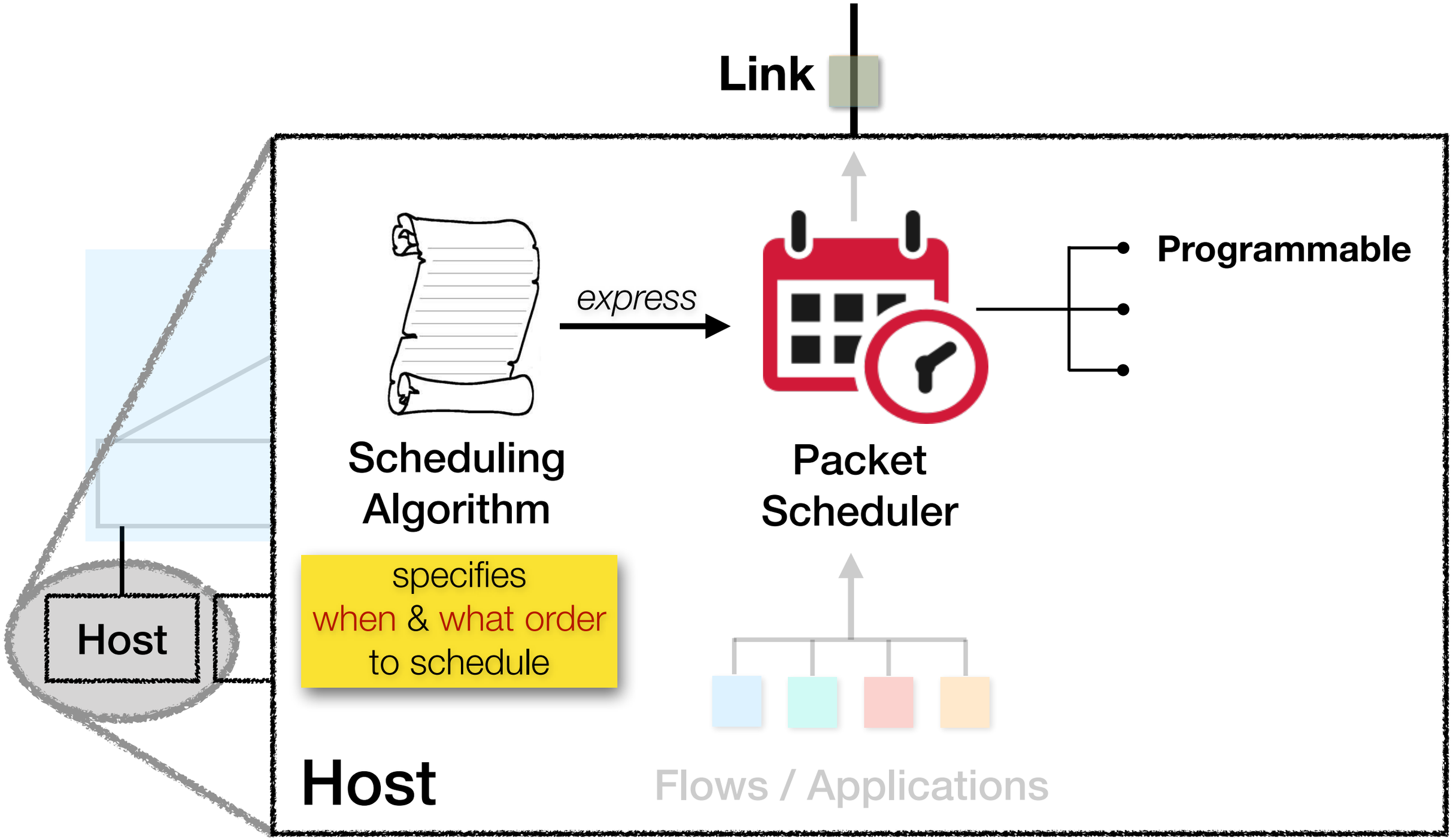

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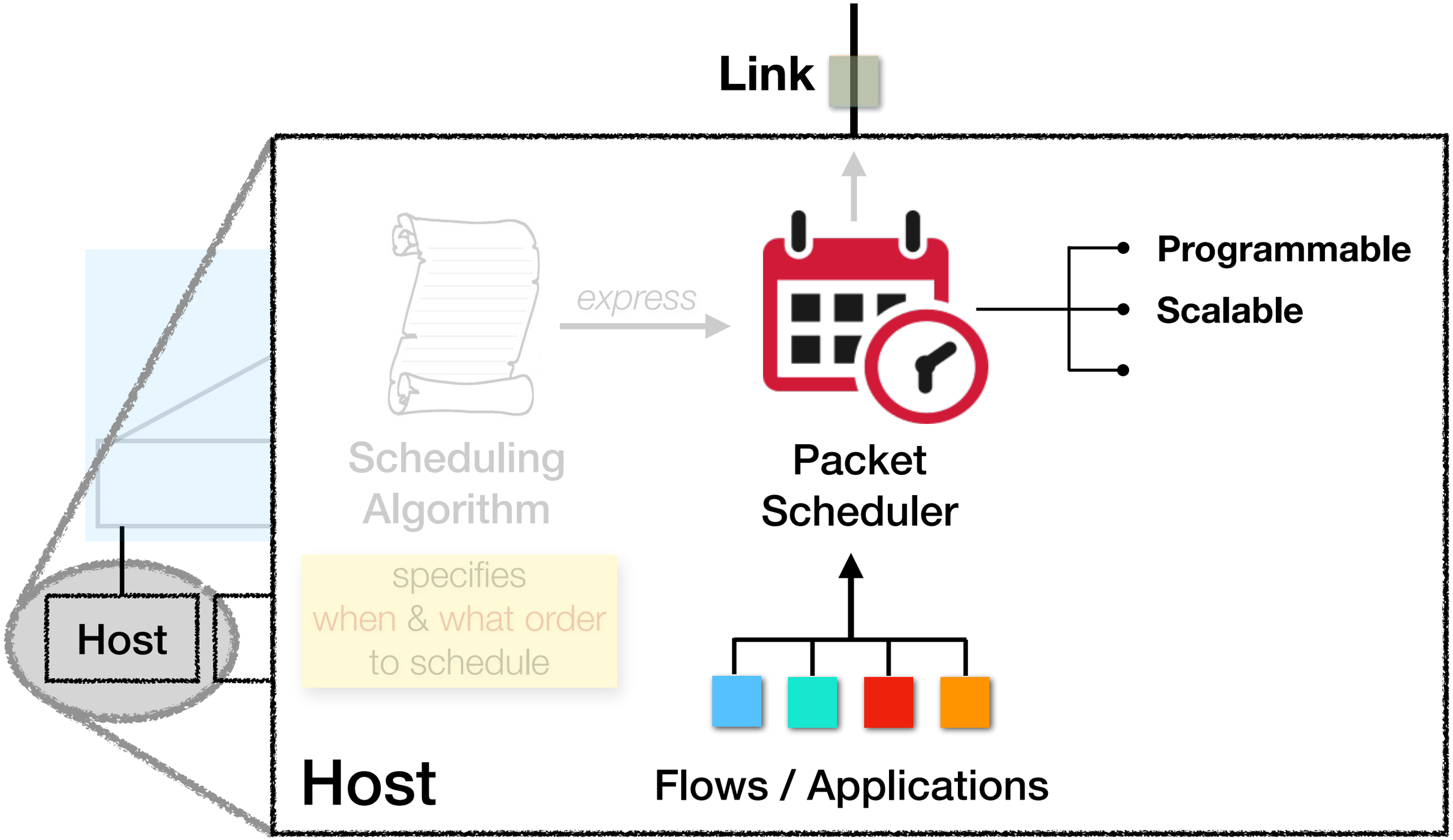

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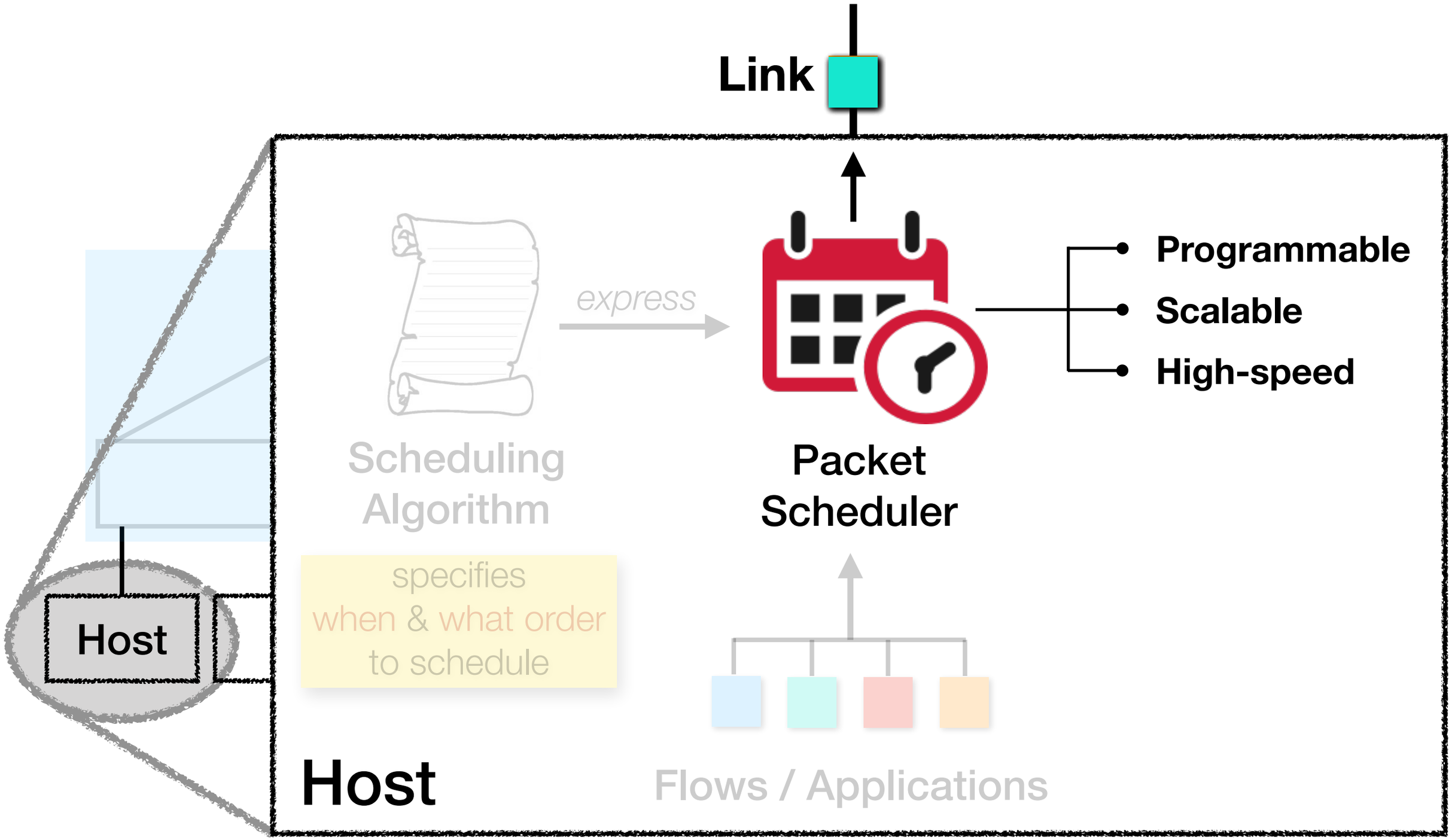
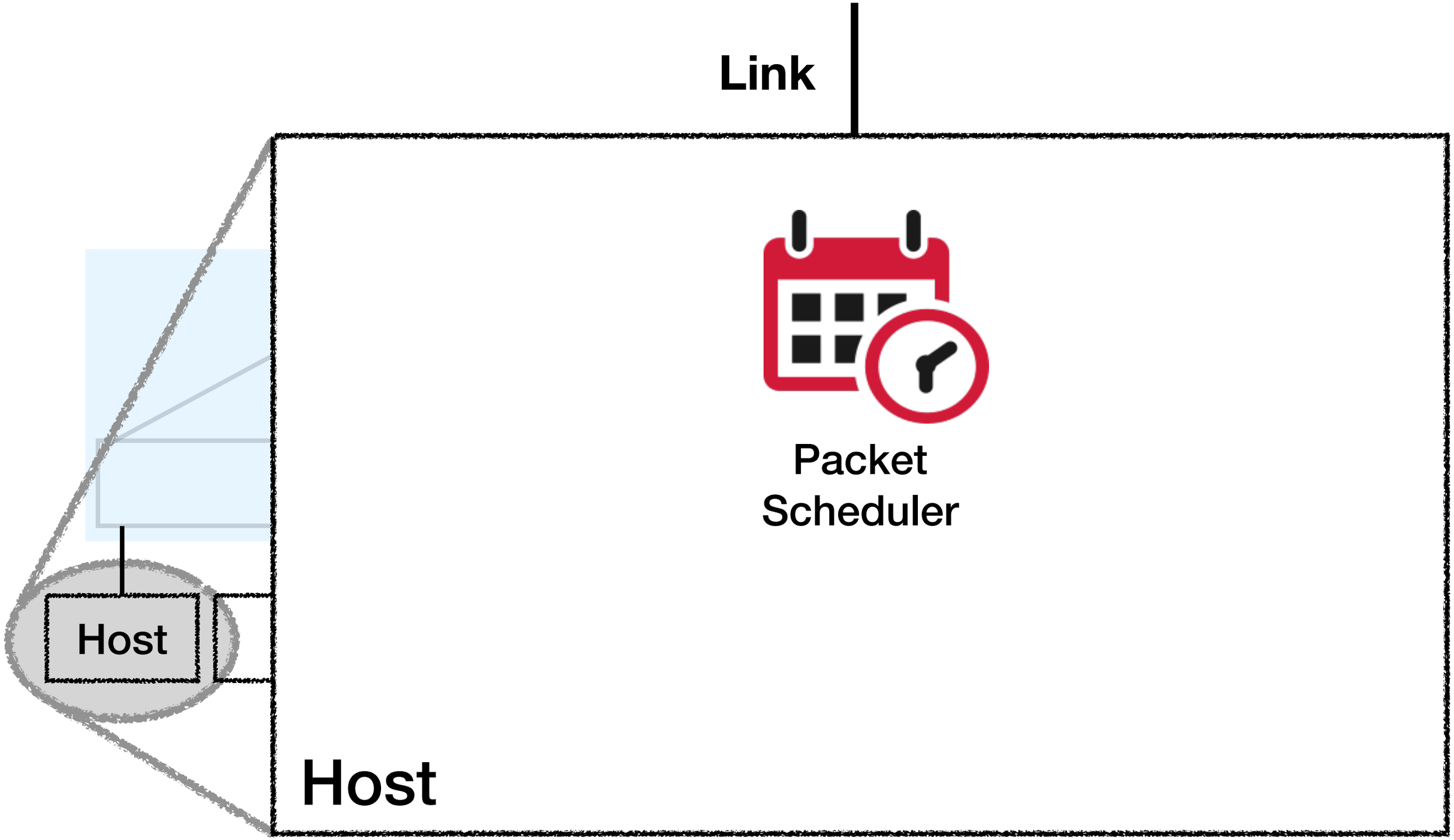


State-of-the-Art Packet Schedulers



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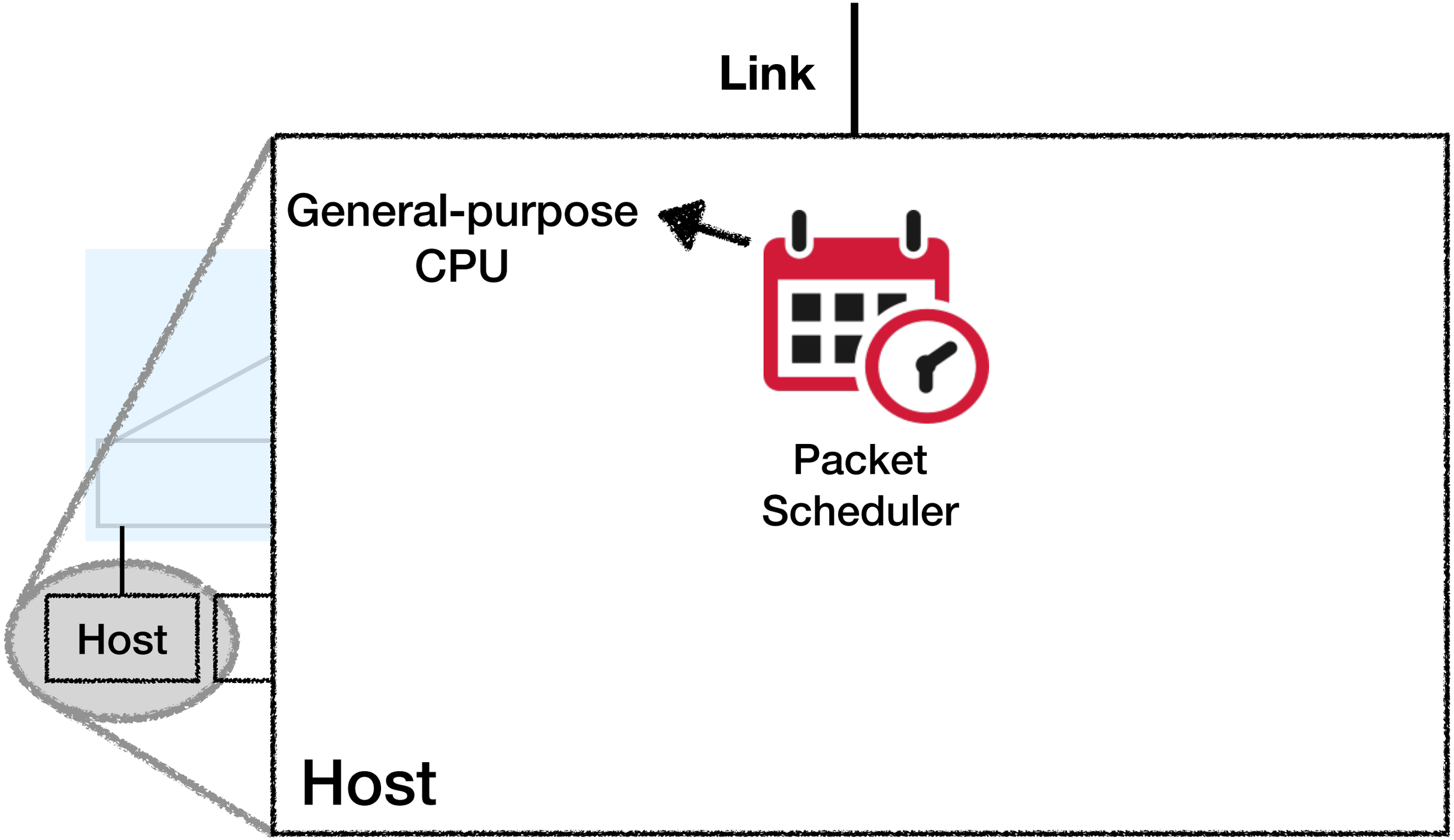

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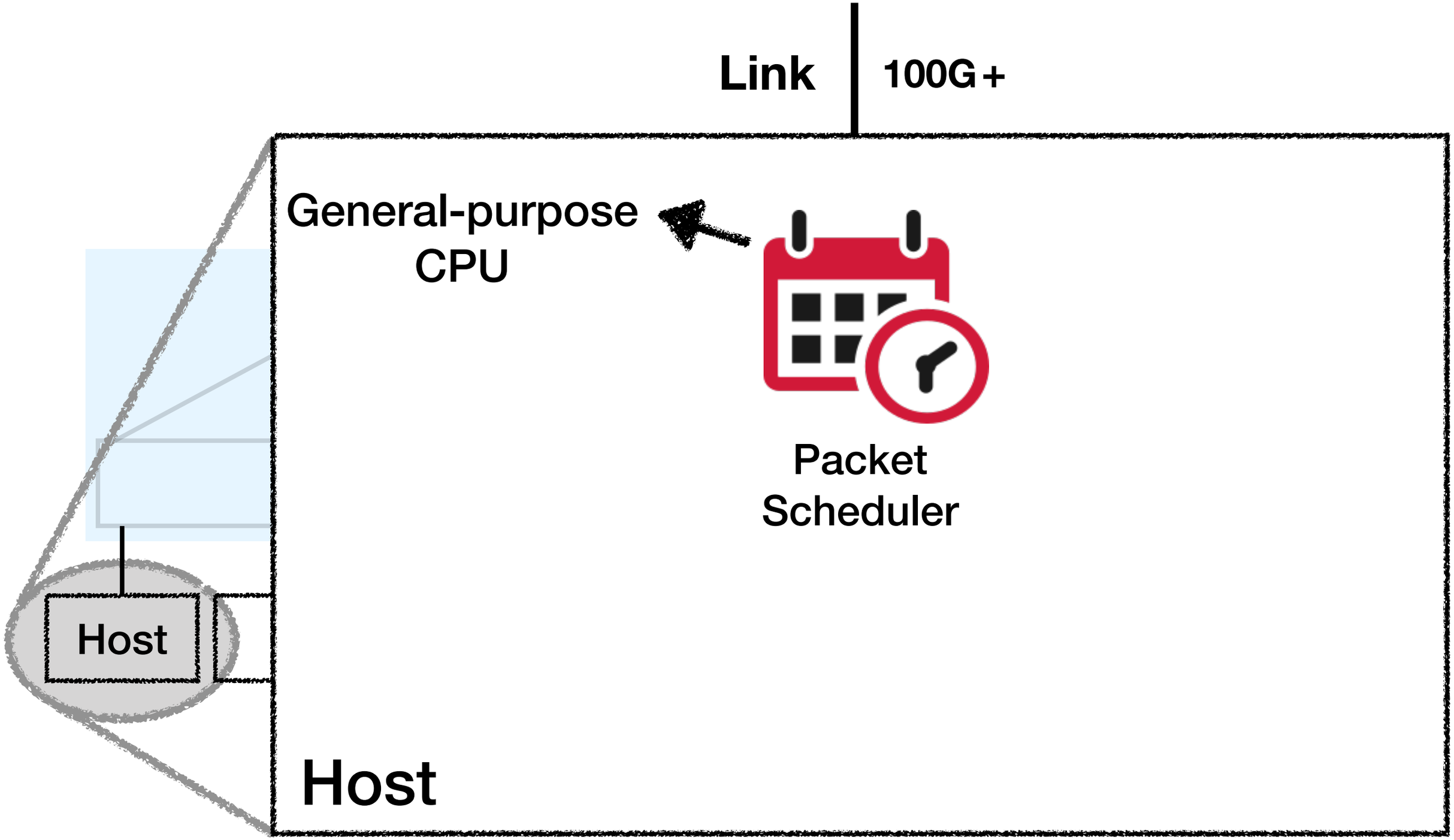

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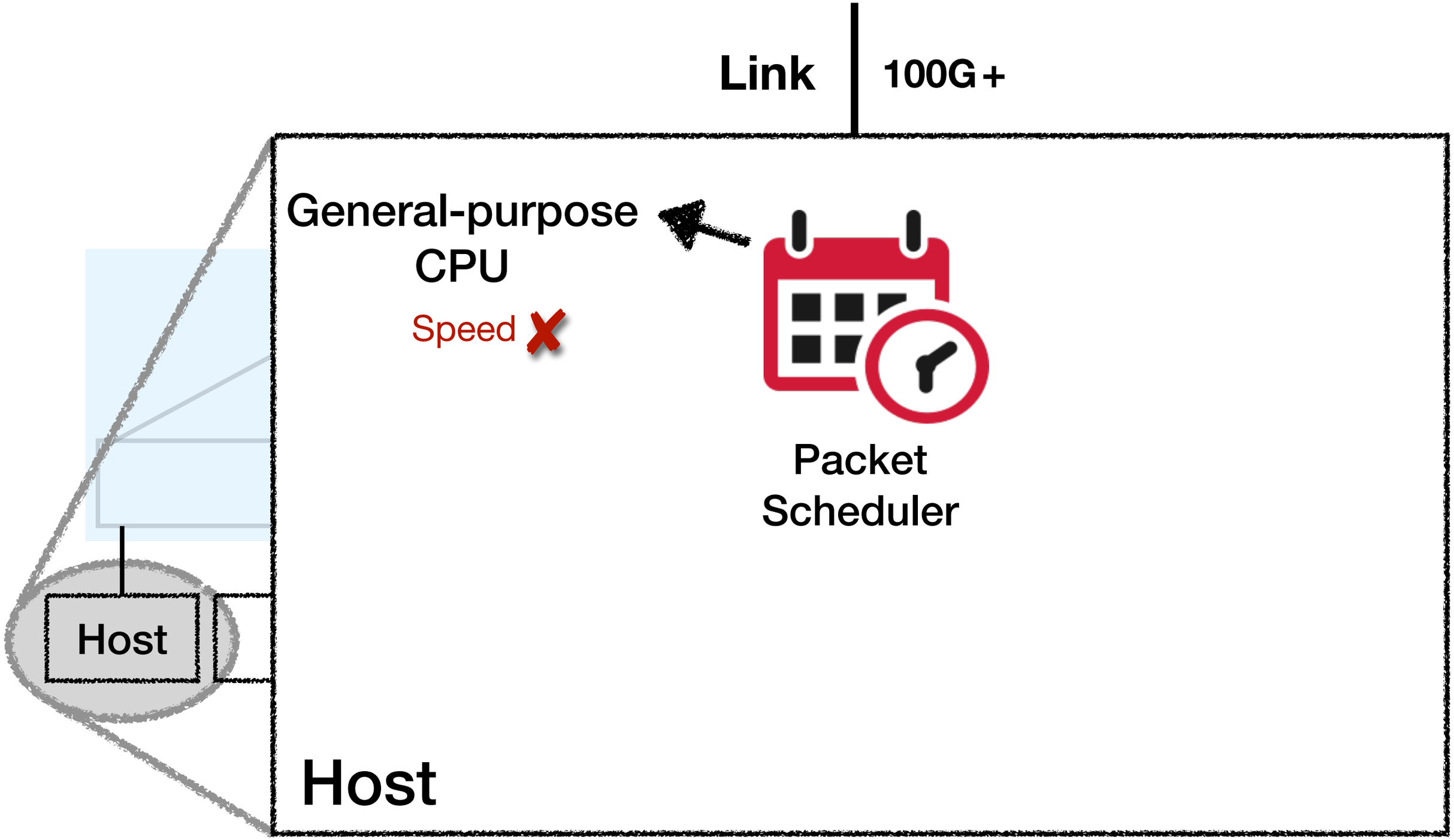

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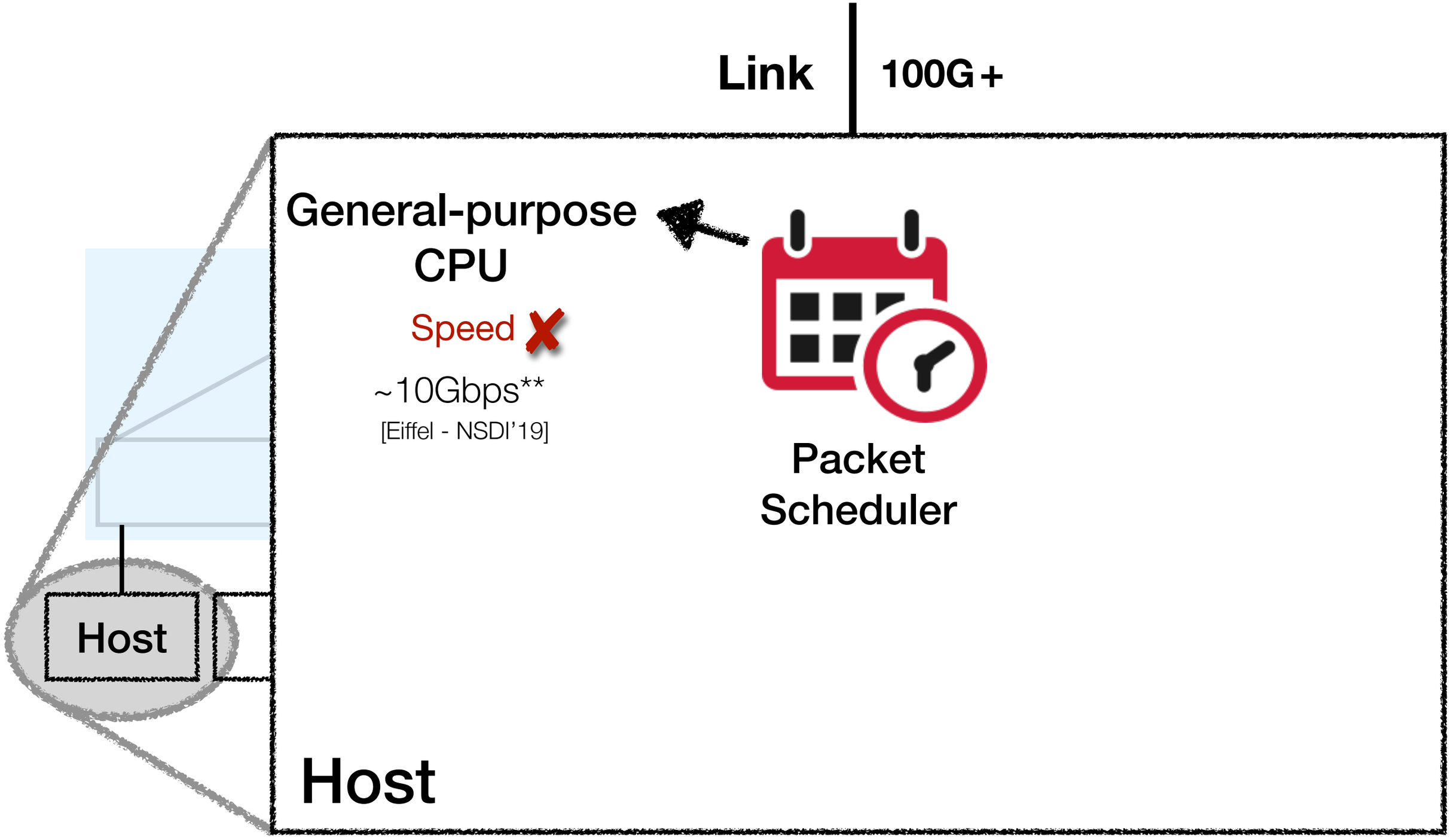

**1 core, 1500B packets, running variant of SJF algorithm

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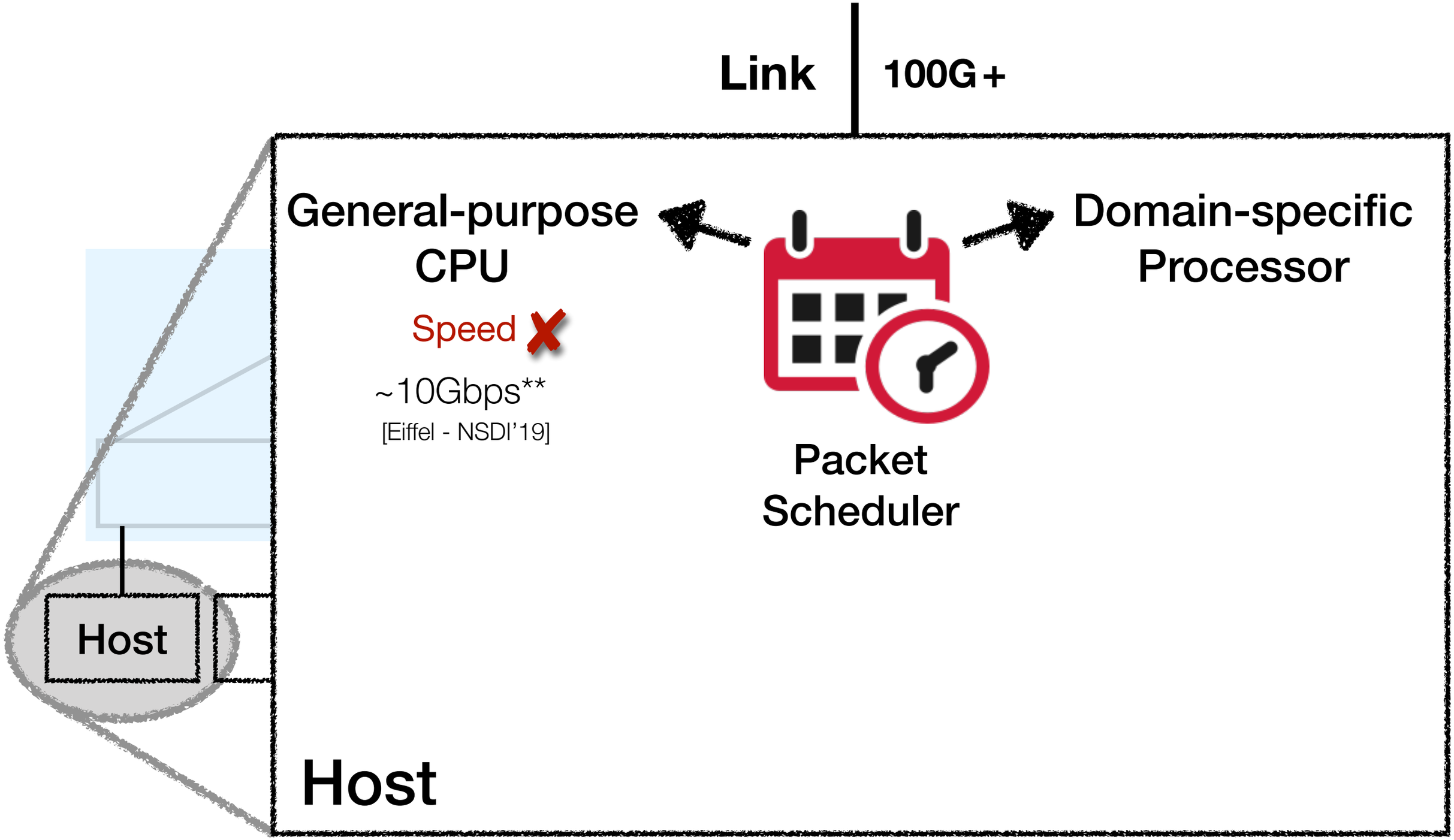

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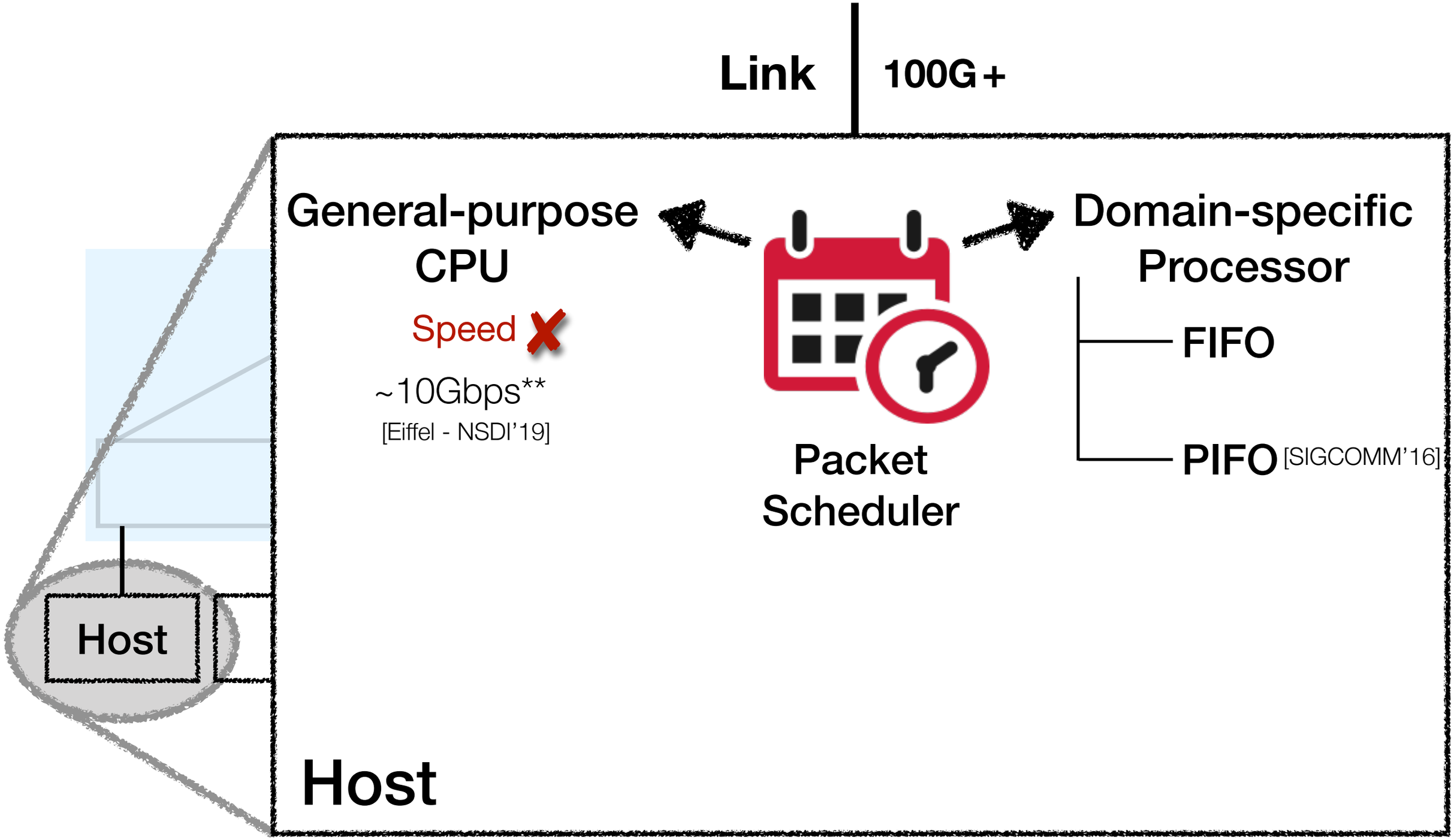

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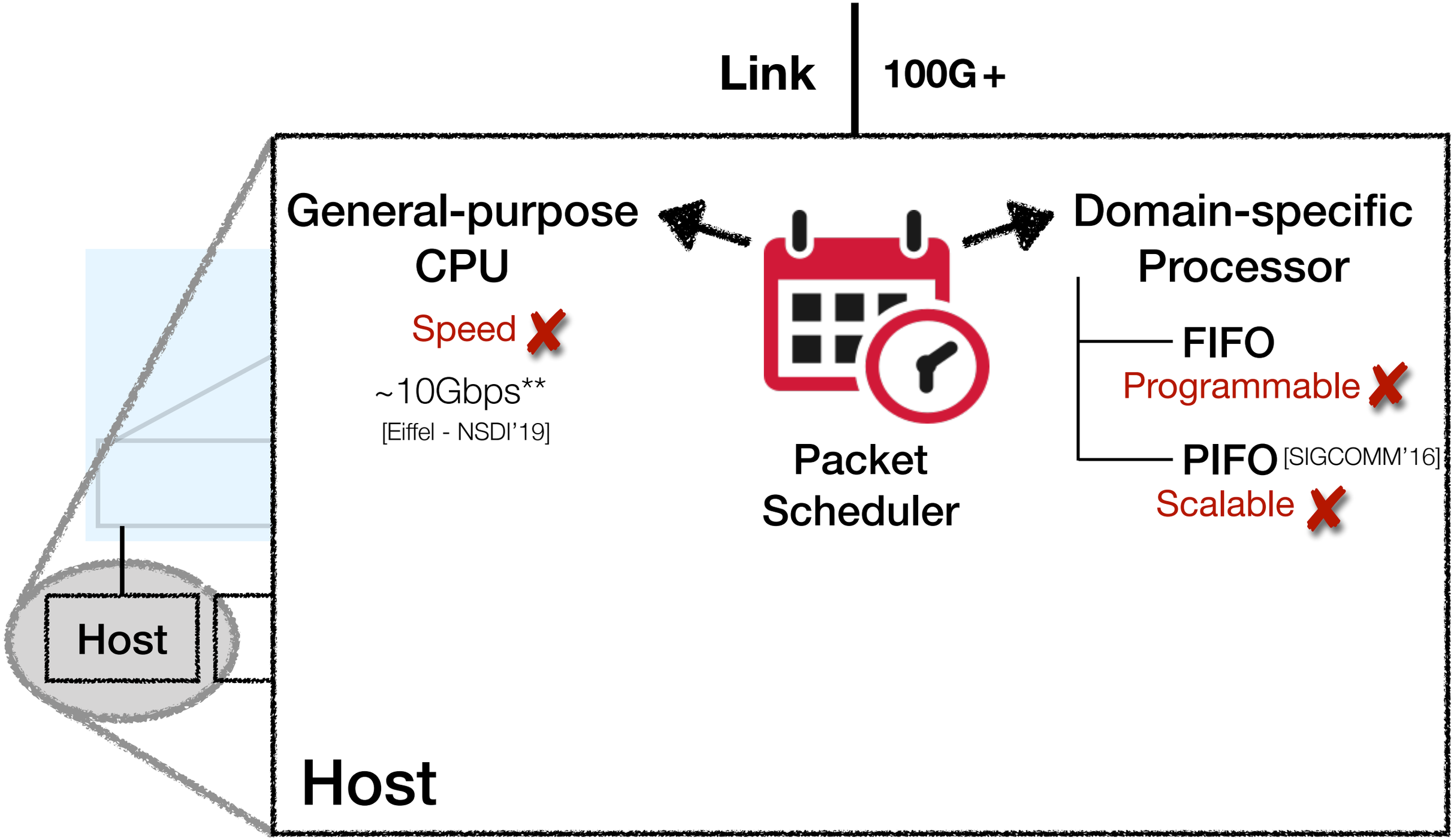

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How to build a packet scheduler that is simultaneously Programmable, Scalable, High-speed?

express wide range of packet scheduling algorithms

schedule 10s of thousands of flows

ref. [SENIC - NSDI'14]
[Carousel - SIGCOMM'17]

schedule at line rate 100G+

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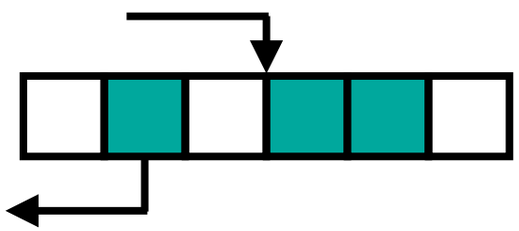

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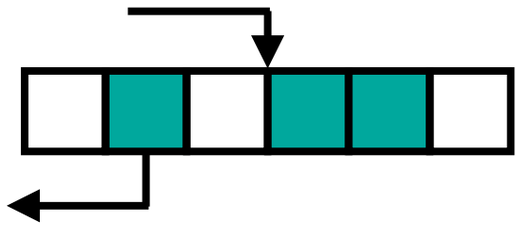

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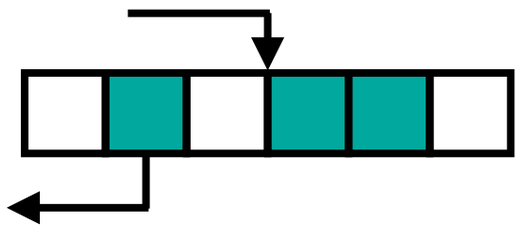

Programmable

more expressive than any state-of-the-art packet scheduling primitive

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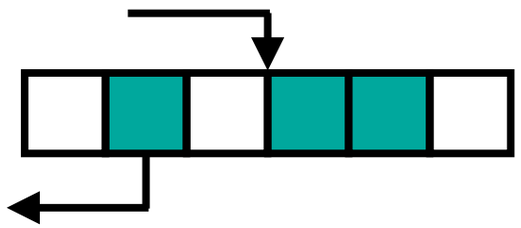

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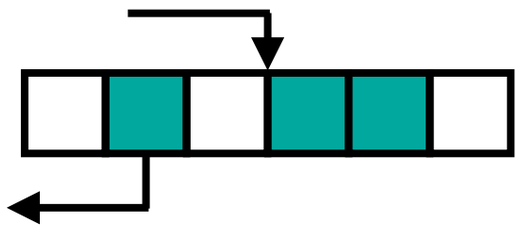
- **Scalable**
  easily scales to 10s of thousands of flows

PIEO



Programmable

more expressive than any state-of-the-art packet scheduling primitive

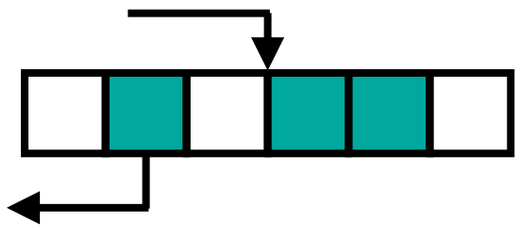
Scalable

easily scales to 10s of thousands of flows

High-speed

makes scheduling decisions in O(1) time [4 clock cycles]

PIEO



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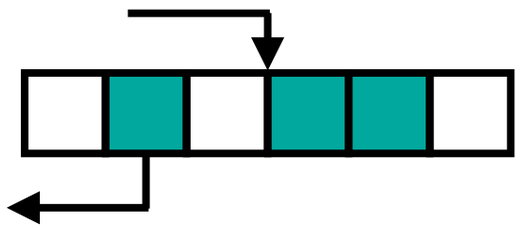

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PIEO Scheduler Abstraction

Scheduling Algorithms

PIEO Scheduler Abstraction

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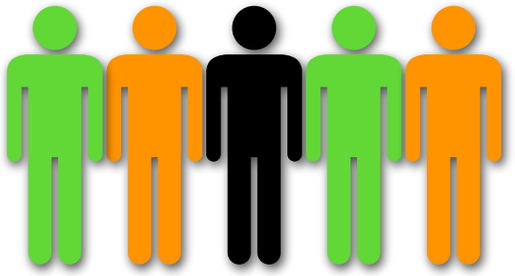
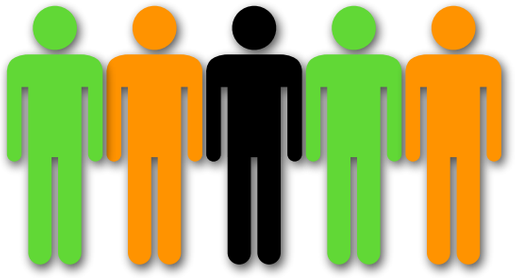


when an element becomes eligible for scheduling?

what order to schedule amongst eligible elements?

PIEO Scheduler Abstraction

Scheduling Algorithms



when an element becomes eligible for scheduling?

encode using a $t_{eligible}$ value

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encode using a $rank$ value

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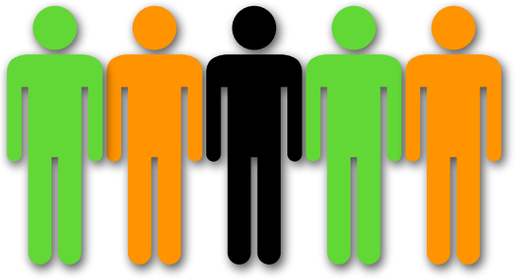

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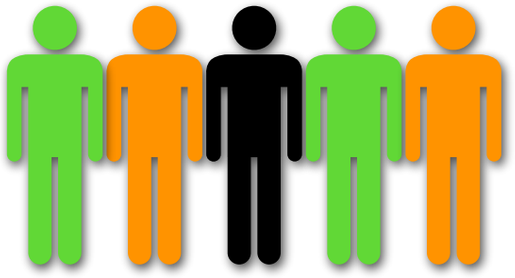

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PIEO scheduler simply schedules the smallest ranked eligible element at any given time

Push-In-Extract-Out Primitive

Push-In-Extract-Out Primitive

programmed based on the choice of scheduling algorithm

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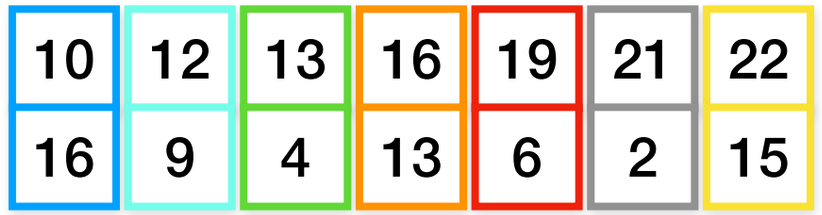
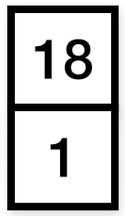
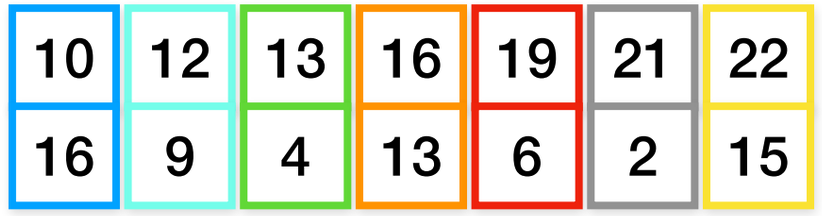
element

ordered list

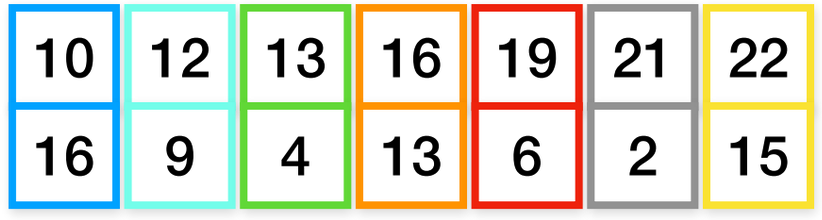
increasing rank value

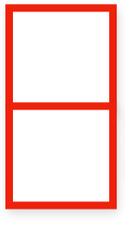


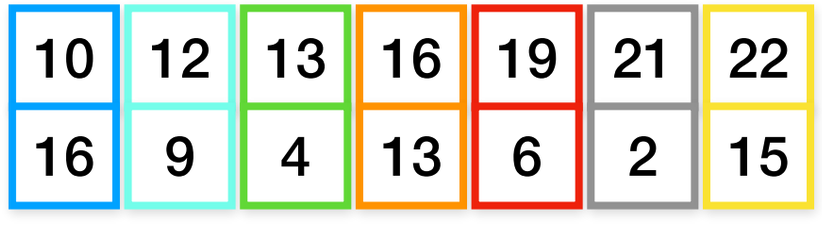
enqueue()



dequeue( )



dequeue()



Push-In-Extract-Out Primitive

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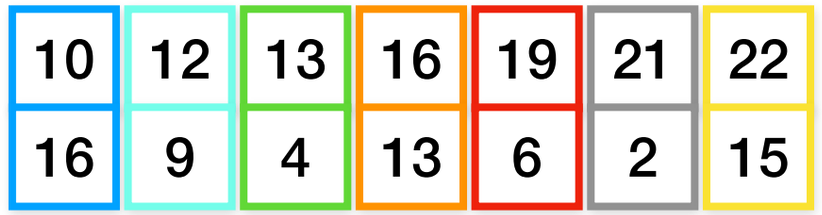
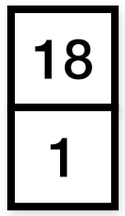
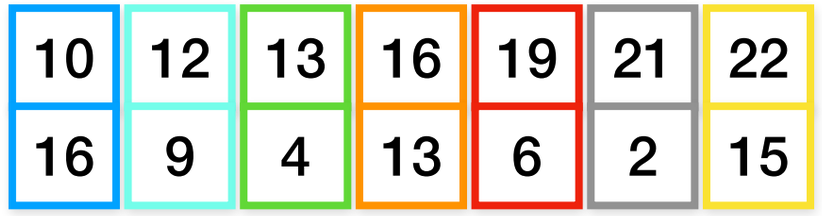


enqueue() "Push-In"

inserts element at position dictated by its rank value



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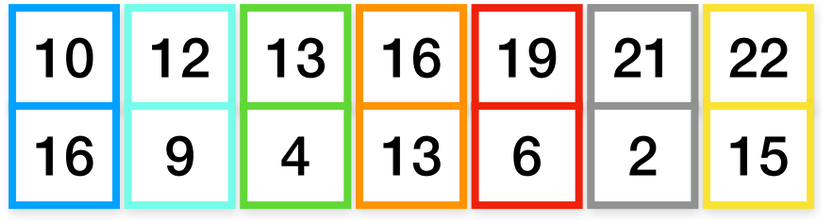
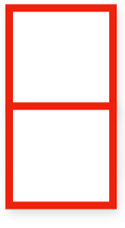
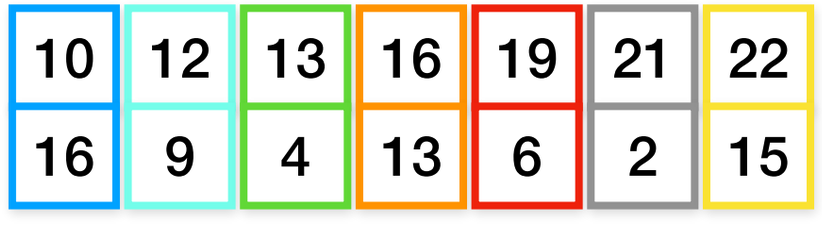


dequeue()



Push-In-Extract-Out Primitive

programmed based on the choice of scheduling algorithm

element: rank, $t_{eligible}$

ordered list — increasing rank value

10	12	13	16	19	21	22
16	9	4	13	6	2	15

enqueue(18 / 1) “Push-In”

inserts element at position dictated by its rank value

10	12	13	16	18	19	21	22
16	9	4	13	1	6	2	15

dequeue( )

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returns "smallest ranked eligible" element

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13
4

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dequeue( )

returns a specific element

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13 / 4

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19 / 6

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Expressiveness of PIEO

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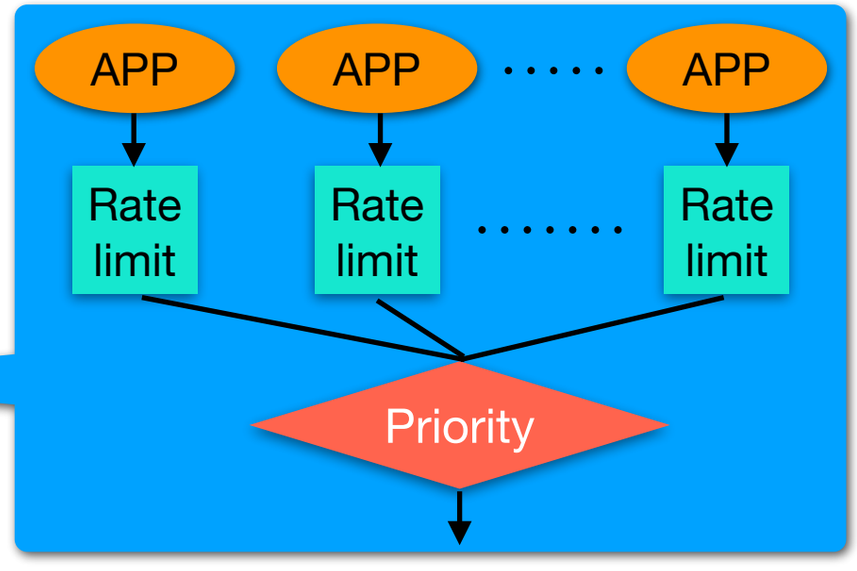
- Work conserving
  - e.g., DRR, WFQ, WF^2Q
- Non-work conserving
  - e.g., Token Bucket, RCSP
- Hierarchical scheduling
  - e.g., HPFQ
- Asynchronous scheduling
  - e.g., Starvation avoidance, D^3
- Priority scheduling
  - e.g., SJF, SRTF, LSTF, EDF
- Complex scheduling policies
  - mixture of shaping and ordering

e.g.



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at time x, all elements s.t. **virtual_time(x) >= start_time:**
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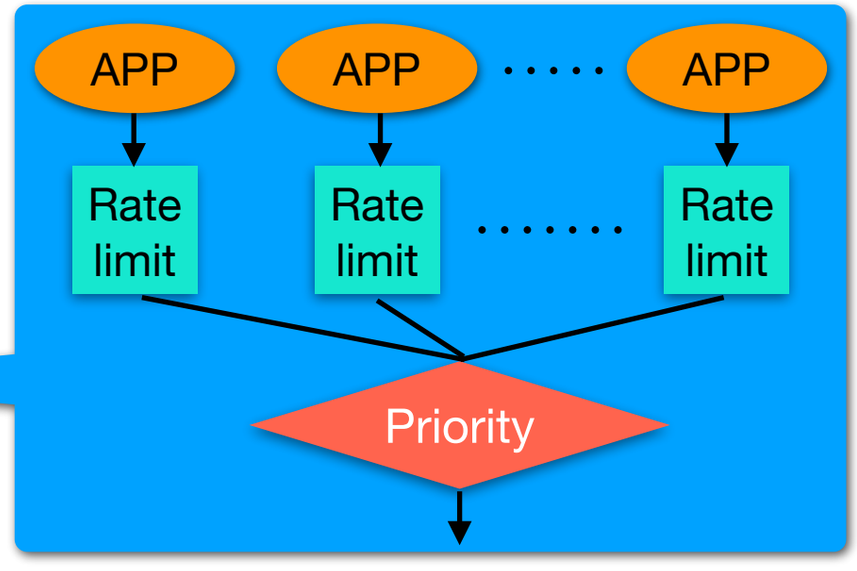

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programming PIEO

$rank = finish\_time$

$t_{eligible} = start\_time$

Predicate for filtering at dequeue at time x:

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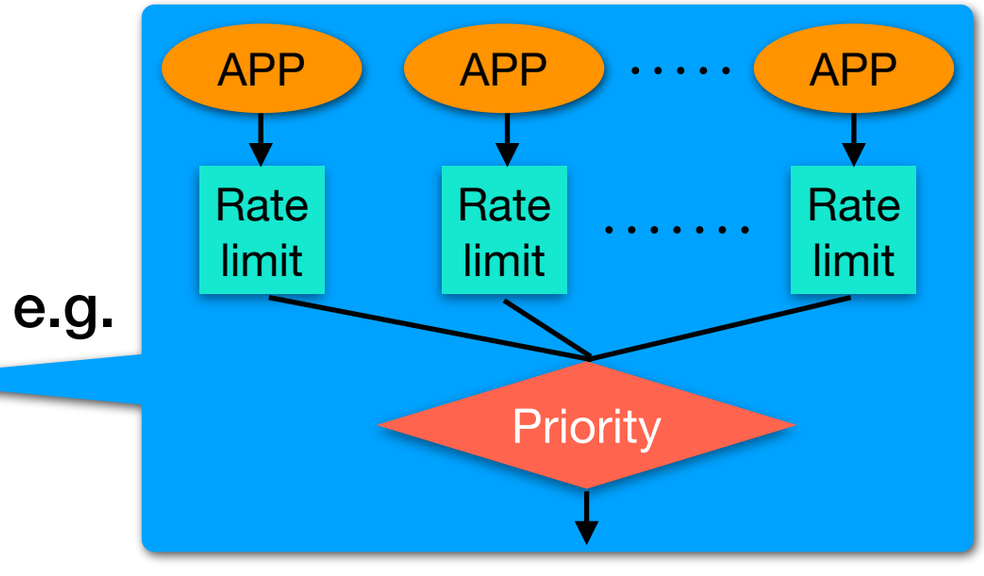

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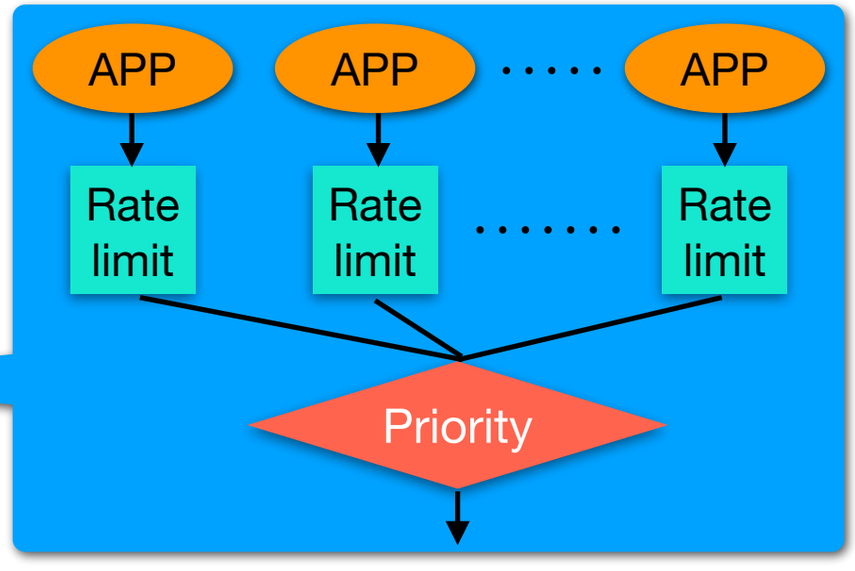
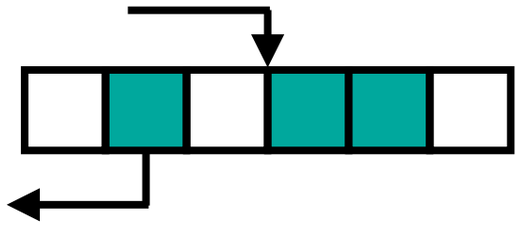


cannot express accurately using state-of-the-art (PIFO)

PIEO



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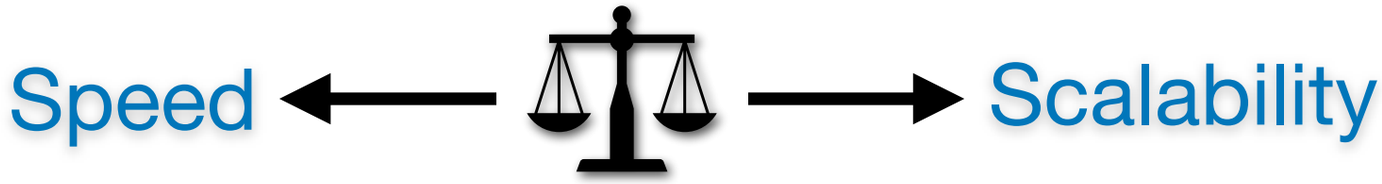

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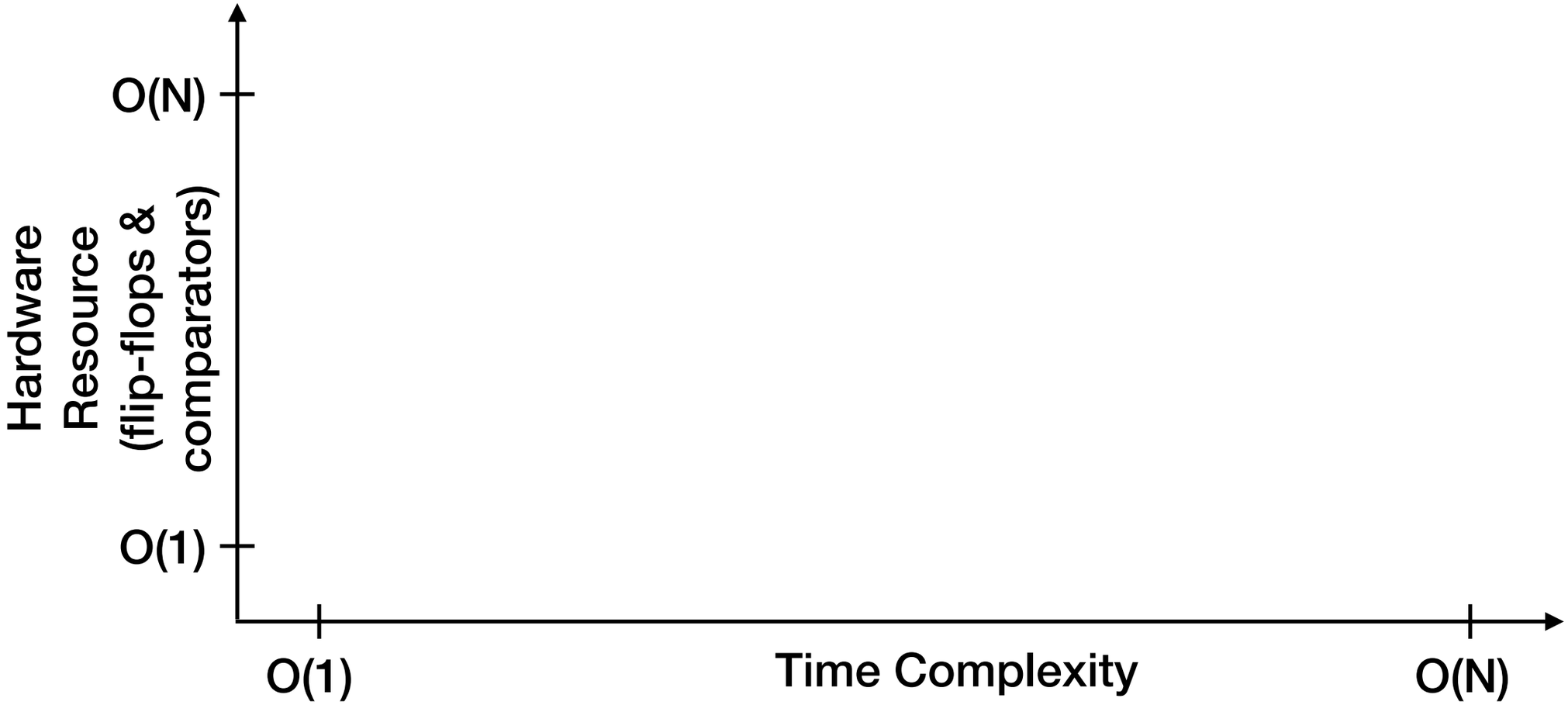
Speed ⟵ ⚖ ⟶ Scalability



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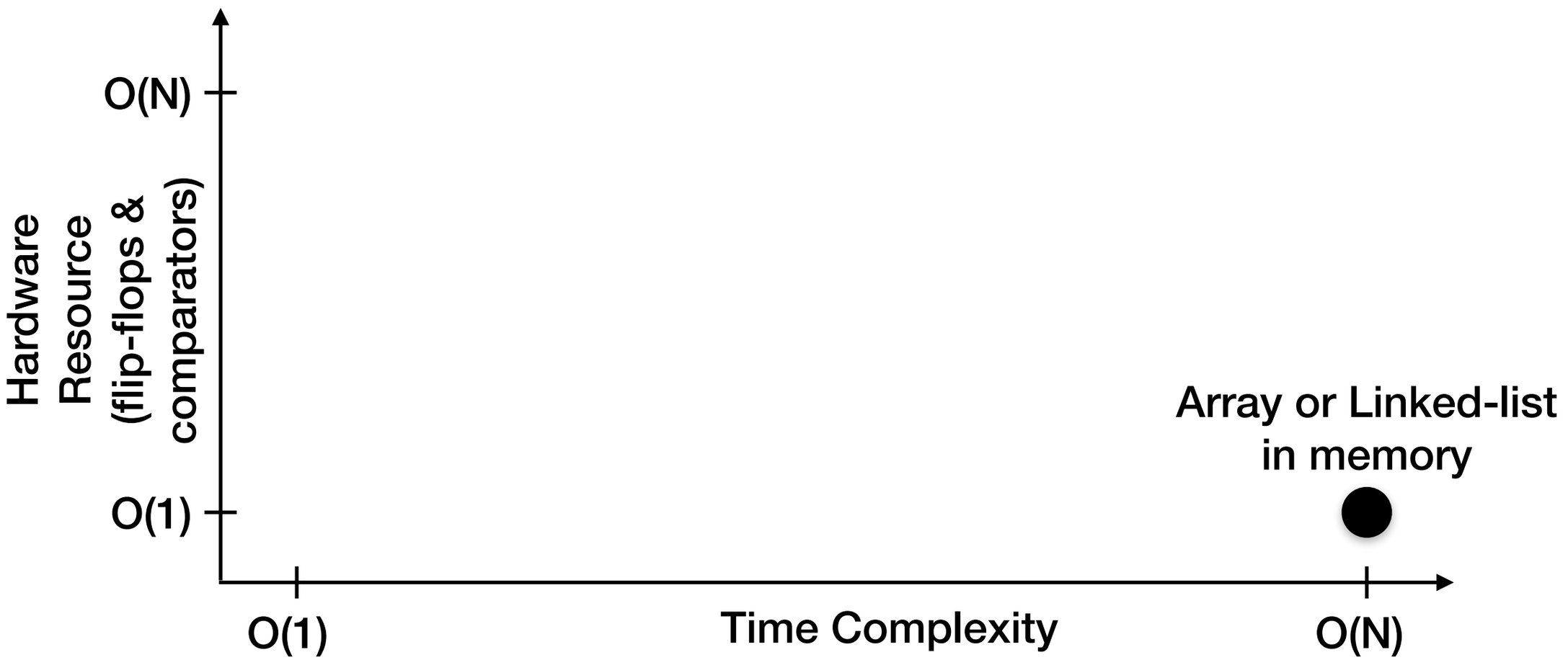

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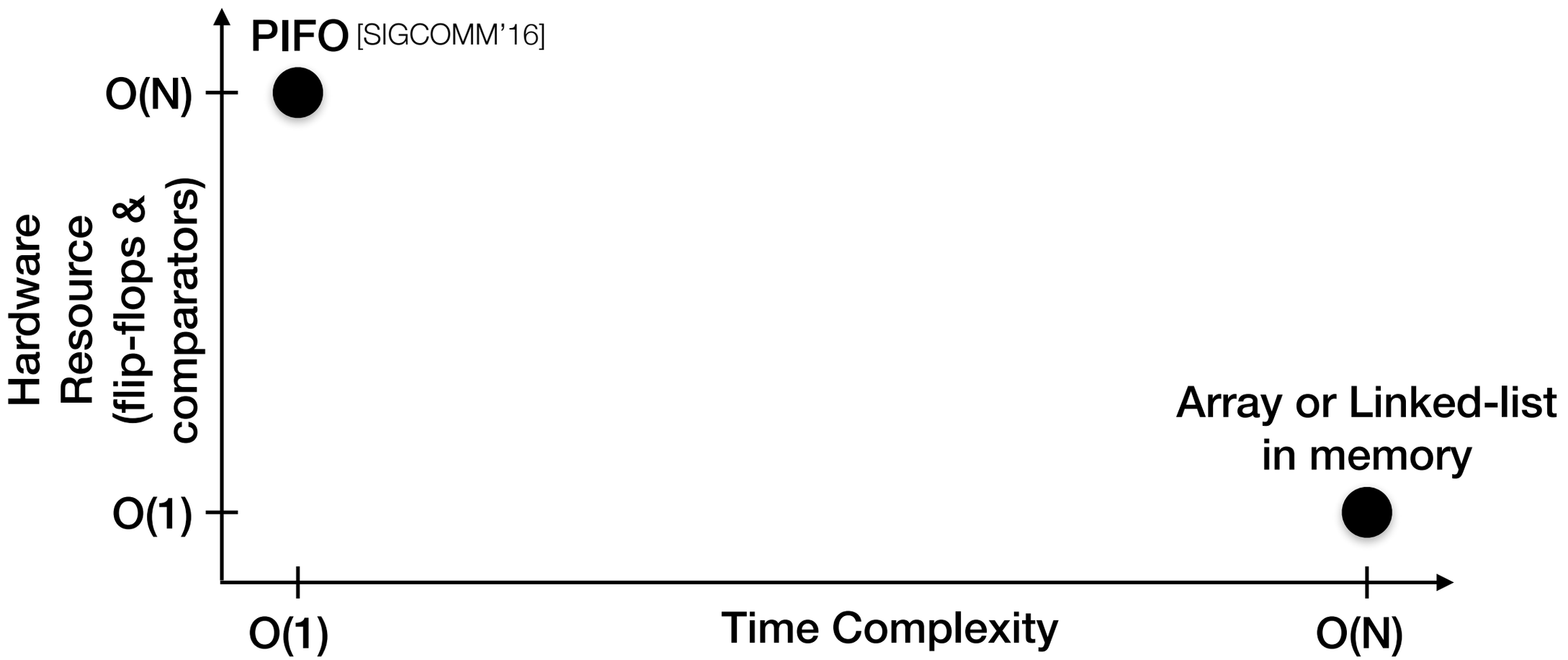

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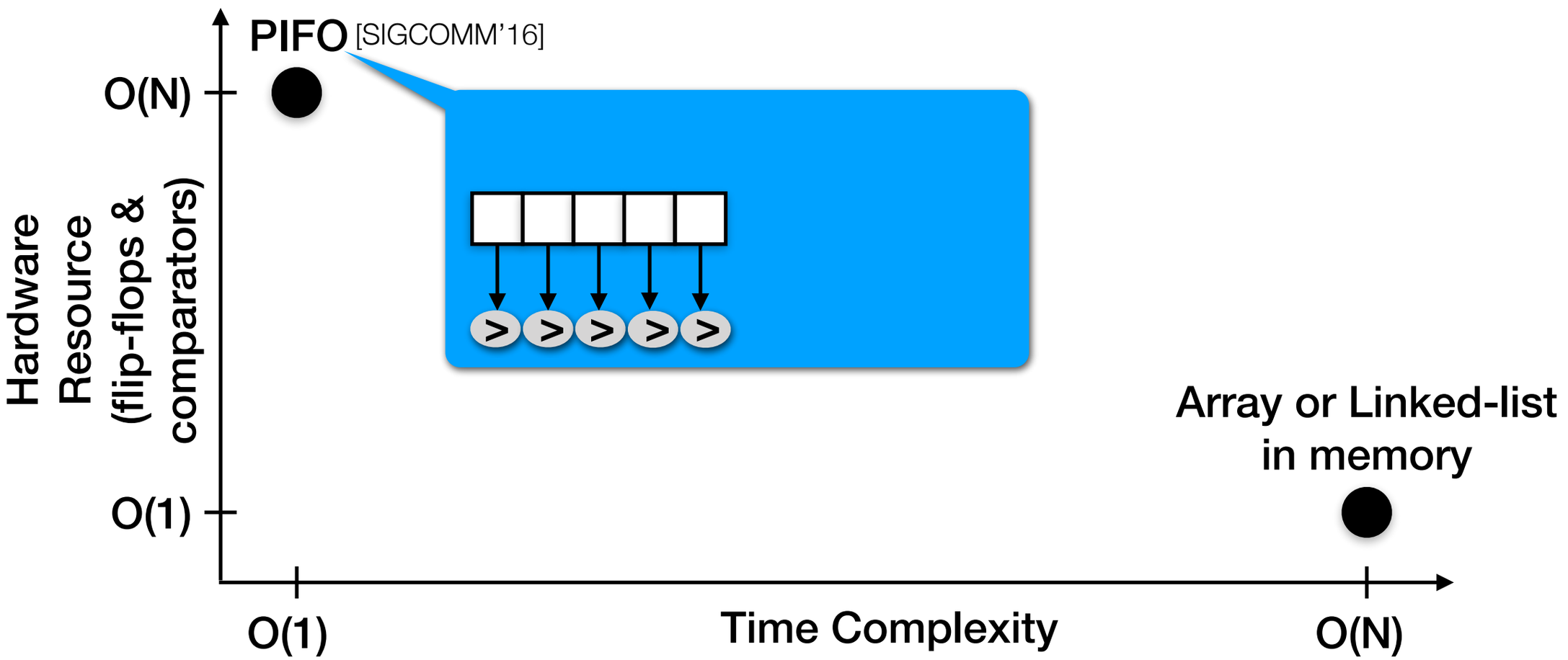

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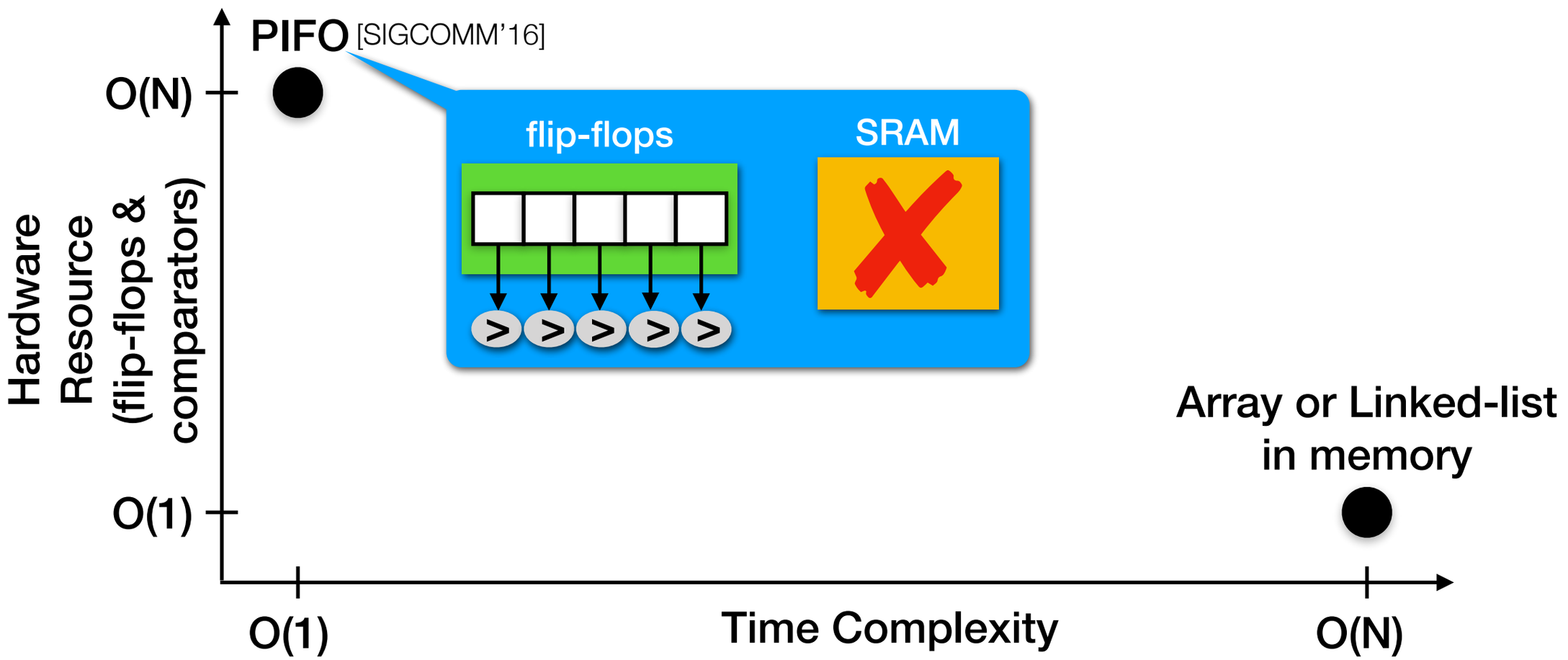

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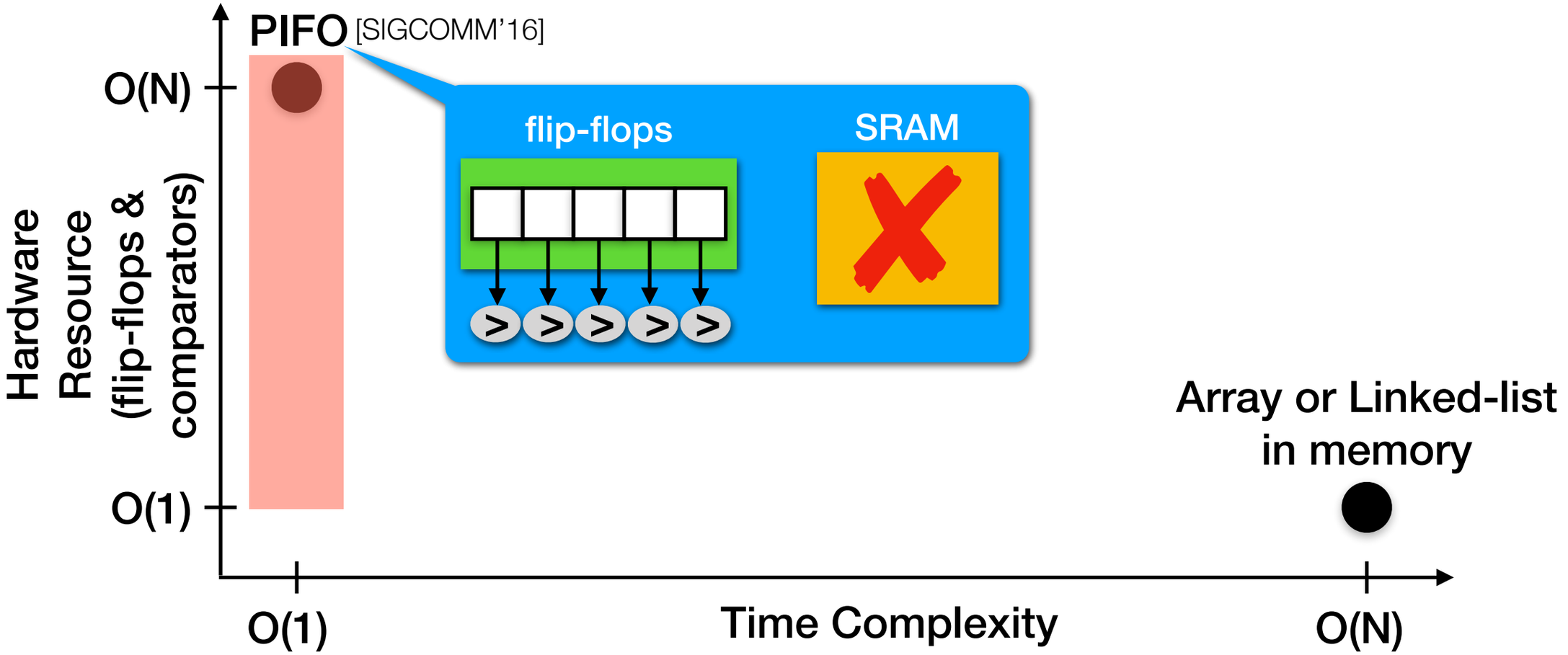

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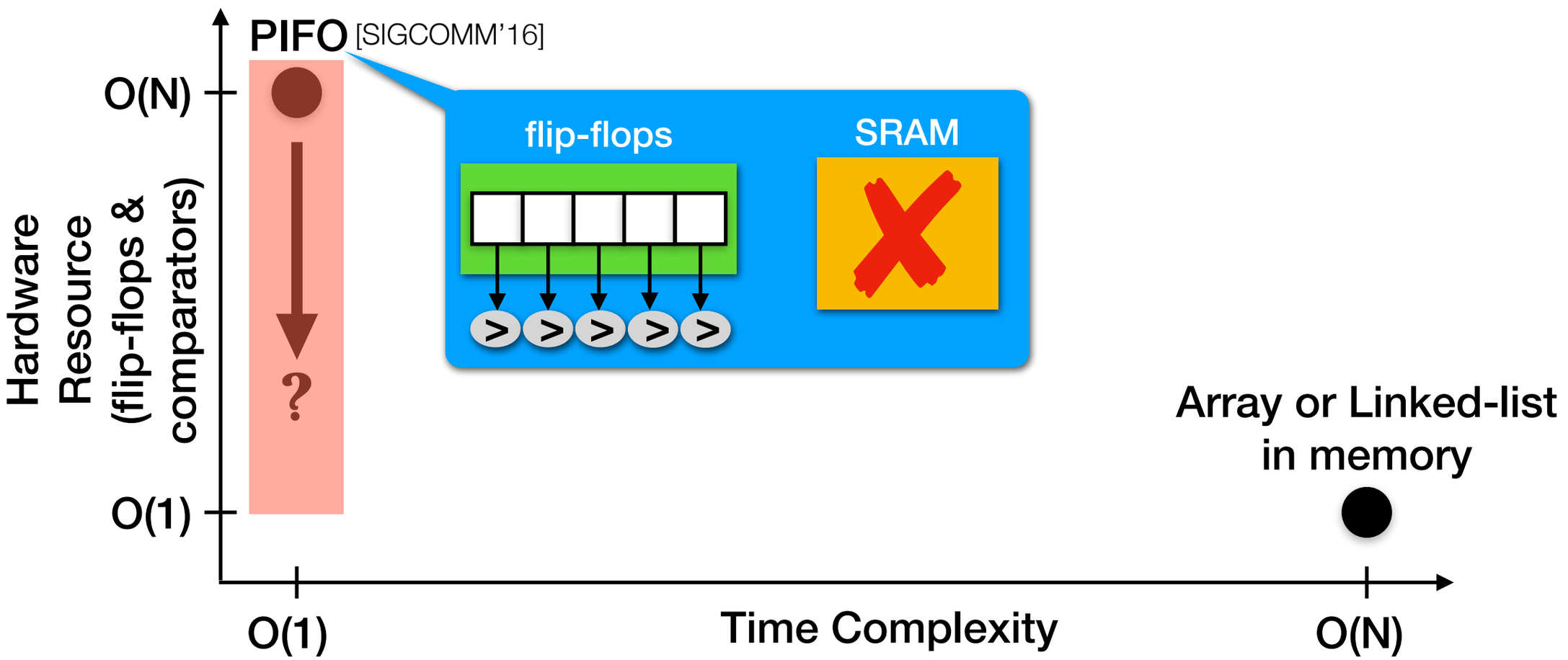

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We present a design that can maintain an (exact) ordered list in $O(1)$ time, but only needs to access and compare $O(\sqrt{N})$ elements in parallel.

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We present a design that can maintain an (exact) ordered list in $O(1)$ time, but only needs to access and compare $O(\sqrt{N})$ elements in parallel.

Key Insight

"All problems in computer science can be solved by another level of indirection"

—David Wheeler

Hardware Architecture

Flip-Flops

SRAM

Hardware Architecture

Flip-Flops

SRAM

Hardware Architecture

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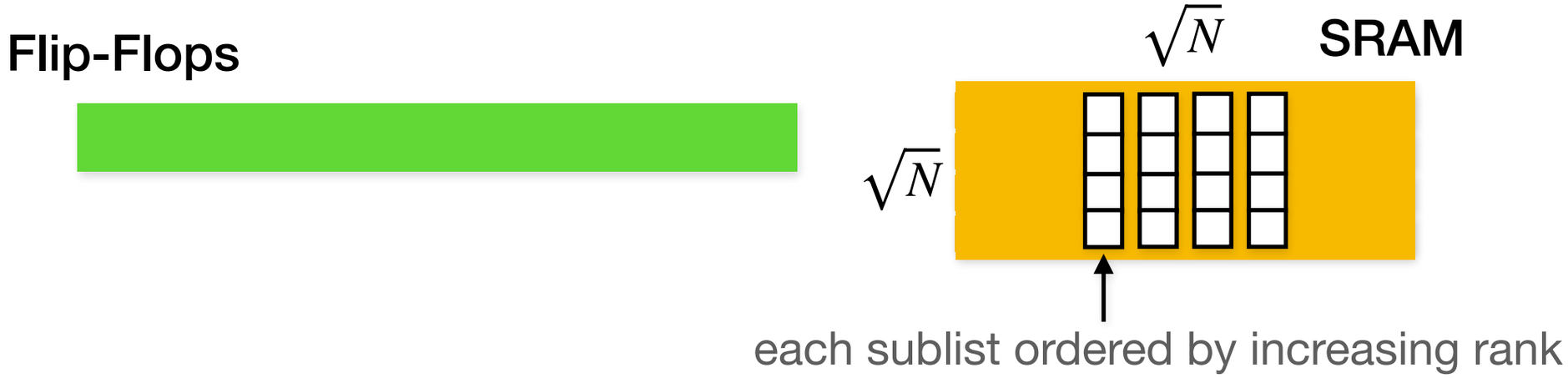
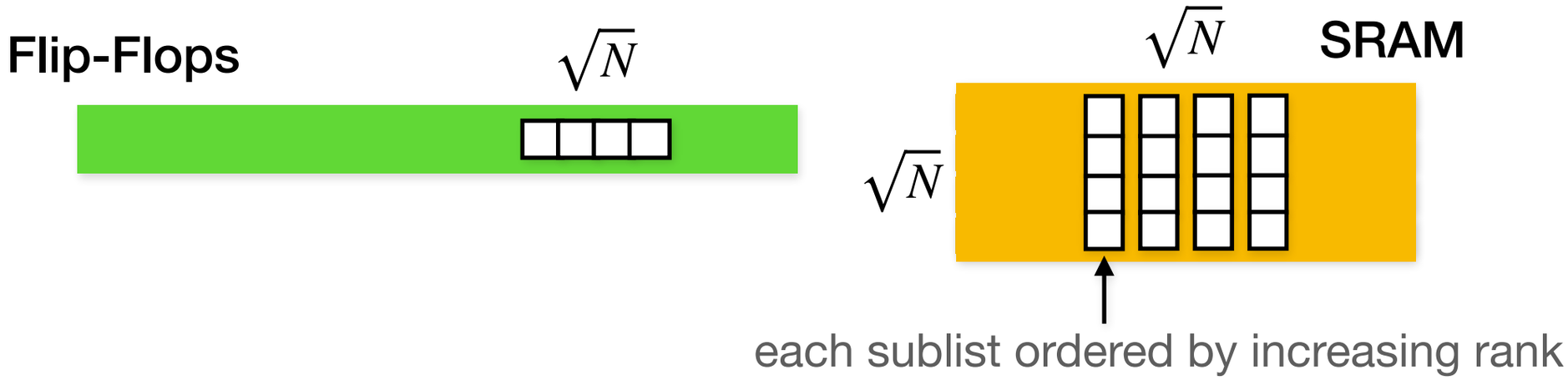


Hardware Architecture



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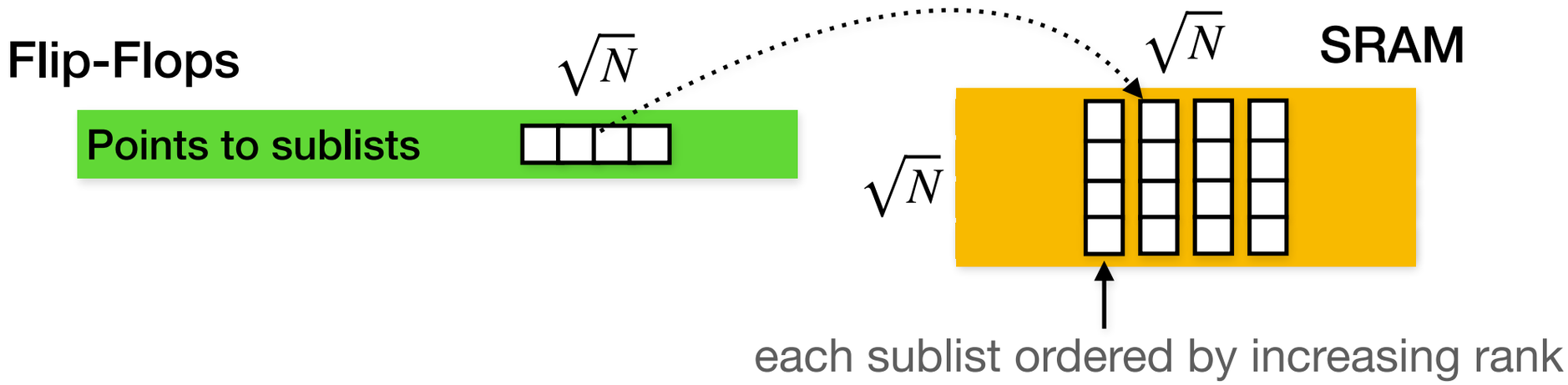

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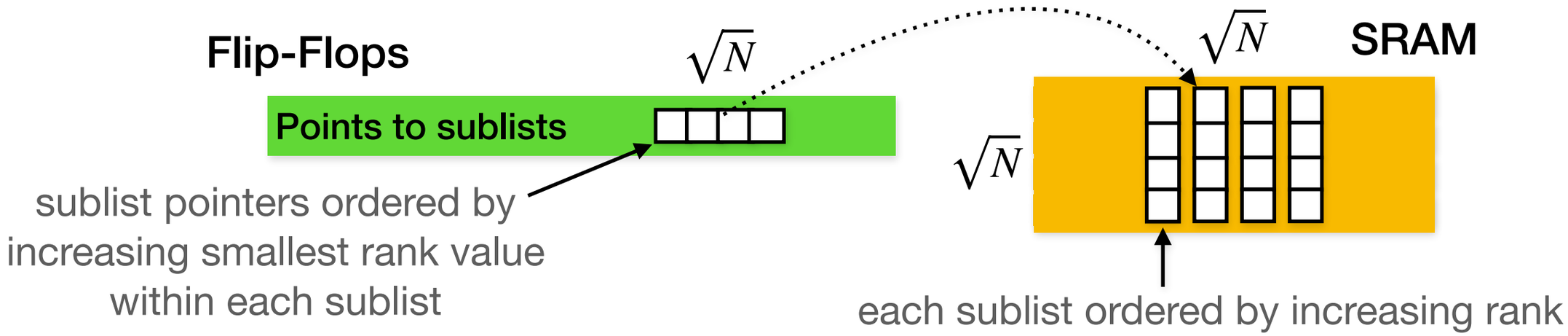
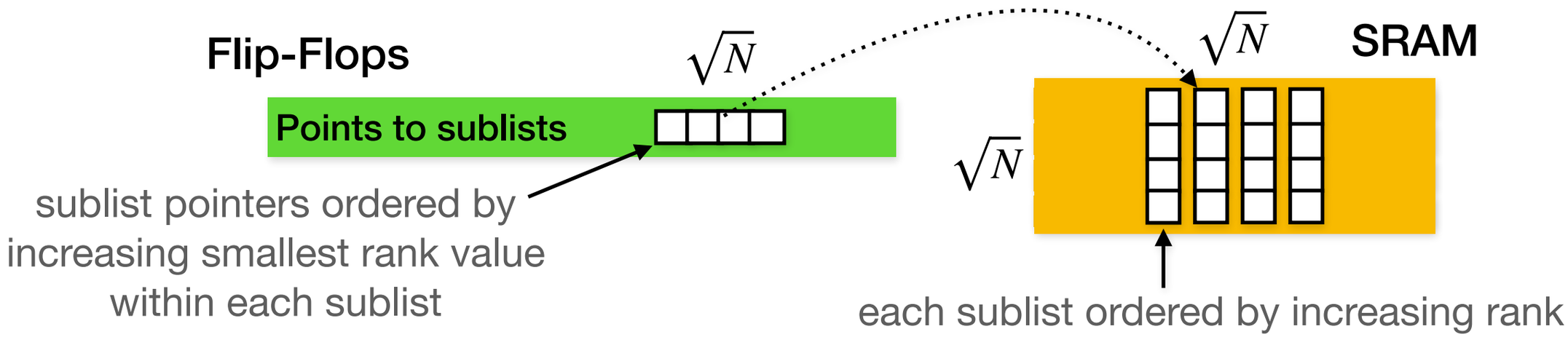


Hardware Architecture



enqueue(f), dequeue(), dequeue(f) each execute in exactly 4 clock cycles

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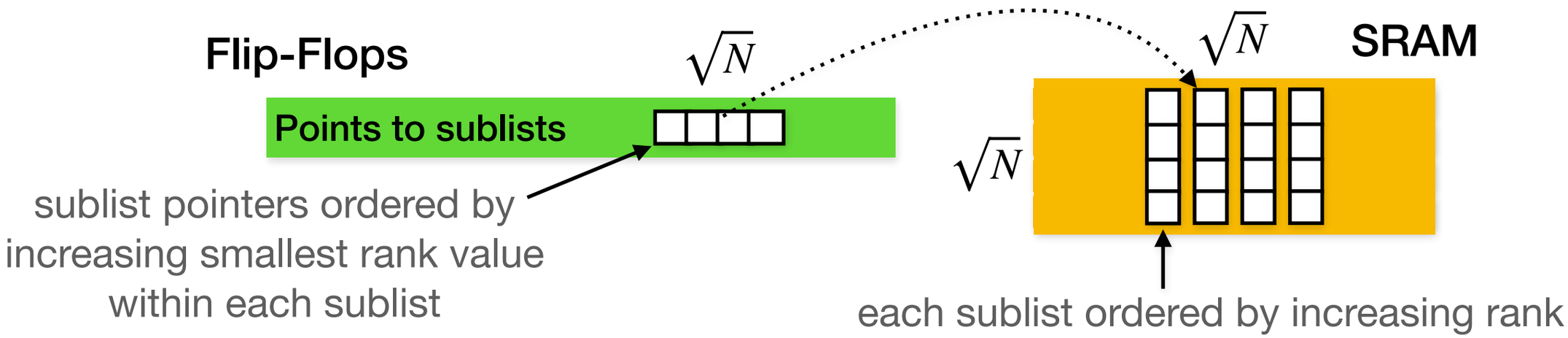

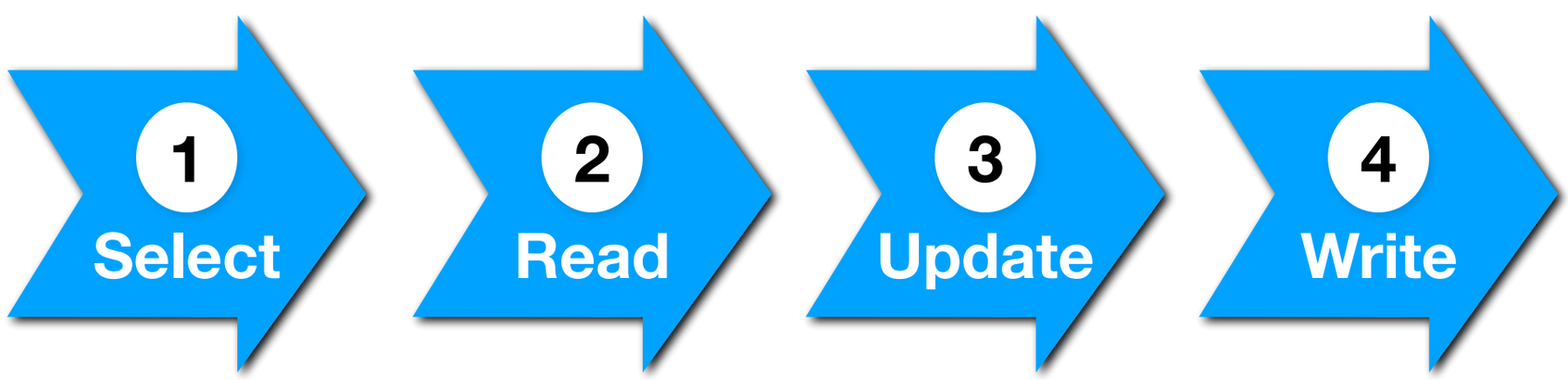

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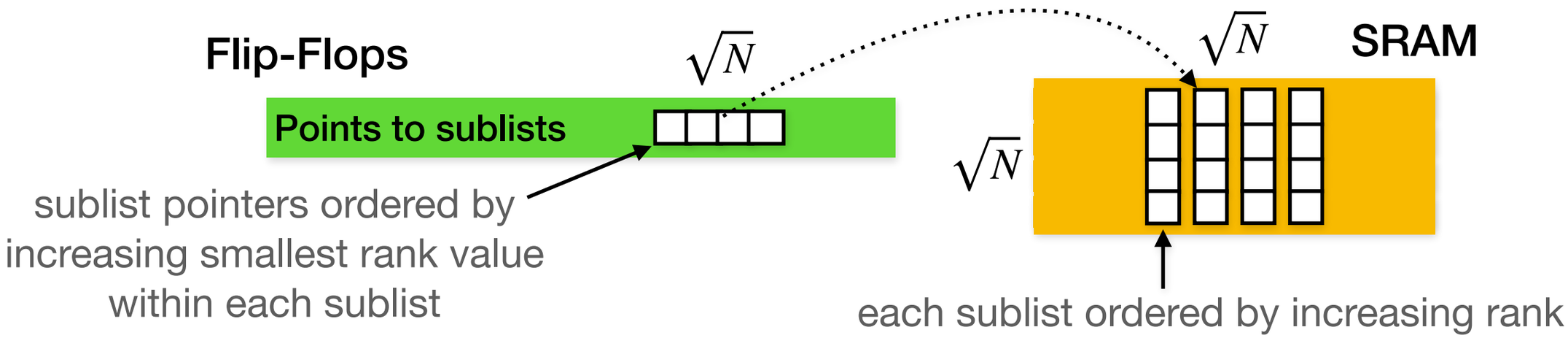

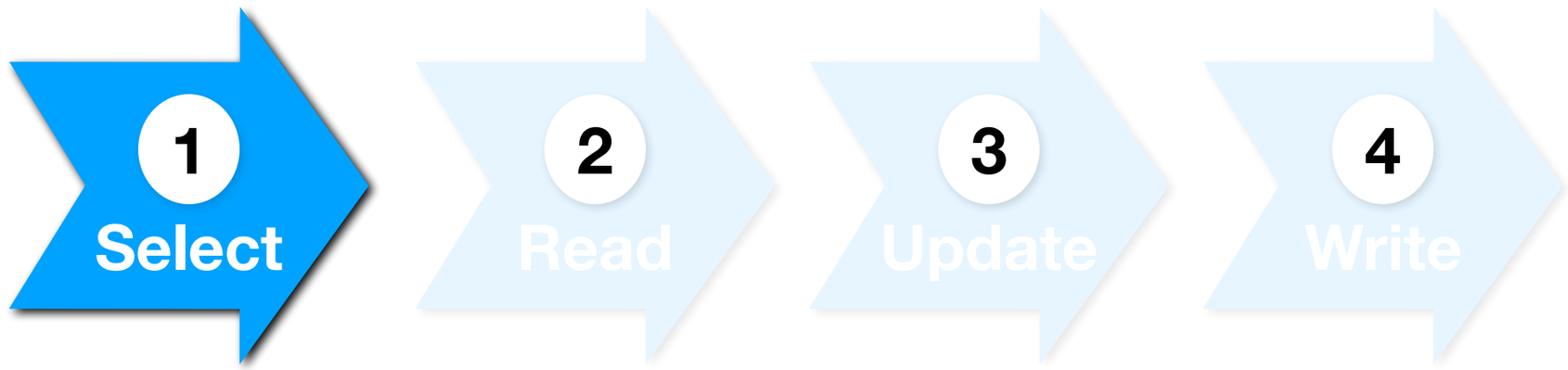

Select correct sublist S

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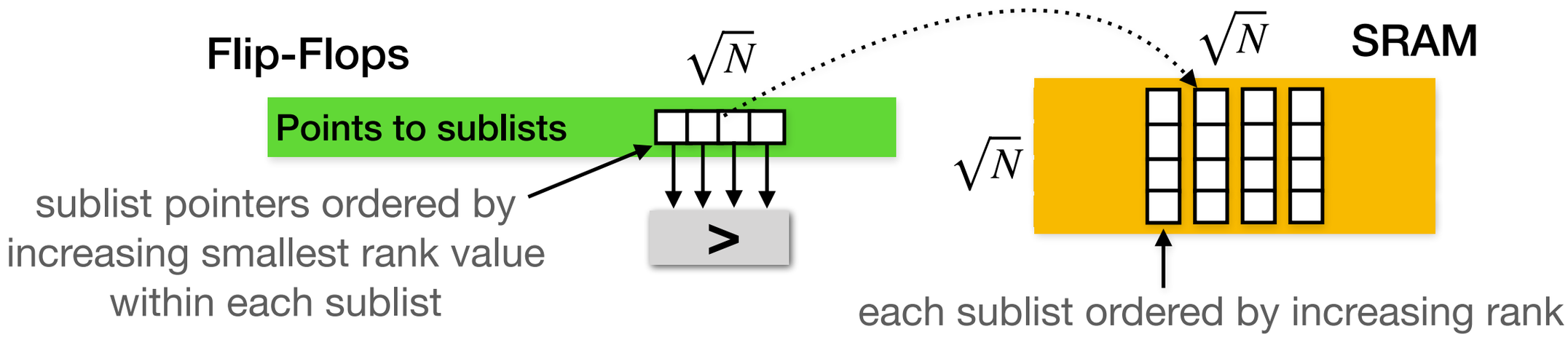
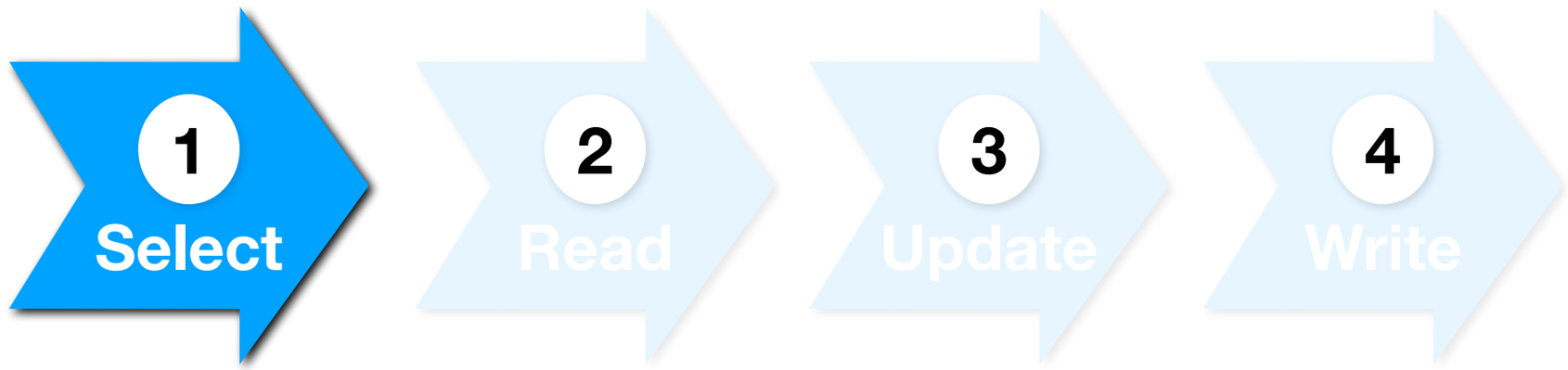
Hardware Architecture





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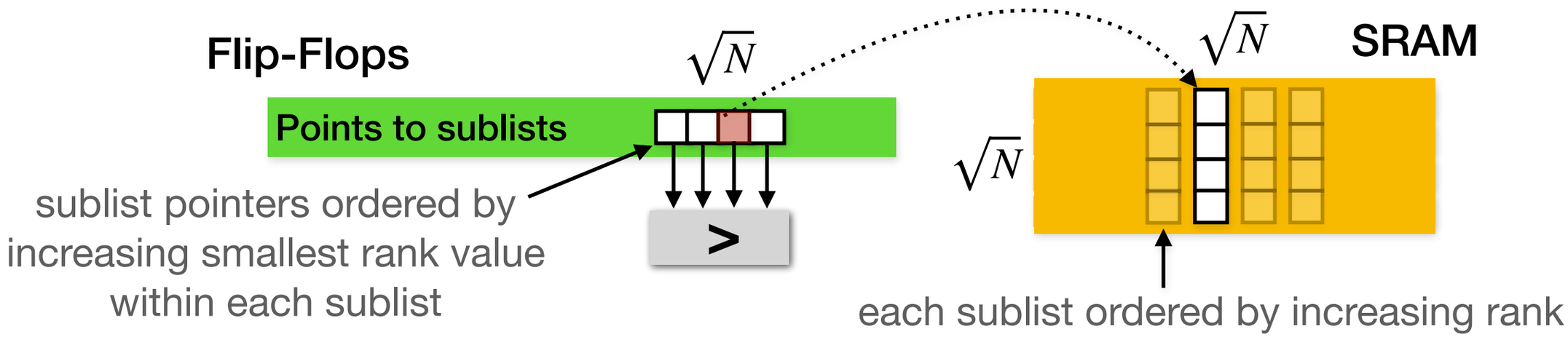

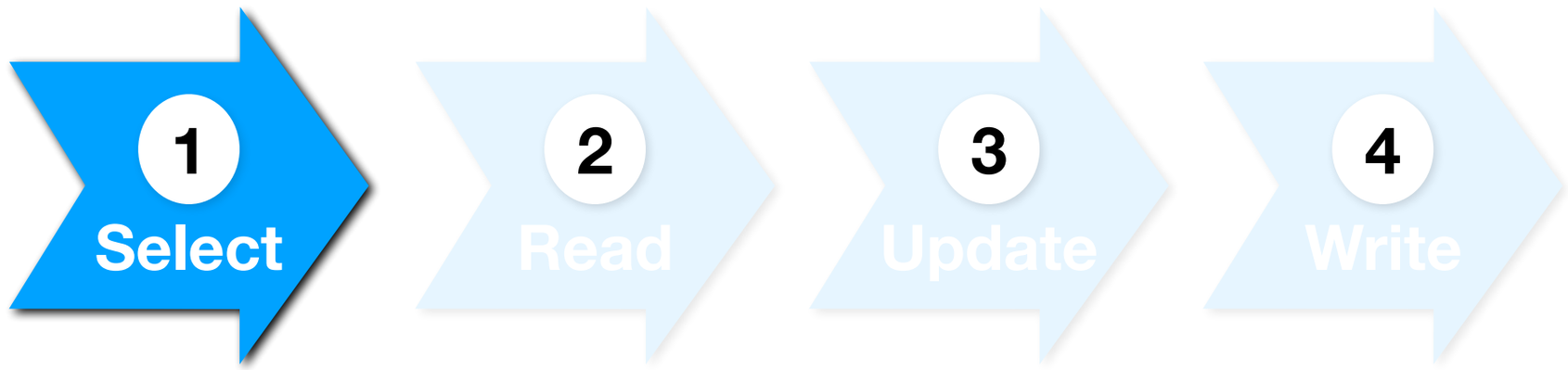

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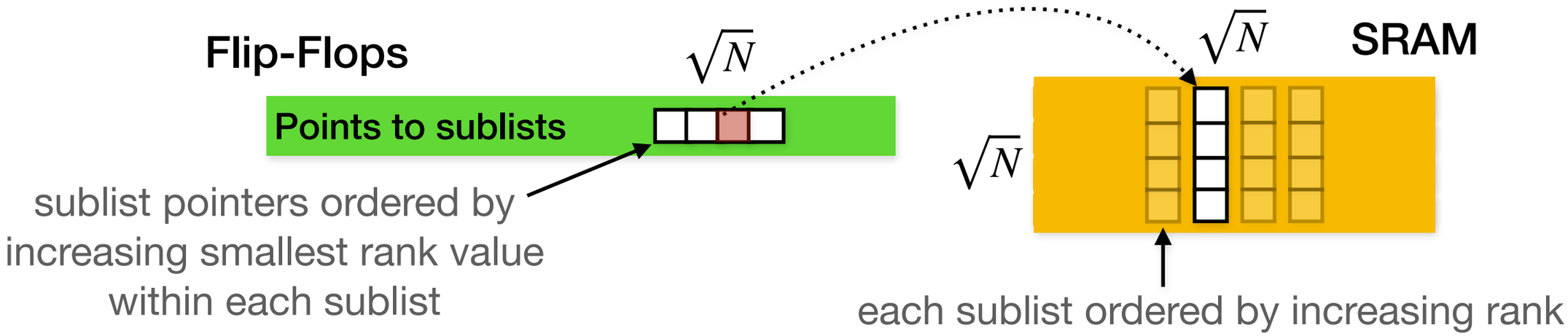

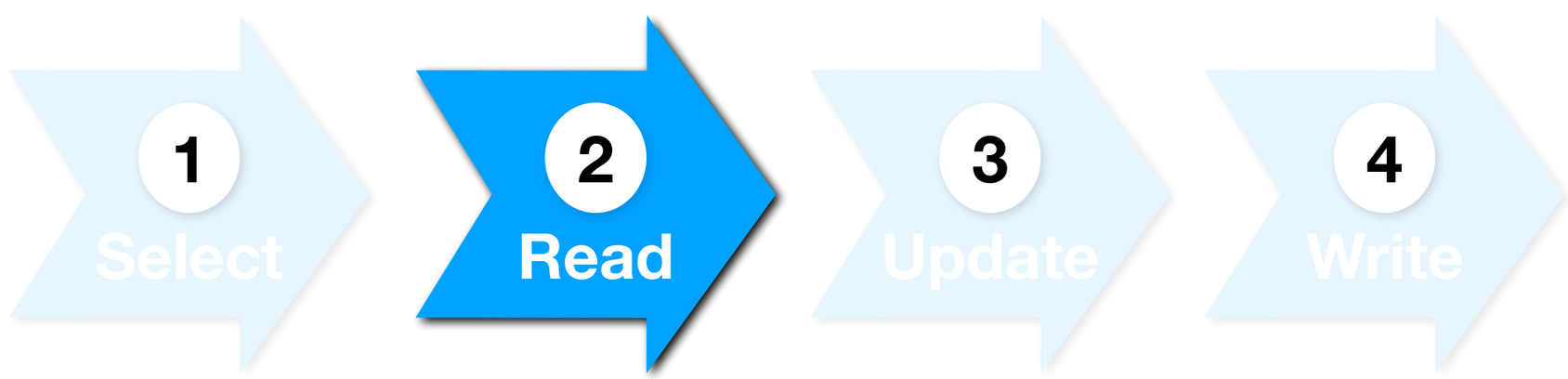

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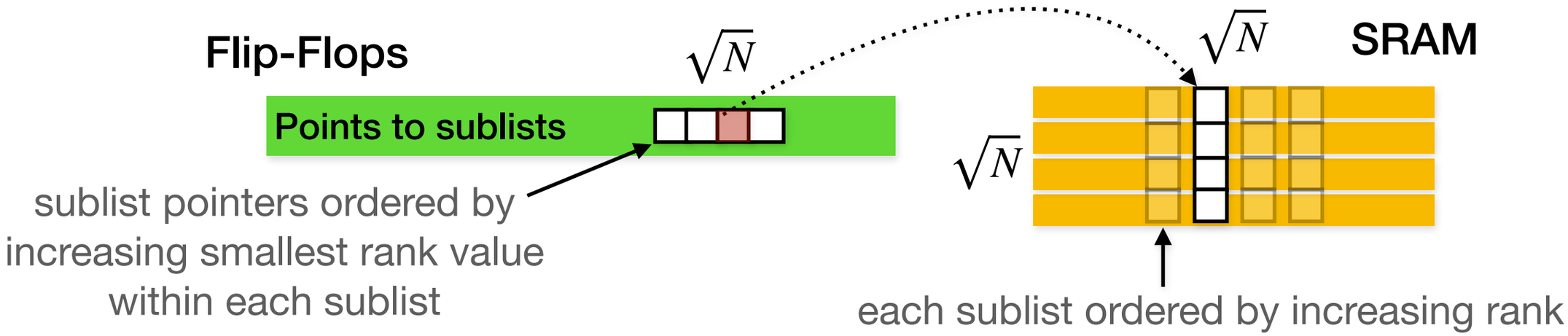

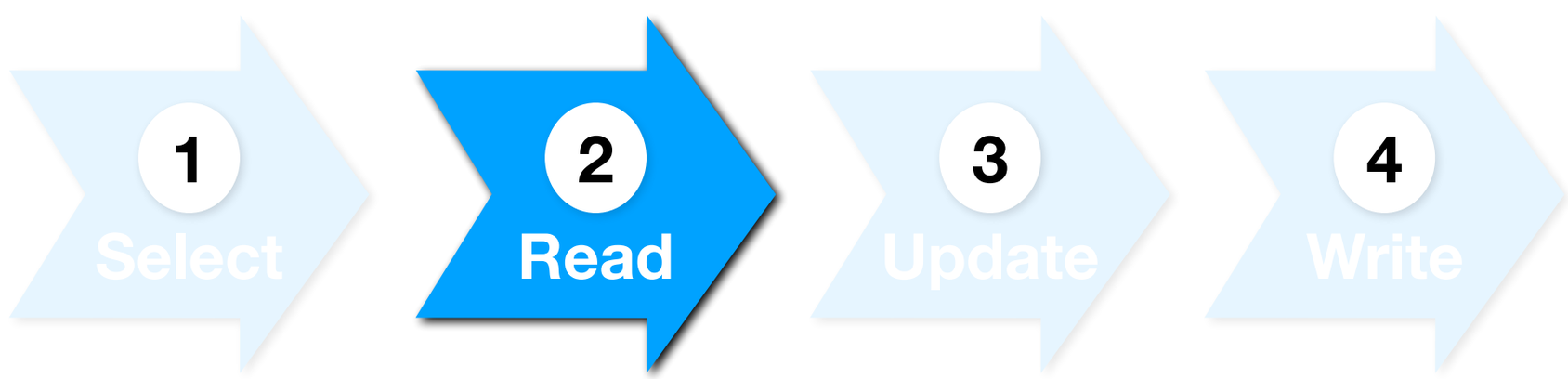

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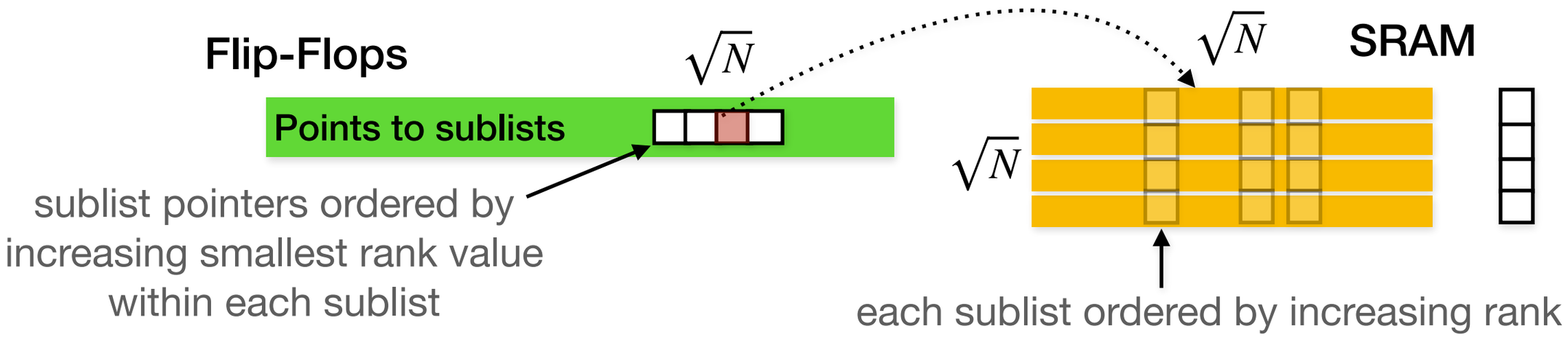

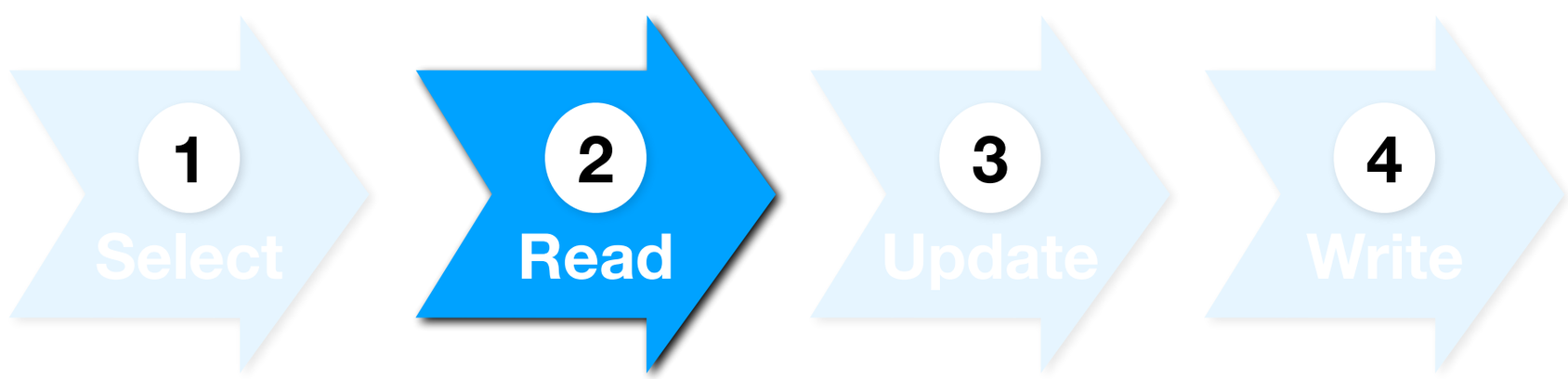

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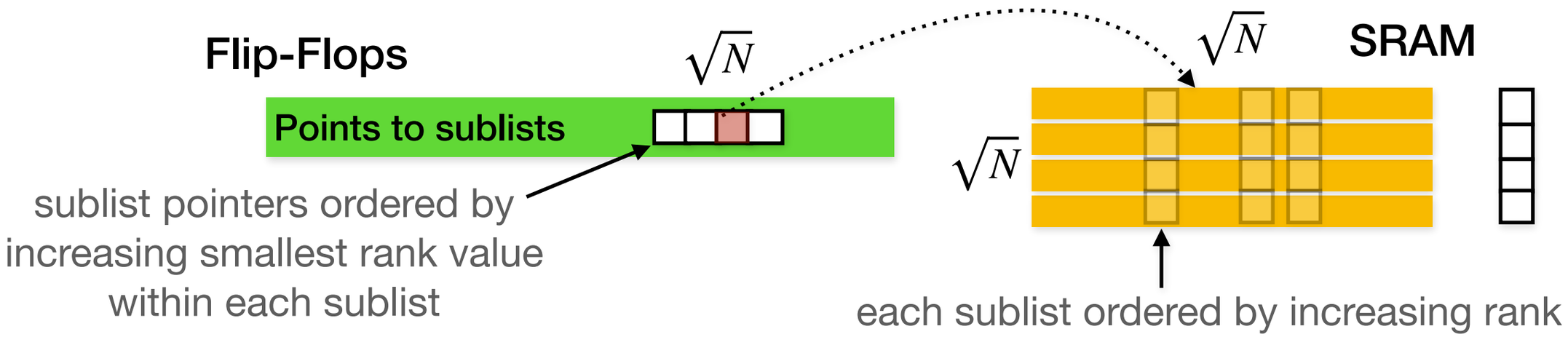

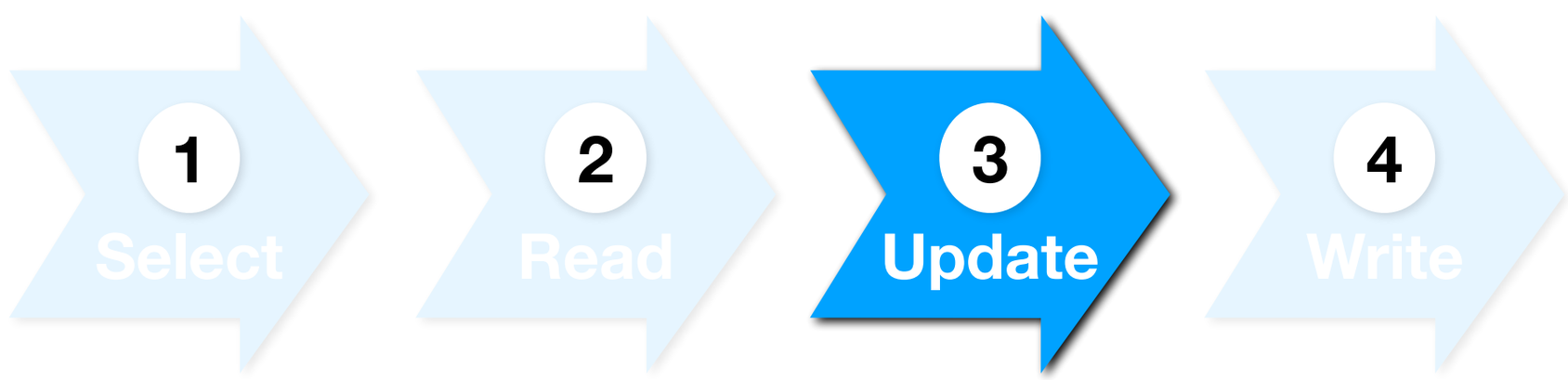

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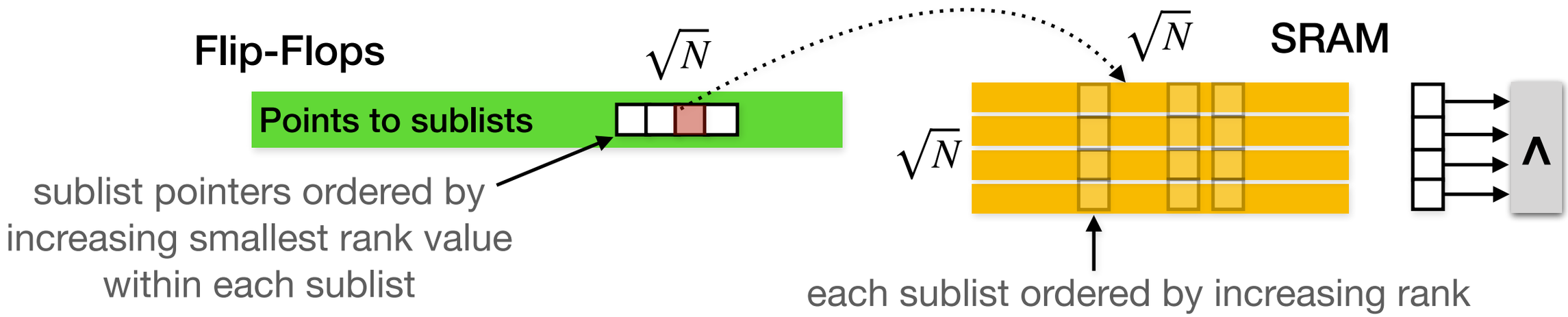

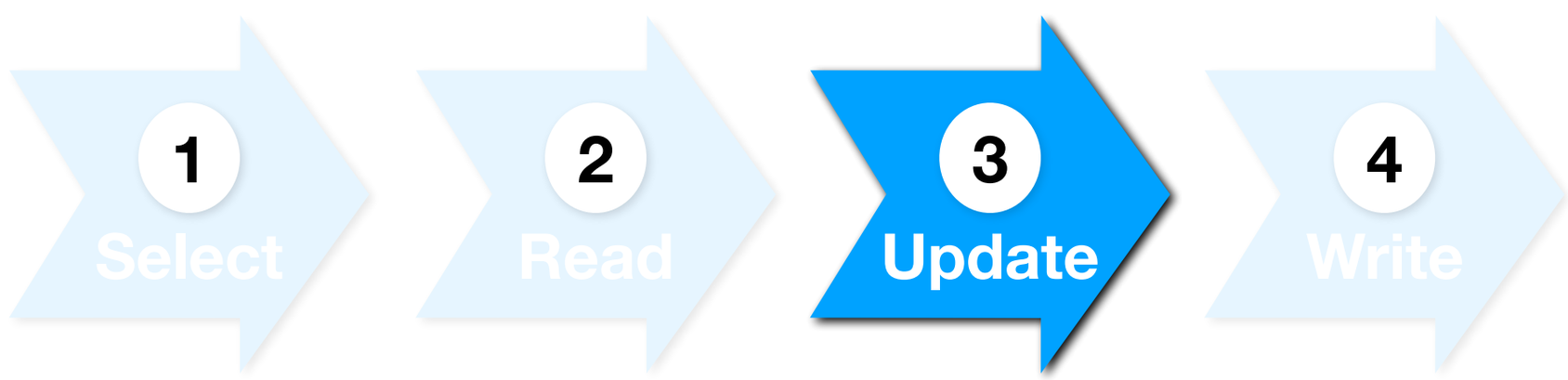

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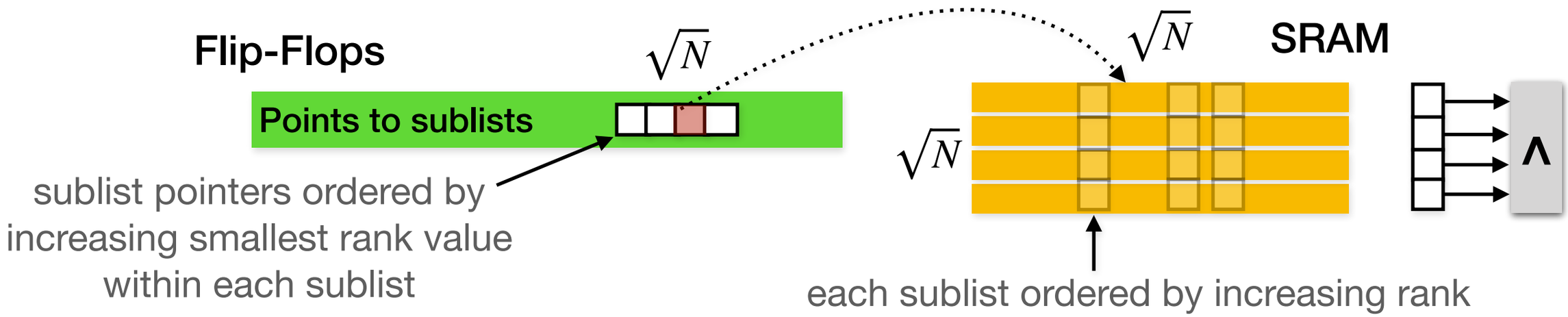

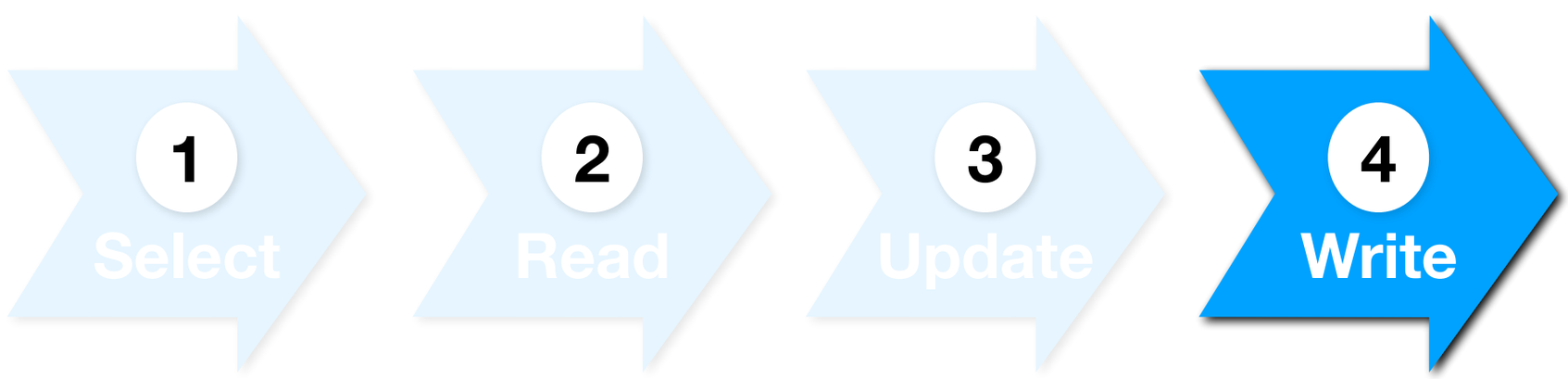

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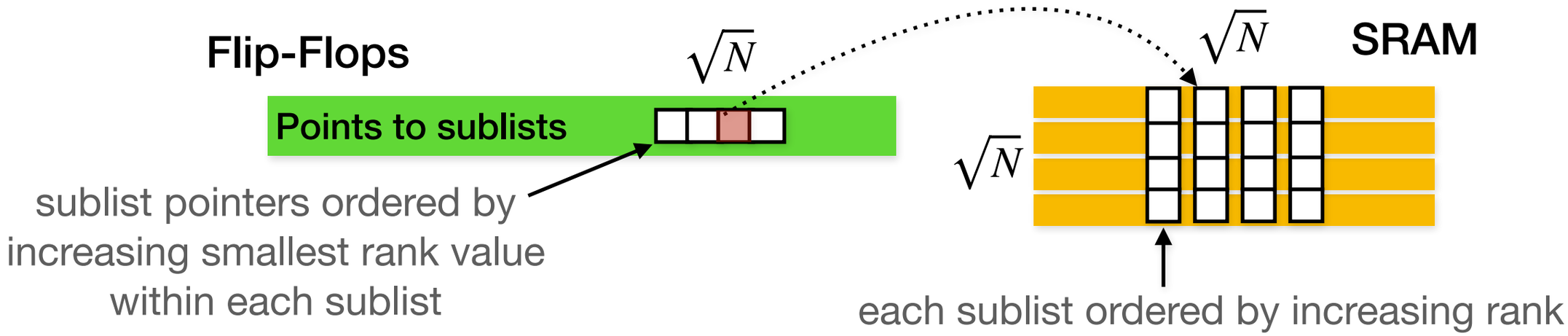

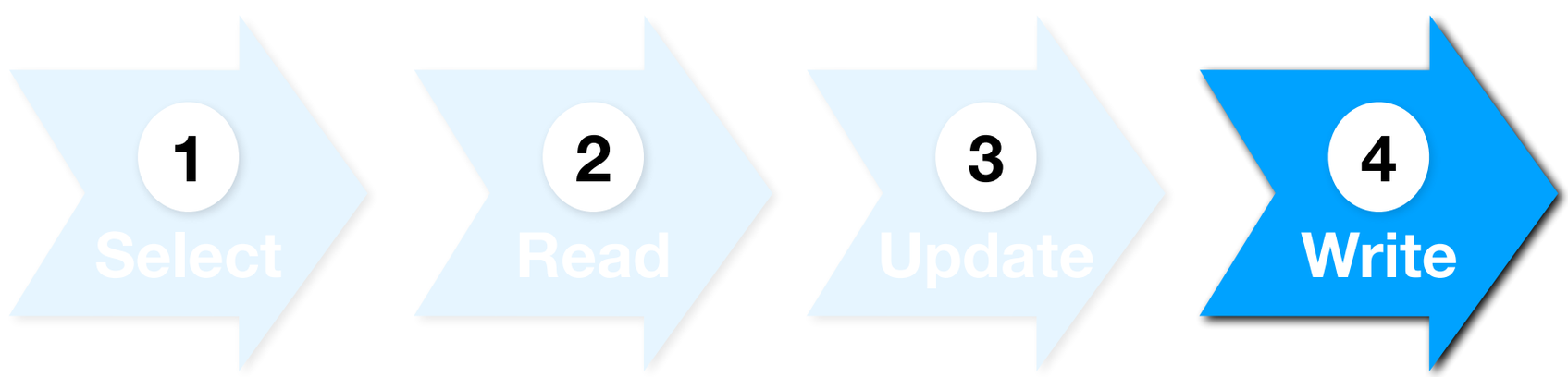

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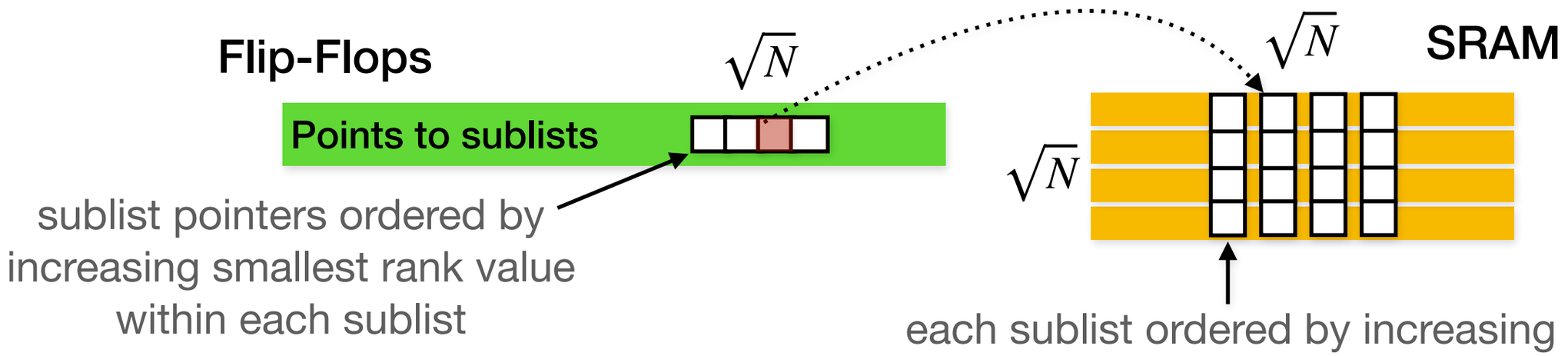

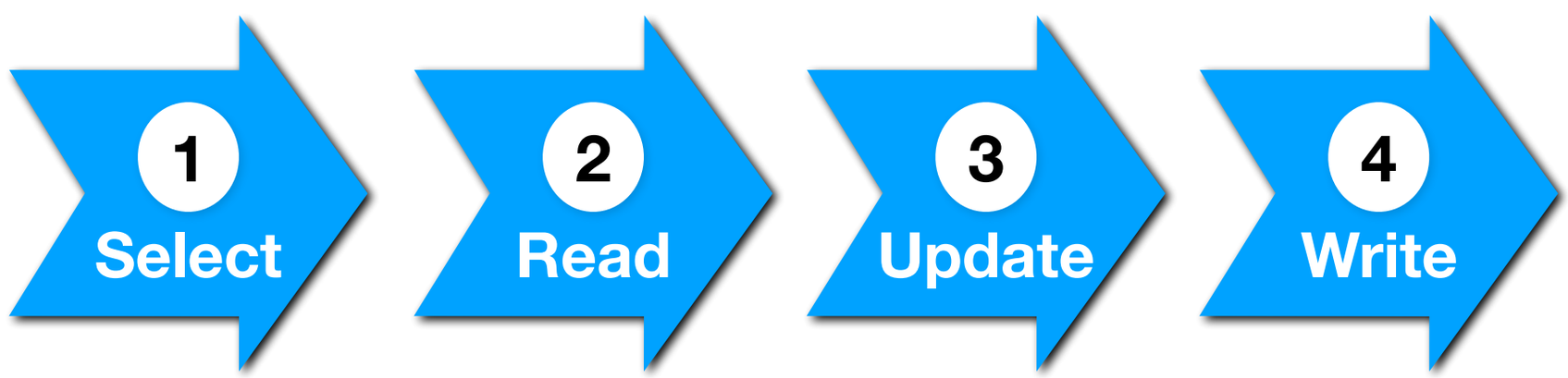

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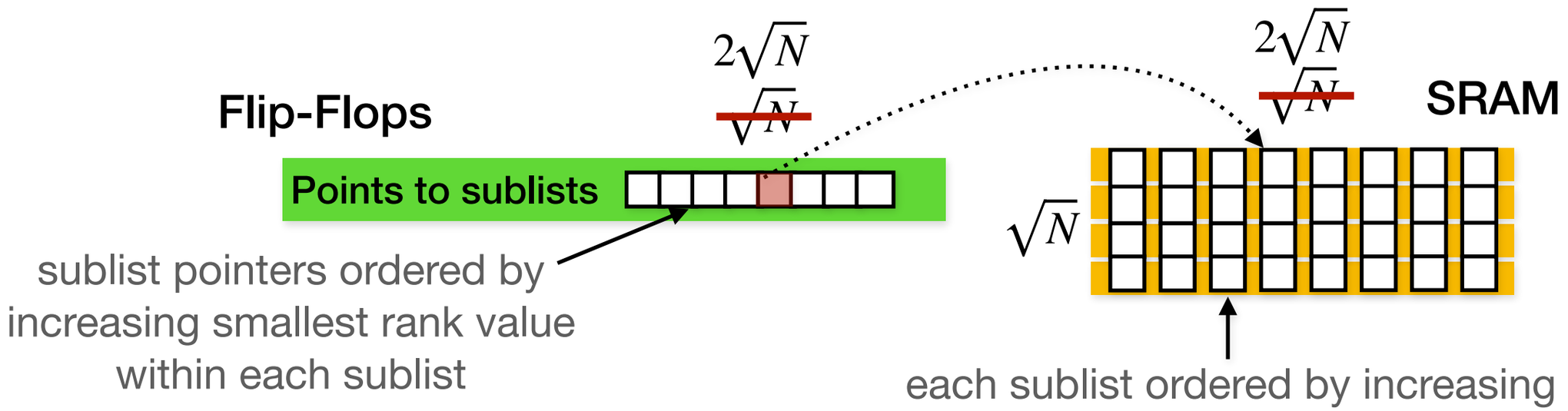
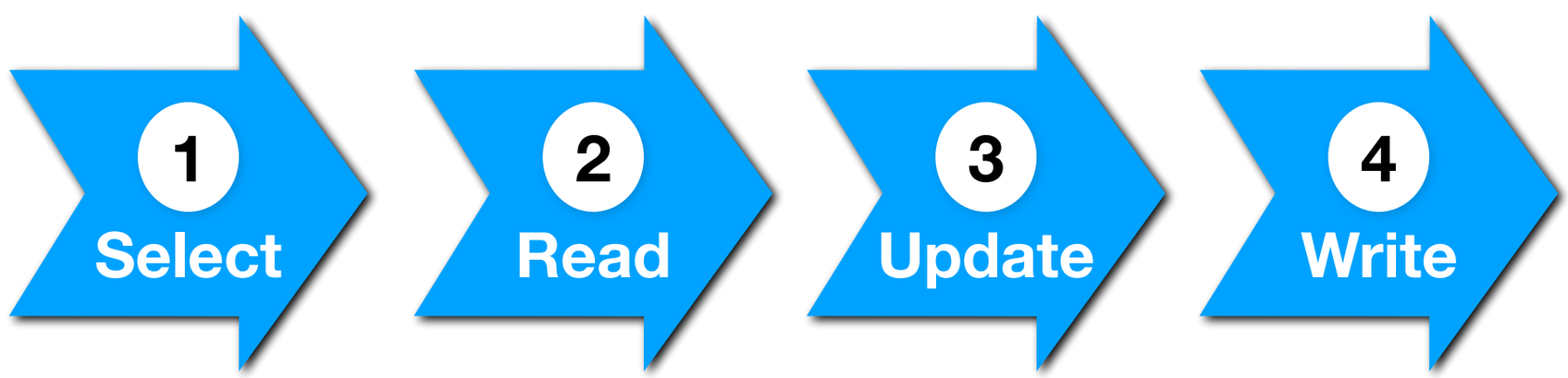




enqueue(f), dequeue(), dequeue(f) each execute in exactly 4 clock cycles

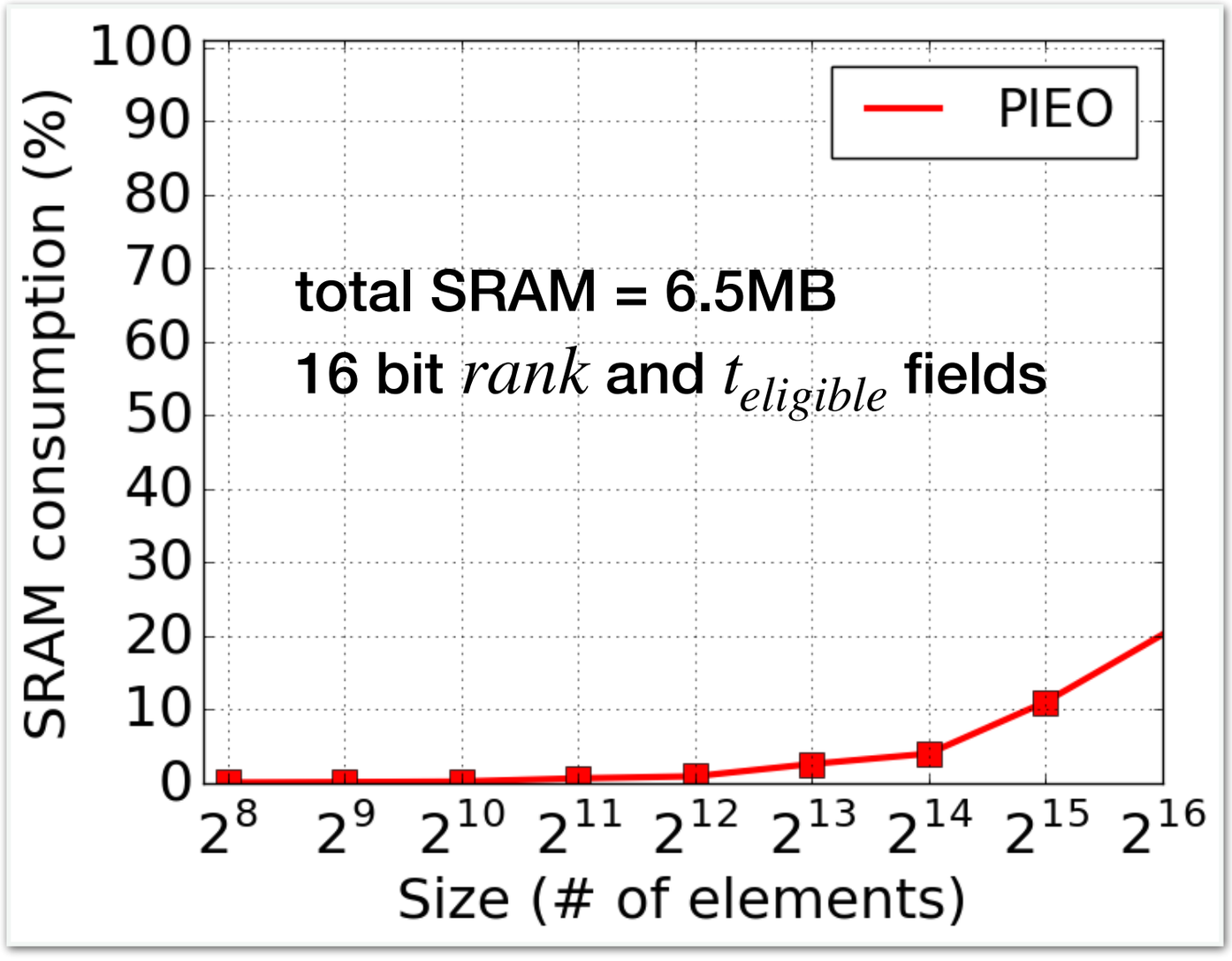
… at the cost of 2x memory overhead

Implementation

- Implemented PIEO scheduler on a **Stratix V FPGA**
  - 234K logic modules (ALMs)
  - 6.5MB SRAM
  - 40Gbps interface bandwidth
- ~1300 LOCs in System Verilog

FPGA code for the implementation of PIEO scheduler is available at:
https://github.com/vishal1303/PIEO-Scheduler

Memory Consumption



Speed

PIEO on FPGA : 80 MHz (for 32K flows)

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~200 Gbps scheduling rate for 1500B (MTU) packets

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Speed

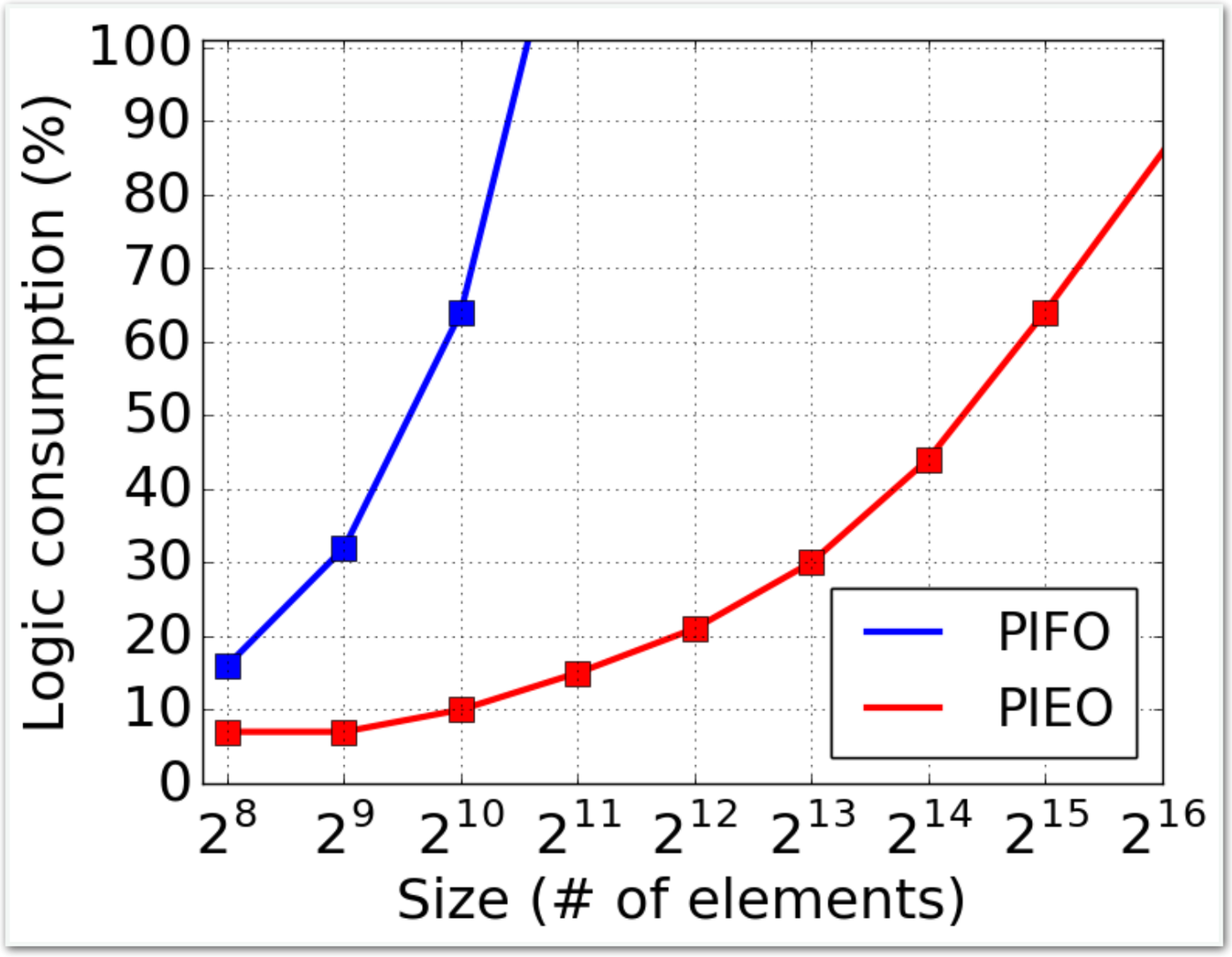
PIEO on FPGA : 80 MHz (for 32K flows) ⟶ 50ns per primitive operation

~200 Gbps scheduling rate for 1500B (MTU) packets

PIEO on ASIC : >1 GHz (expected) ⟶ <4ns per primitive operation

>3 Tbps scheduling rate for 1500B (MTU) packets

Scalability



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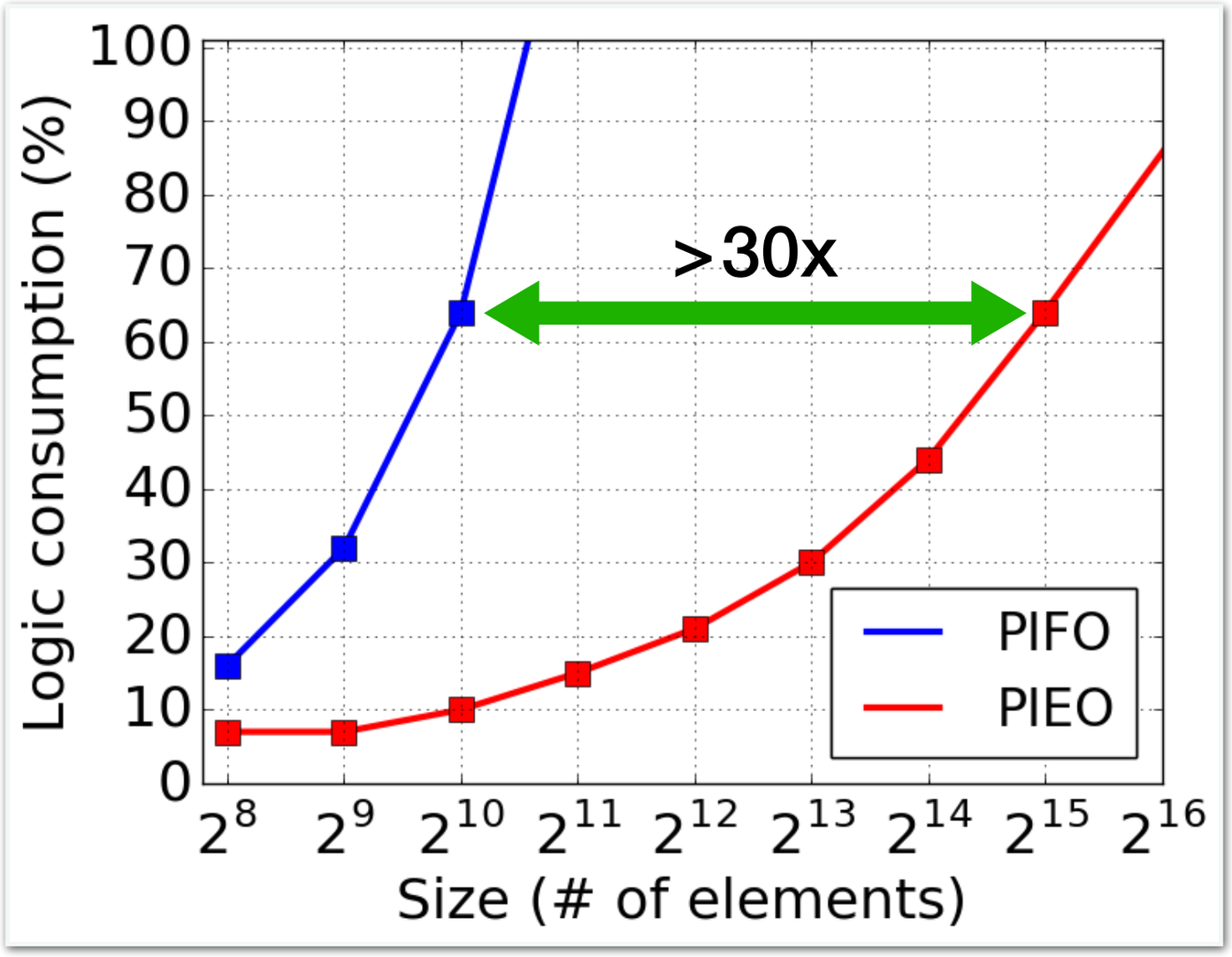
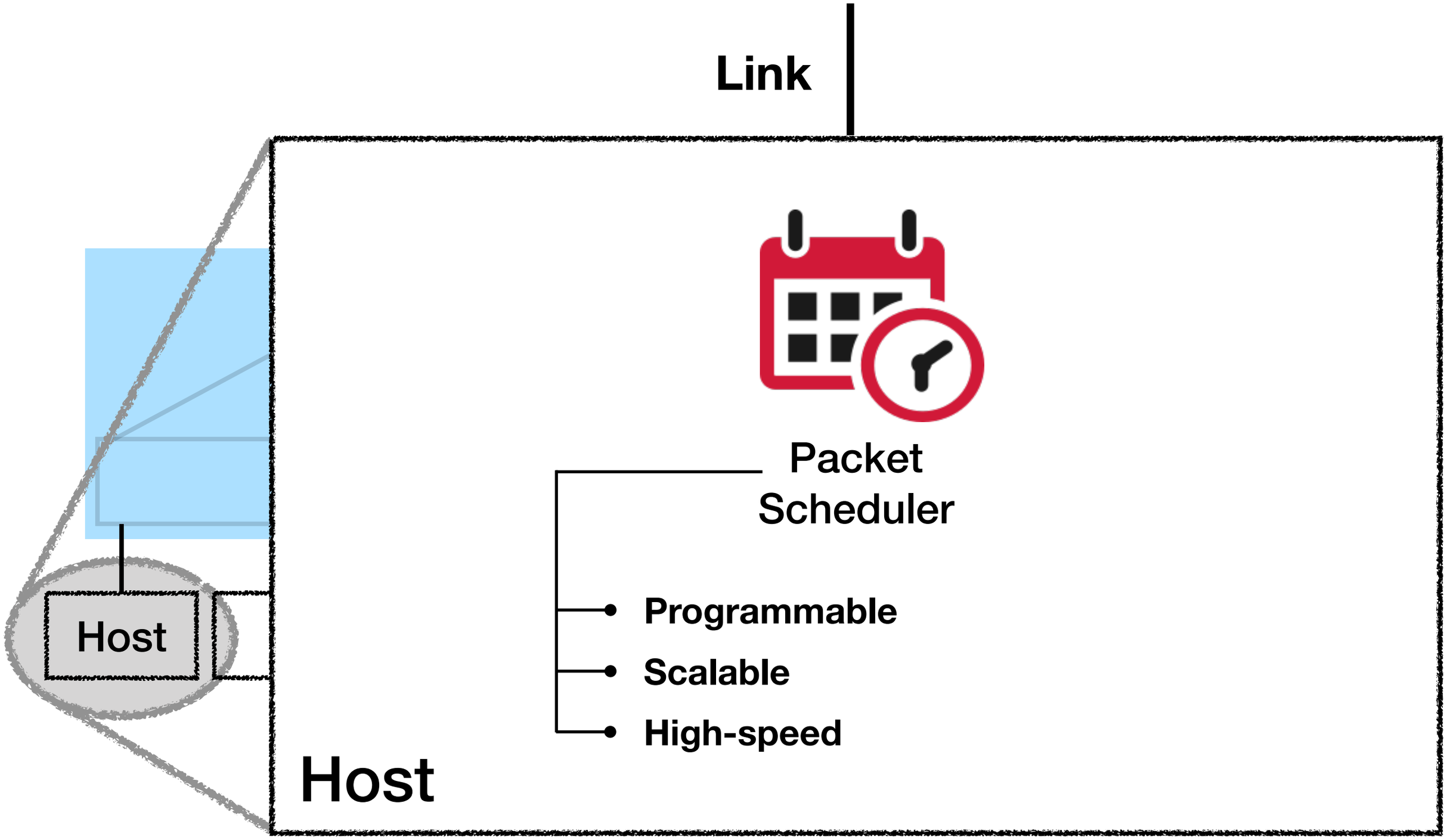


Part I : Summary



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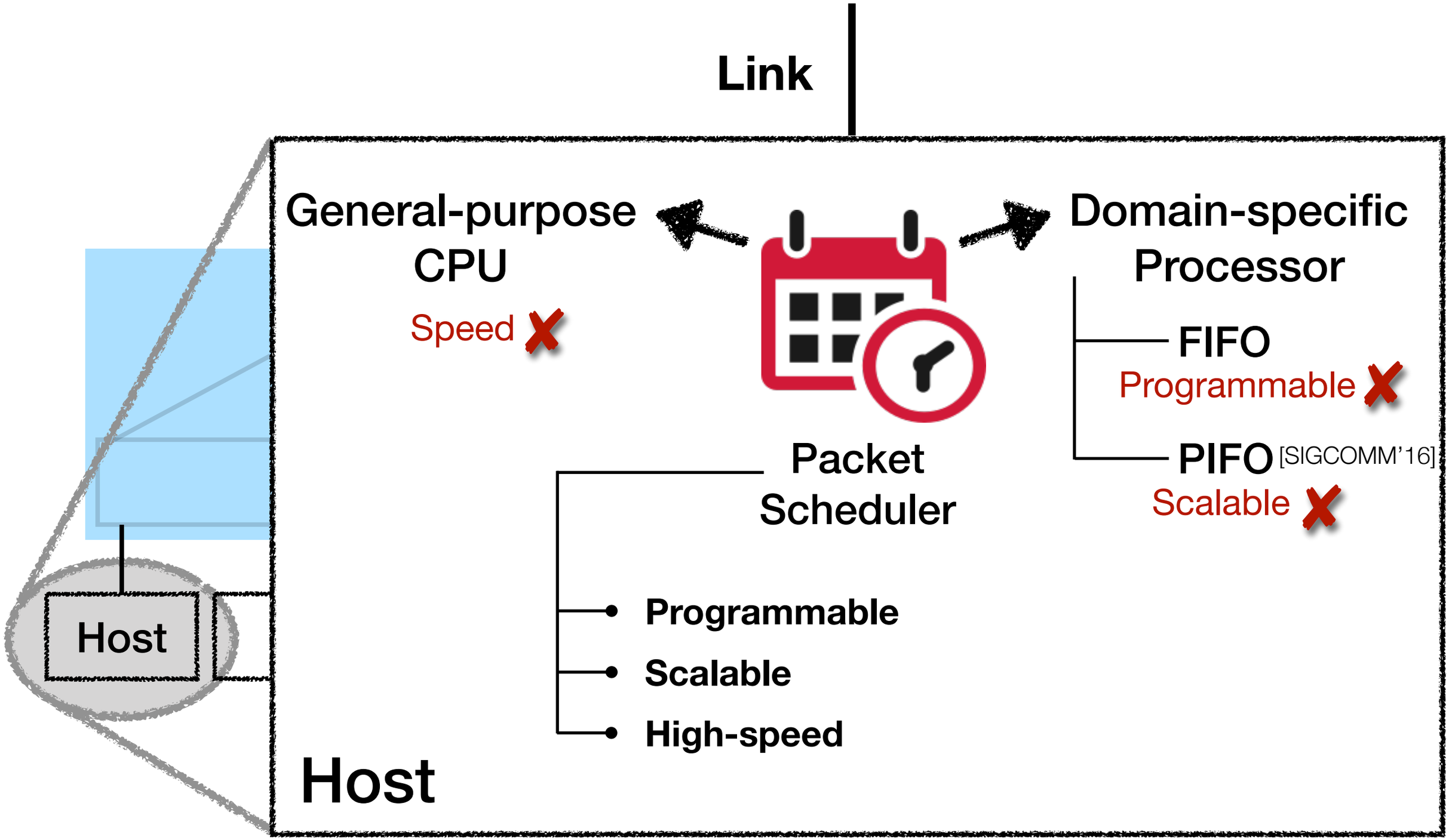

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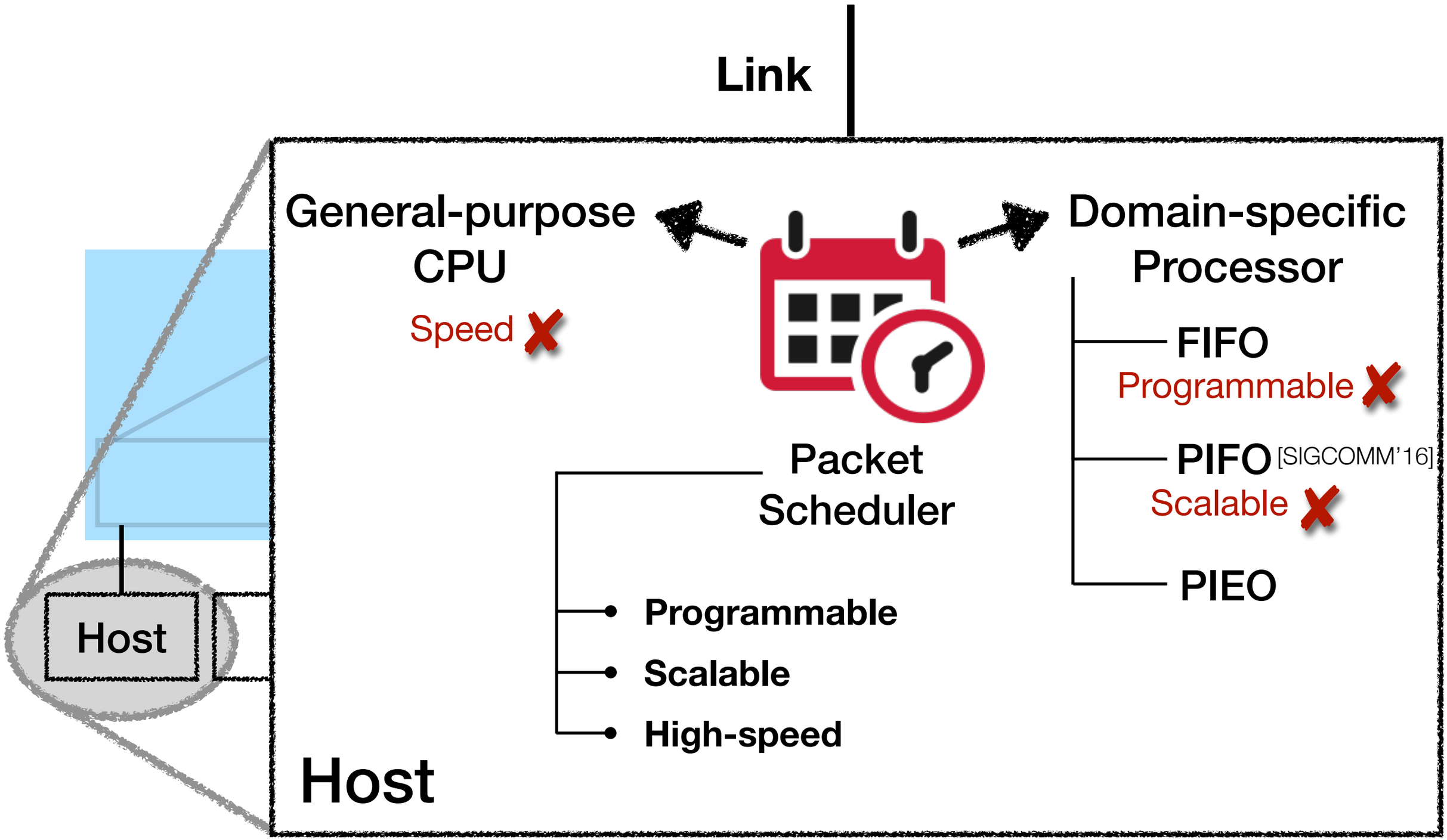

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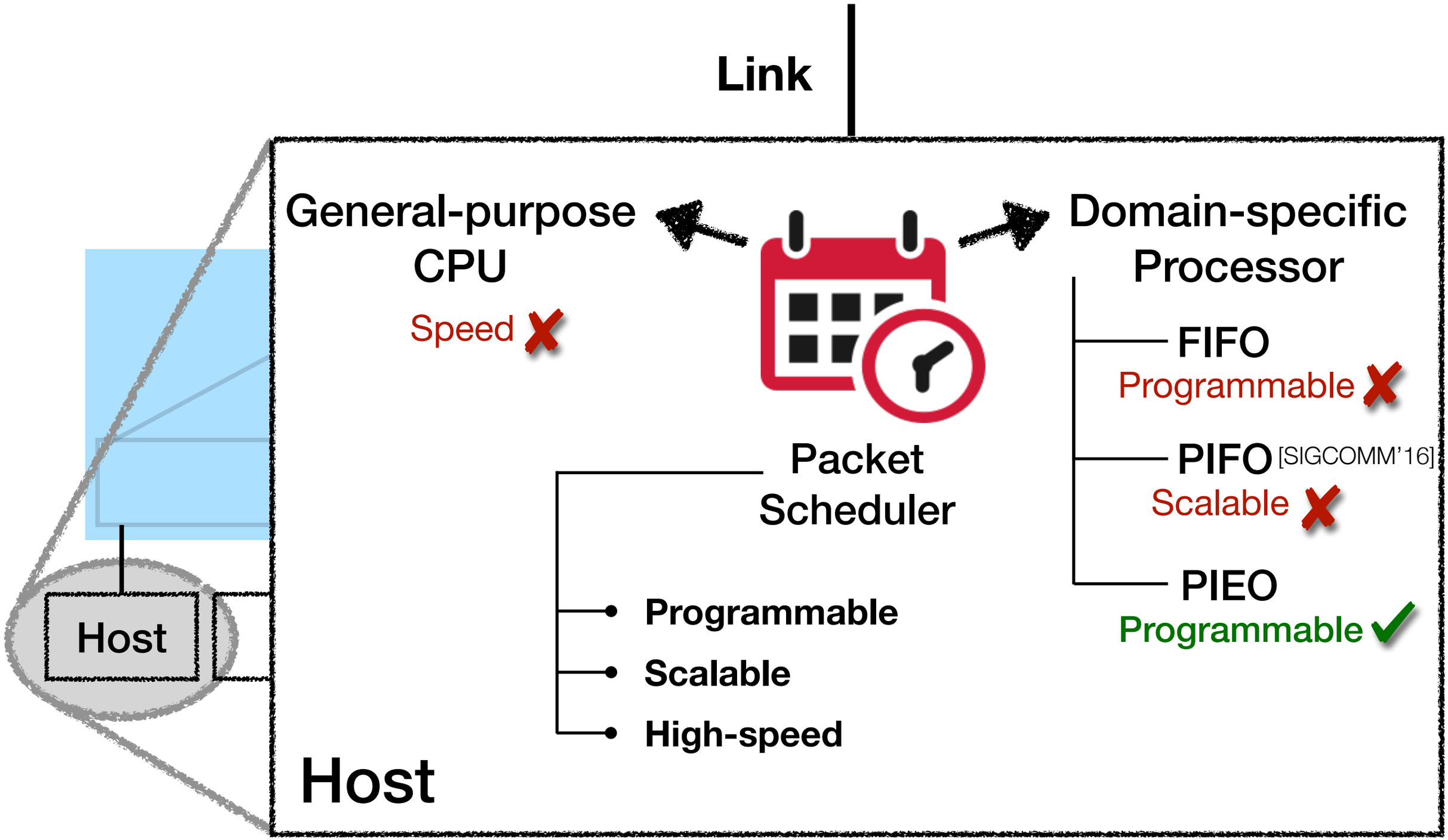

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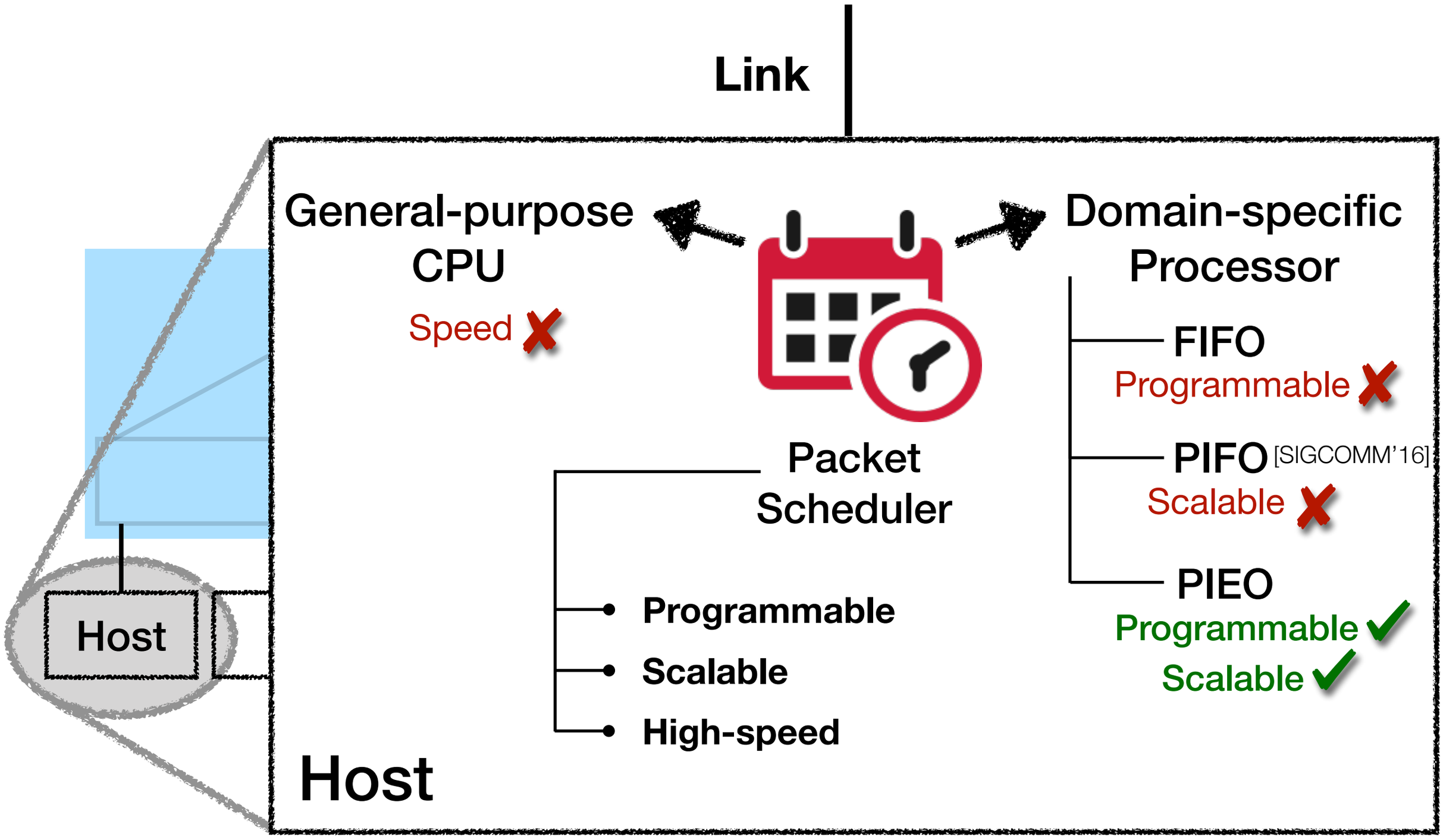

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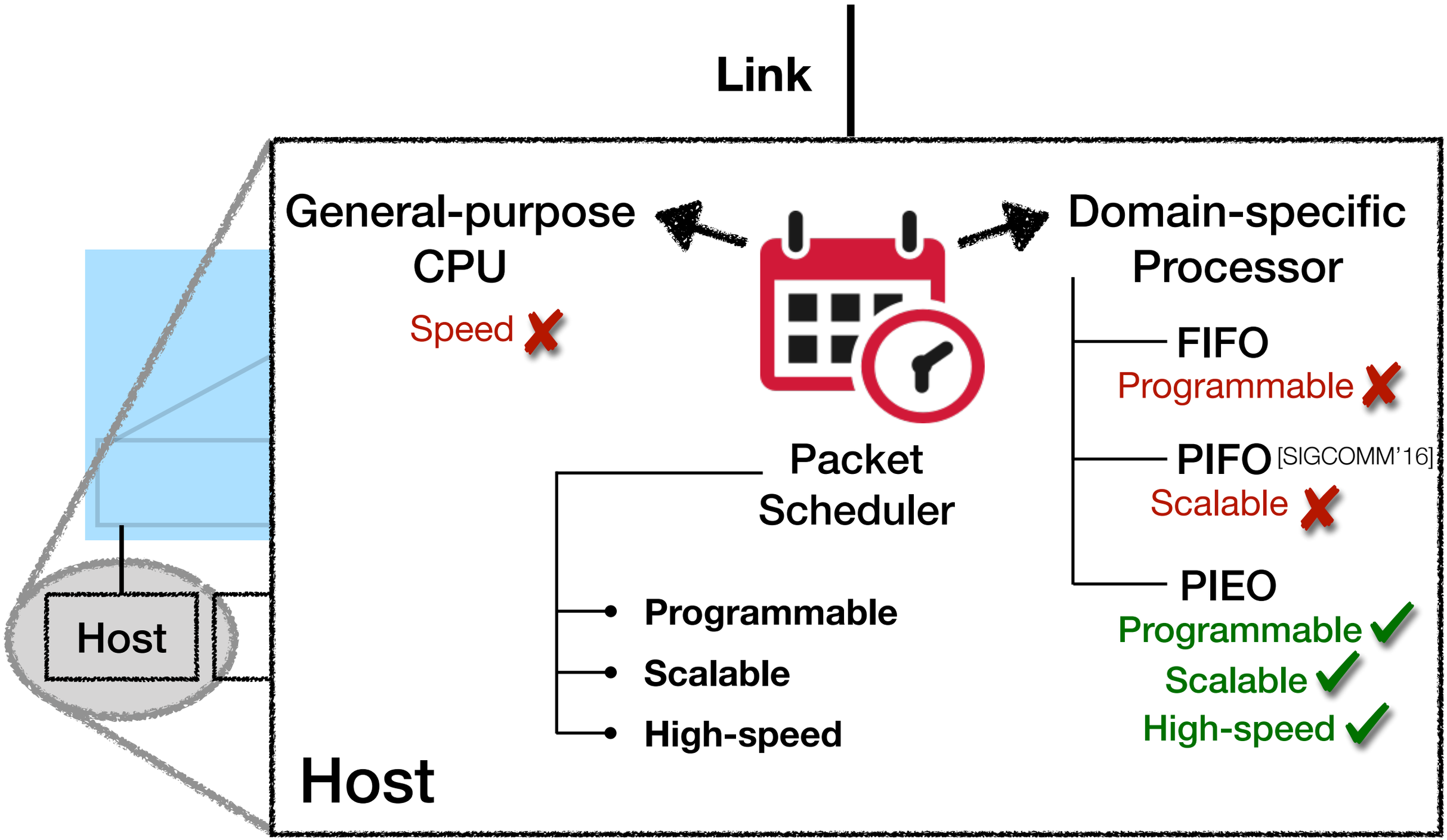
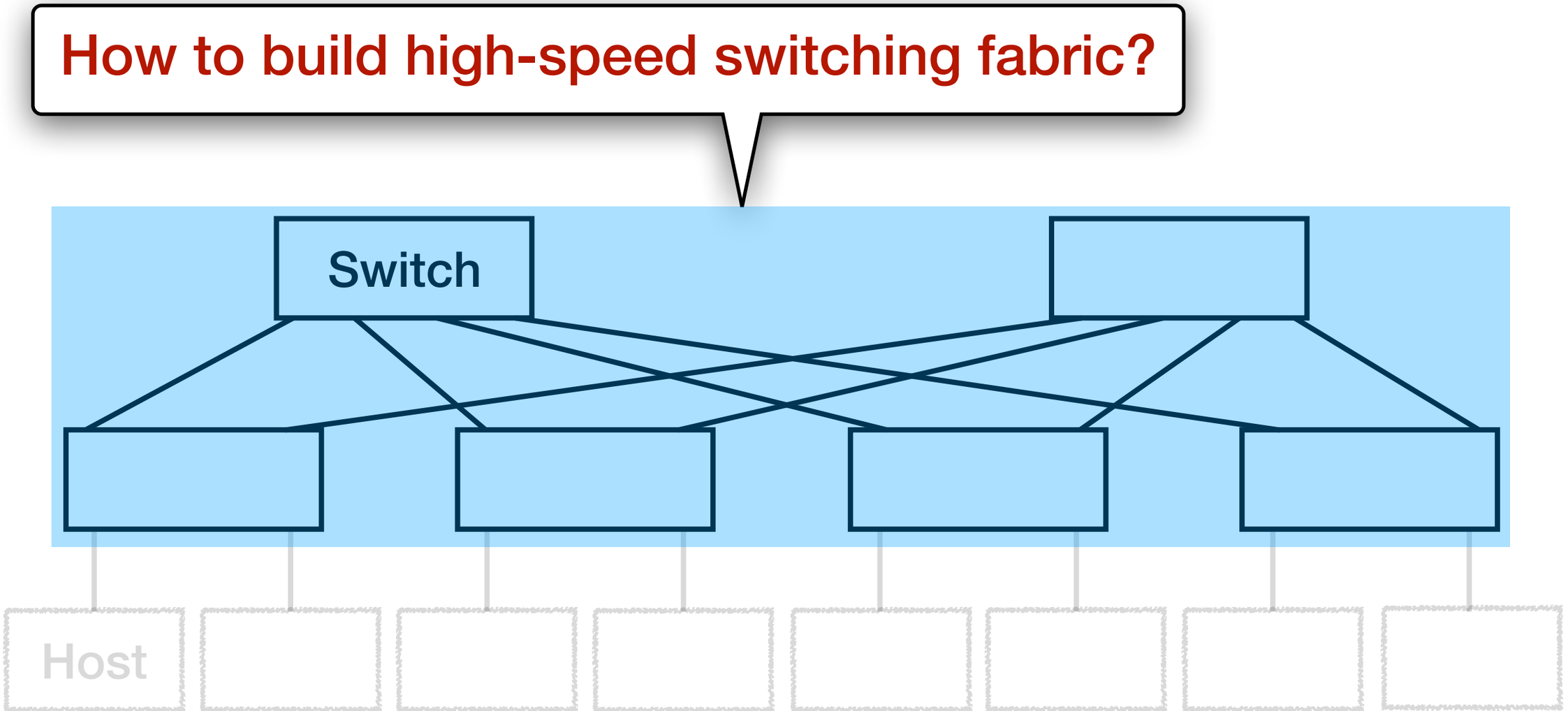


Part II : Switching Fabric



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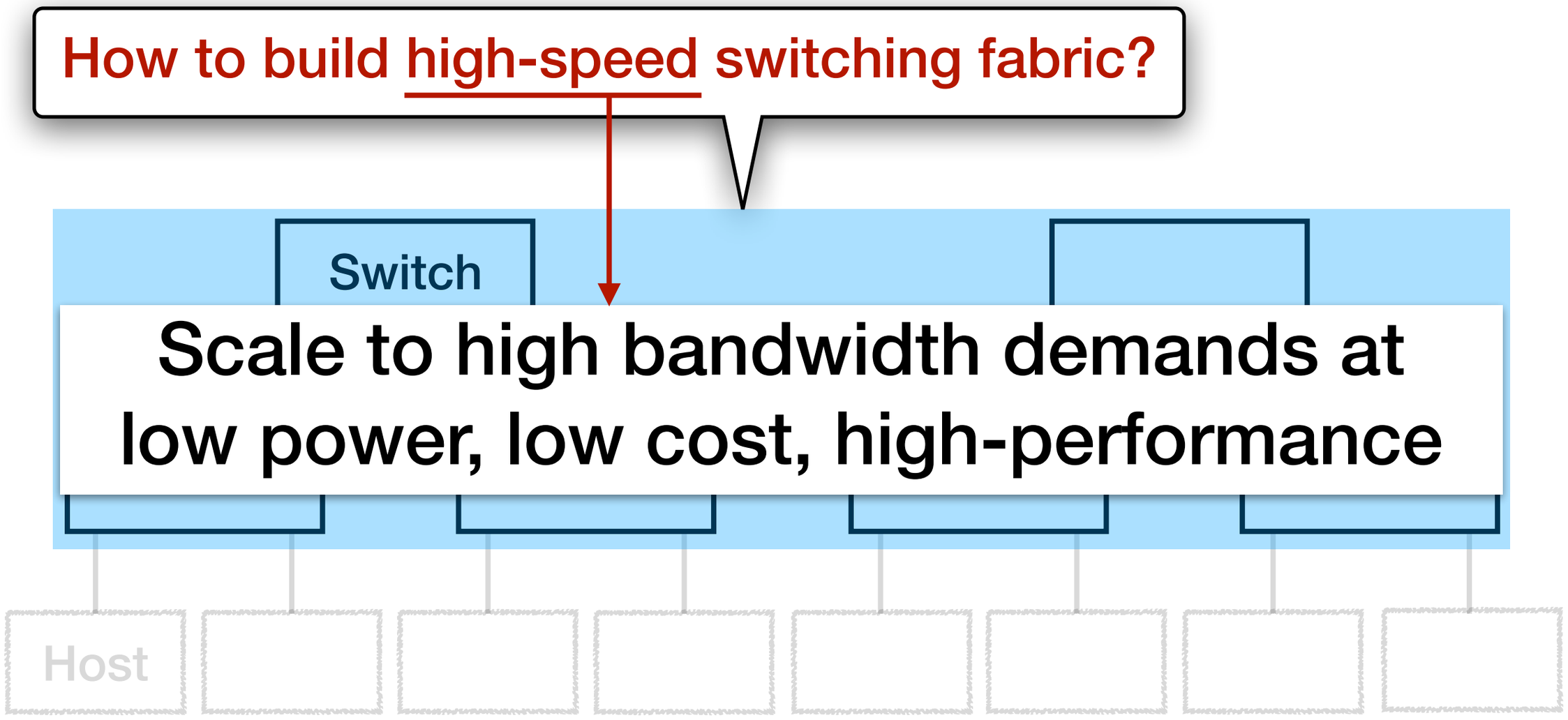


Part II : Switching Fabric

How to build high-speed switching fabric?

Switch

Scale to high bandwidth demands at low power, low cost, high-performance

Host

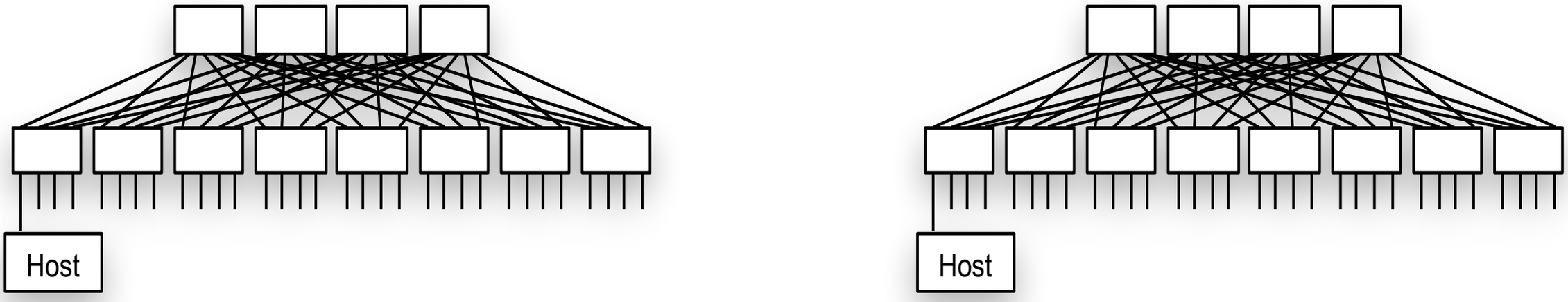
Circuit Switching

Promise of Circuit Switching

Packet Switching

VS.

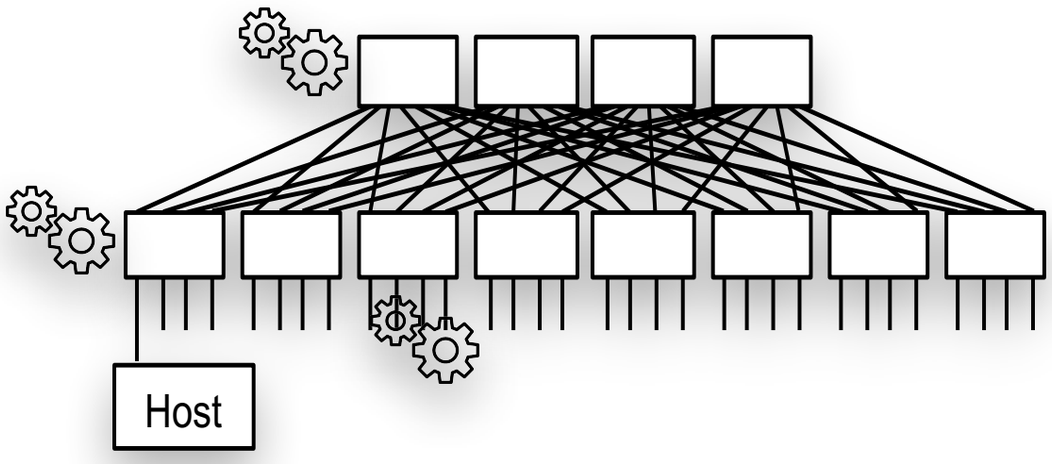
Circuit Switching



Promise of Circuit Switching

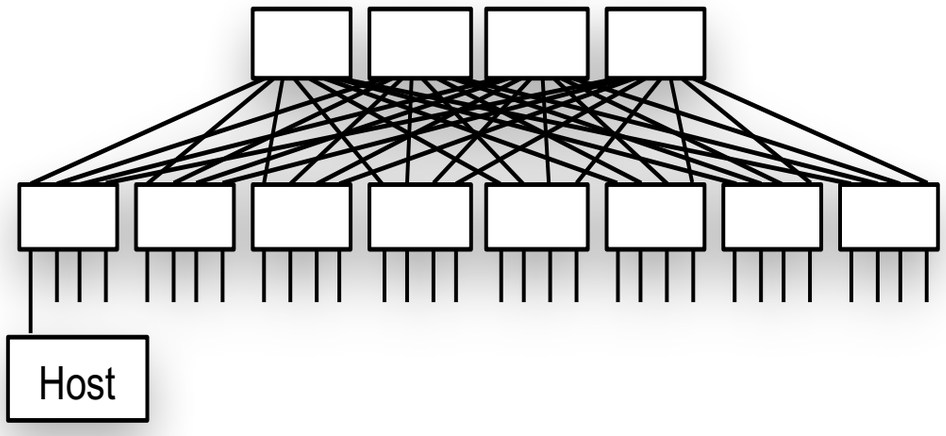
Packet Switching

(Per packet, Per hop Decisions)



VS.

Circuit Switching



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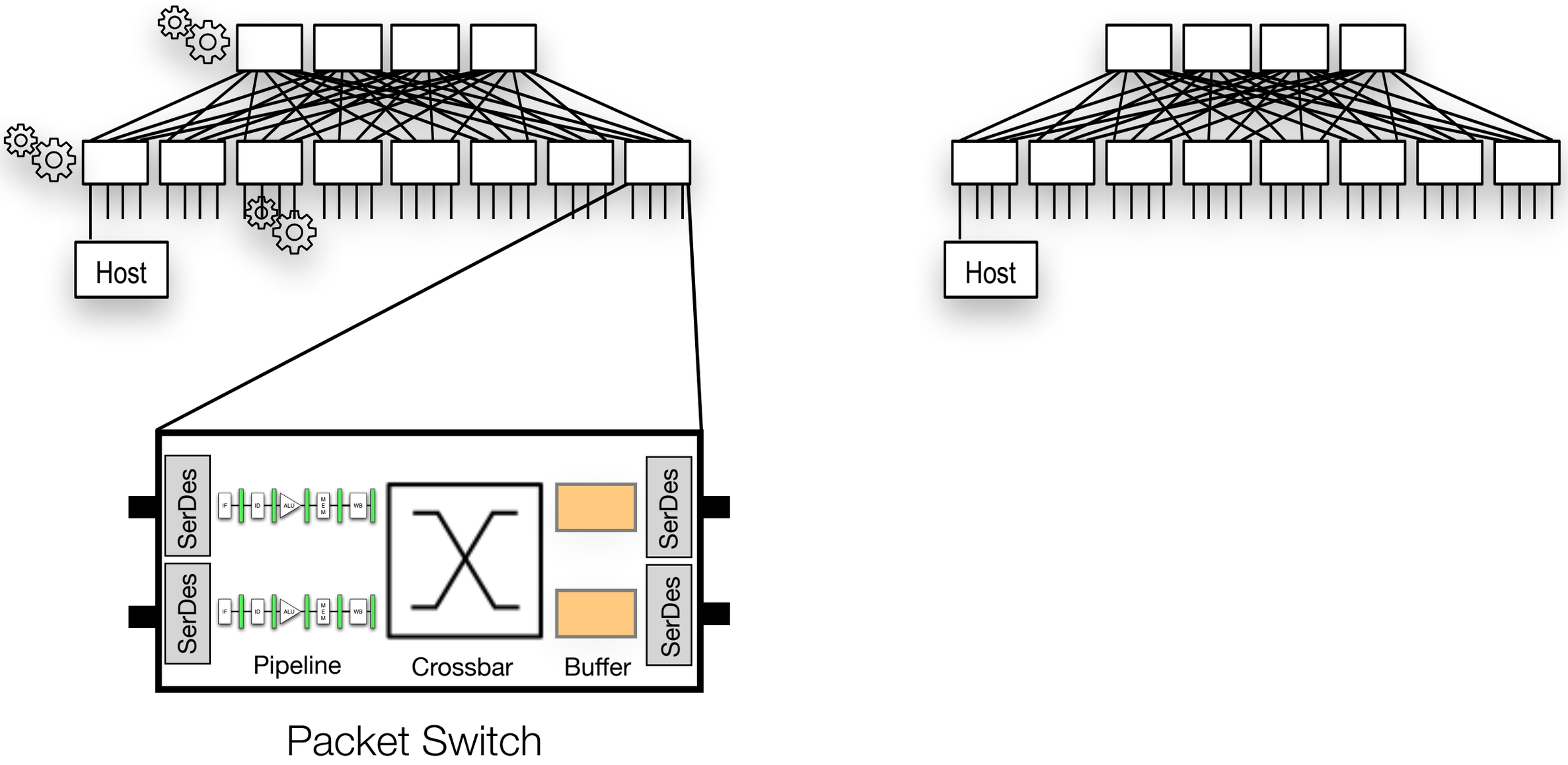

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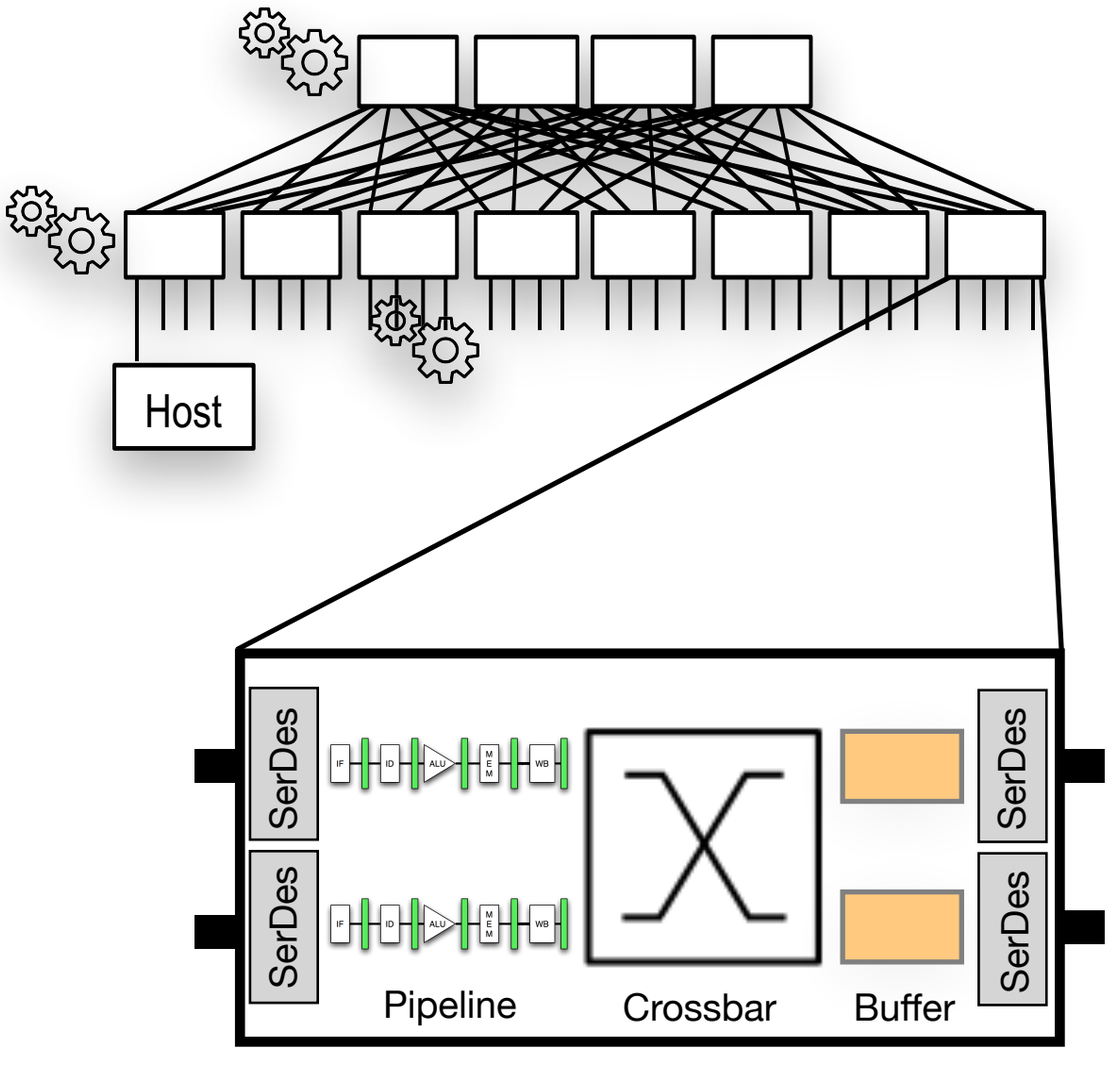

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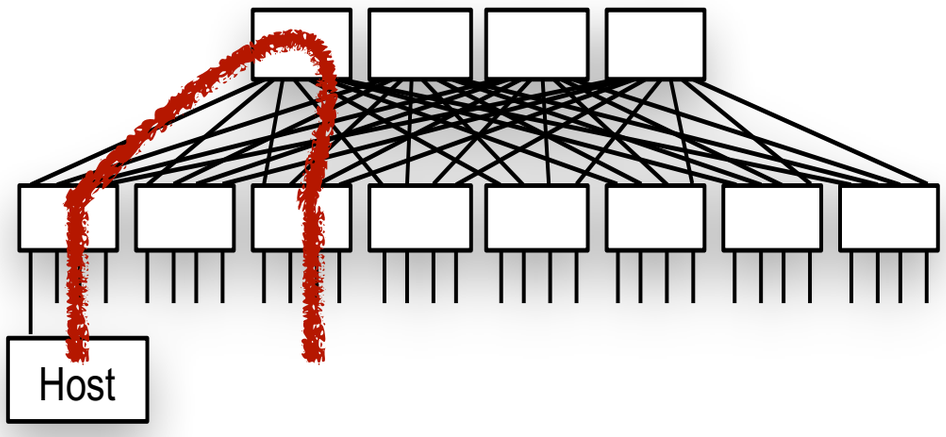

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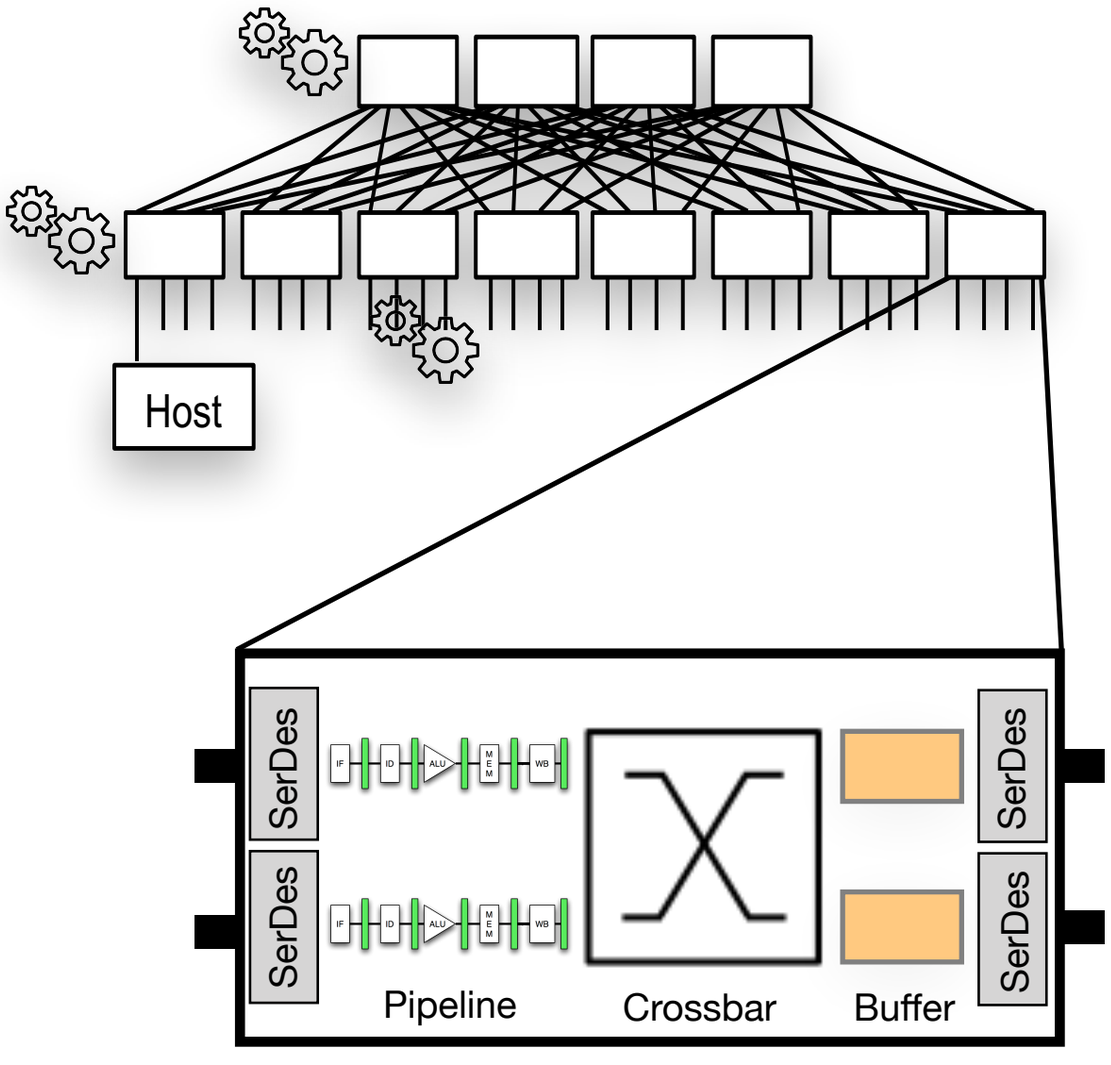

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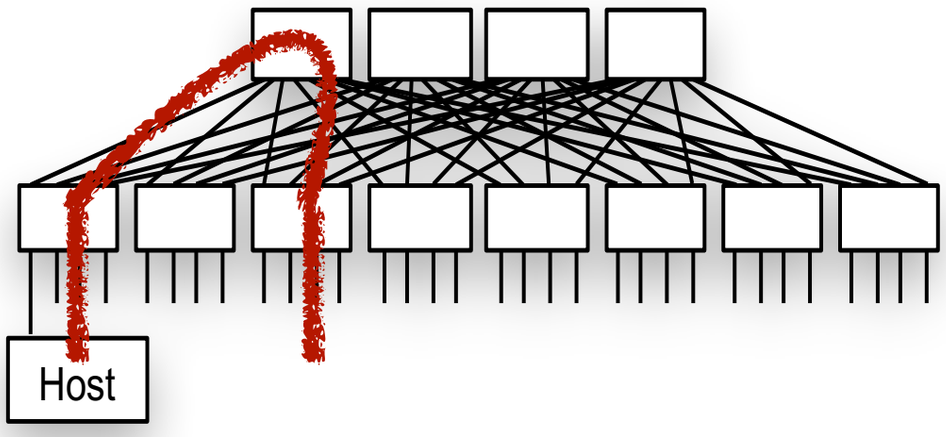

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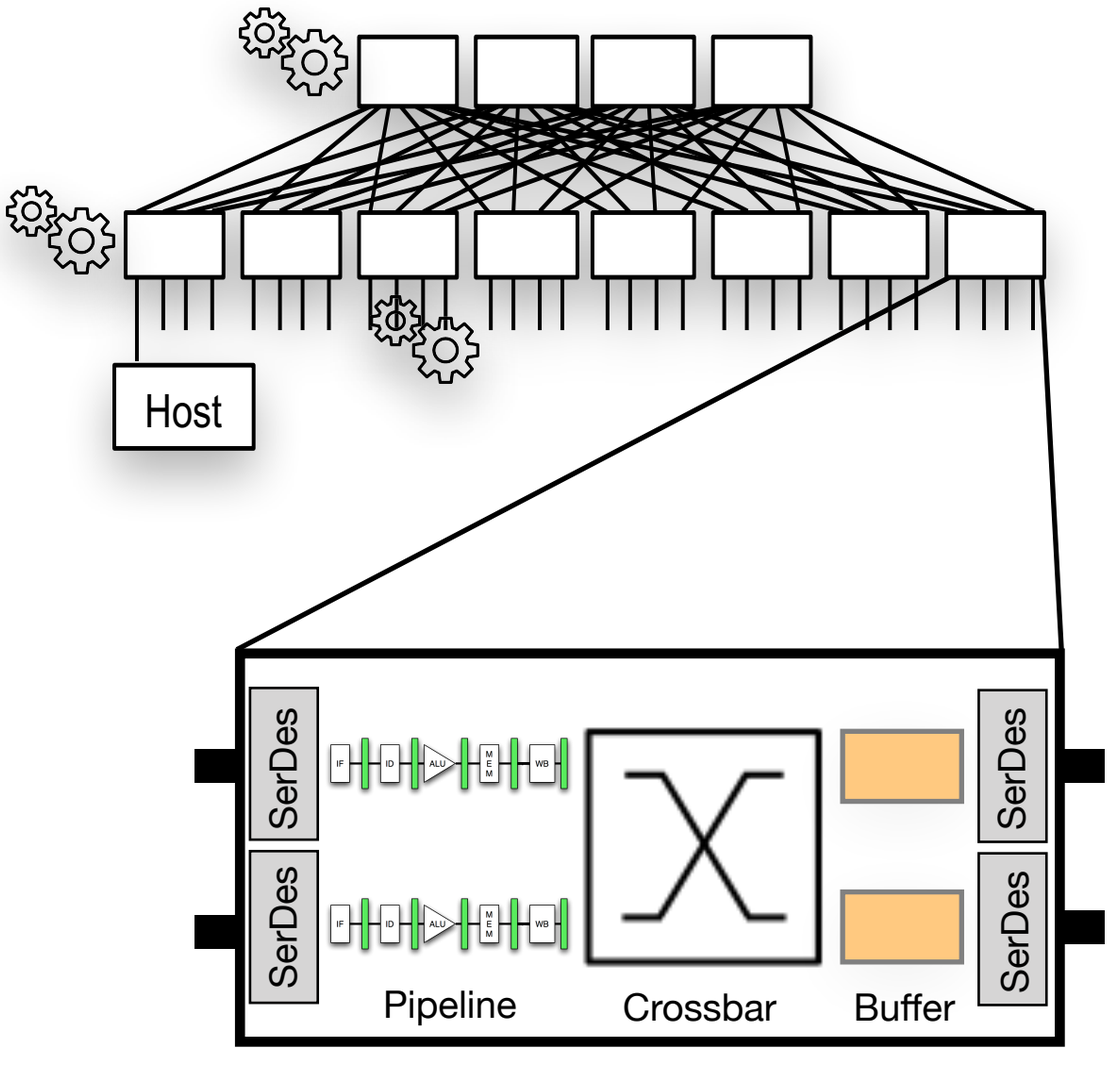

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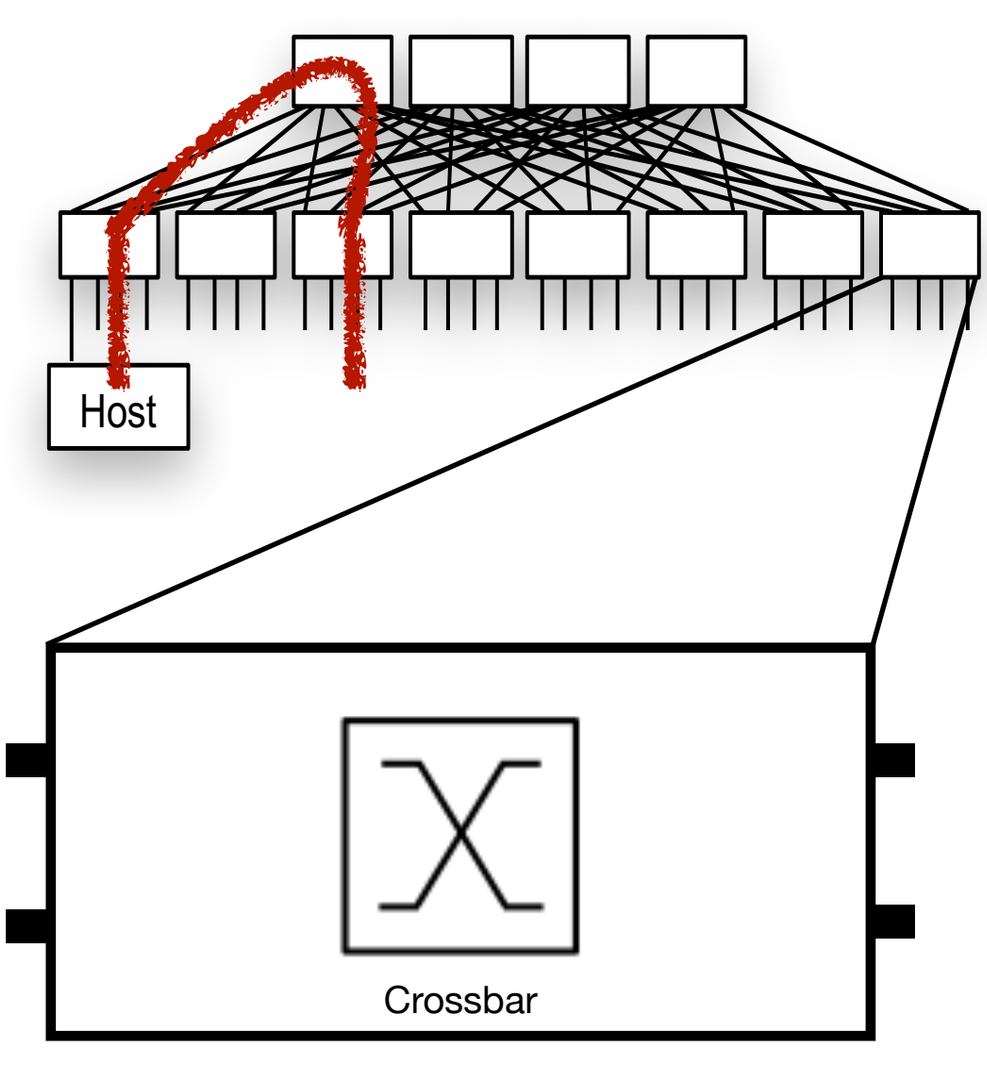

Circuit Switch

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Packet Switching
(Per packet, Per hop Decisions)

VS.

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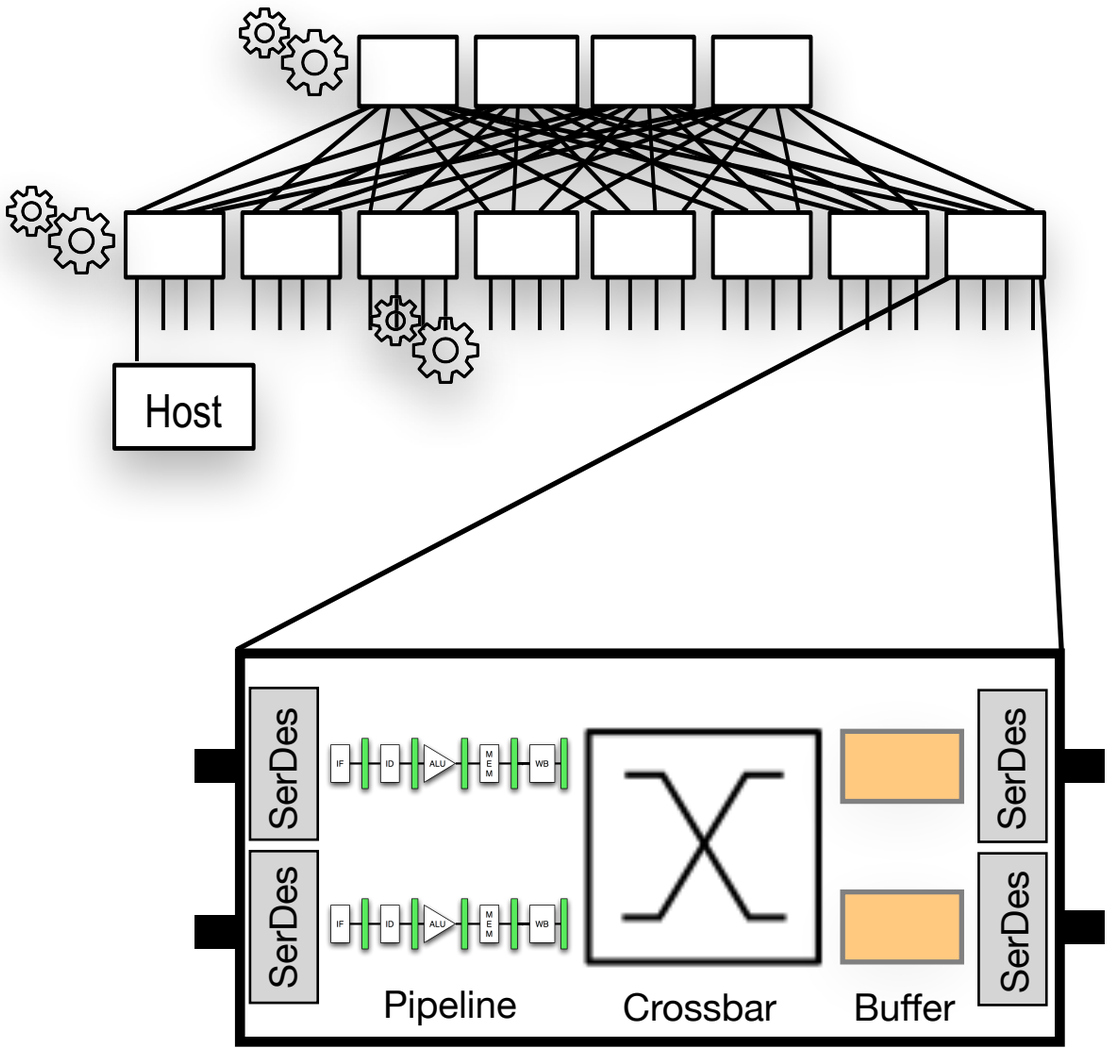
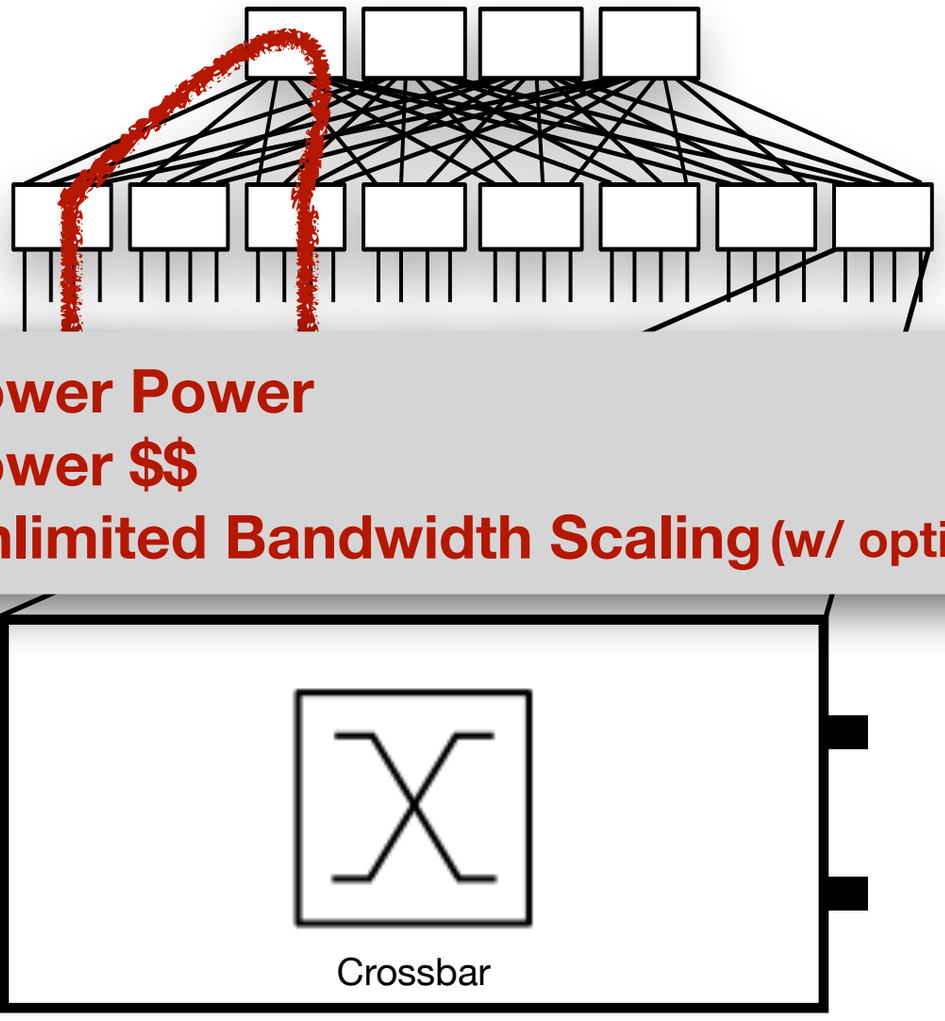
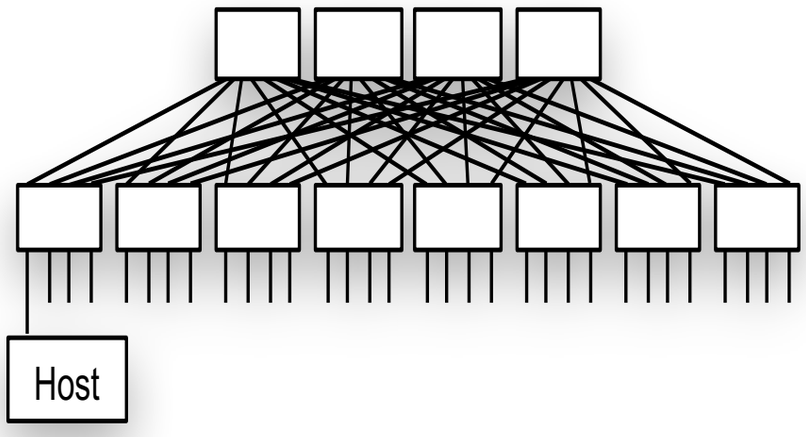


Packet Switch

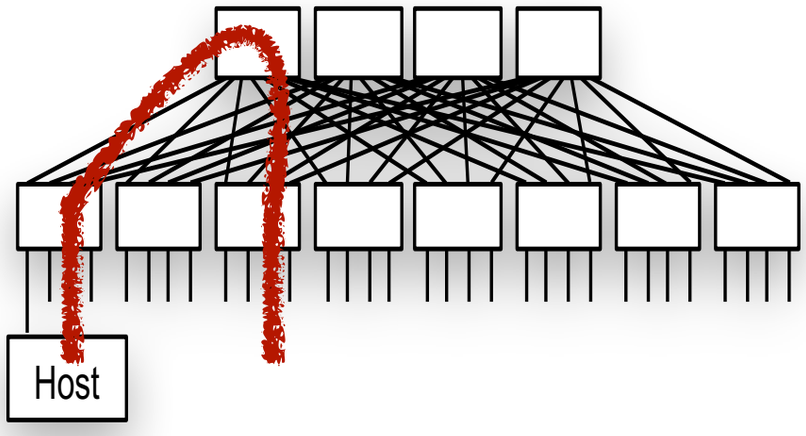


Circuit Switch

Challenge of Circuit Switching

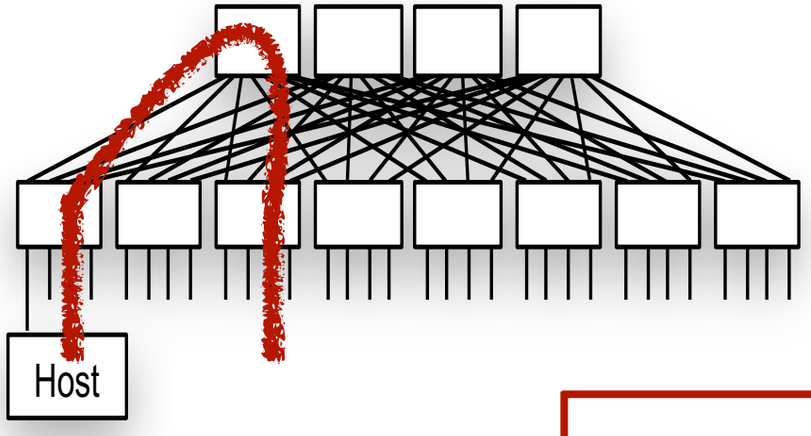


Challenge of Circuit Switching



- Circuit Configuration

Challenge of Circuit Switching



Circuit Configuration

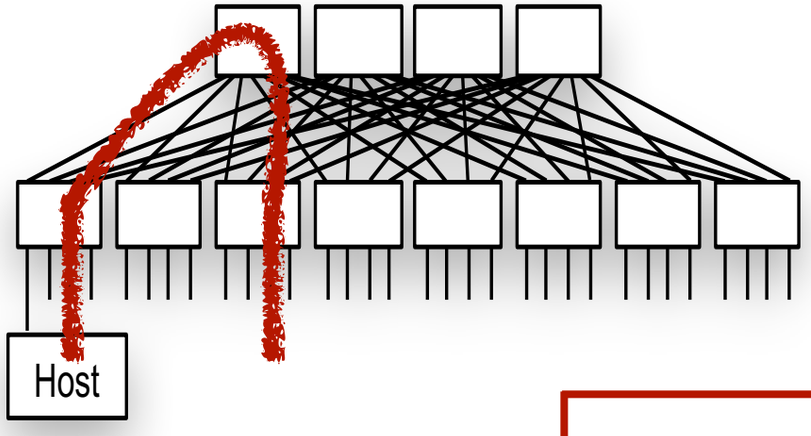
Data Plane

creating physical circuits

Control Plane

circuit scheduling

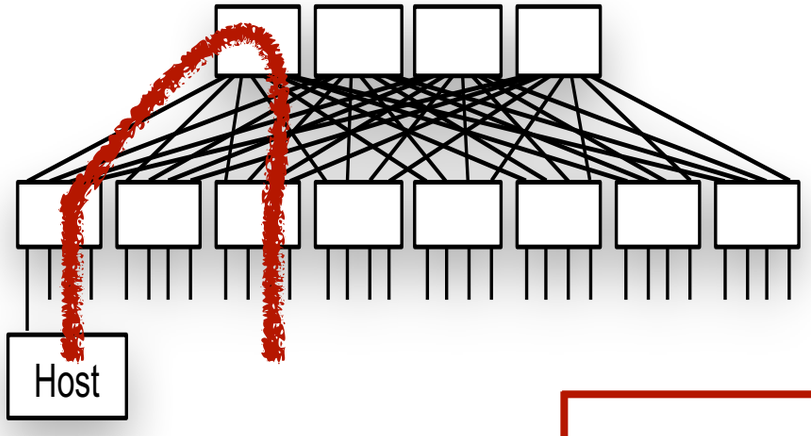
Challenge of Circuit Switching



Circuit Configuration

	Data Plane	Control Plane
	creating physical circuits	circuit scheduling
~2010	milliseconds	

Challenge of Circuit Switching



Circuit Configuration

Data Plane

creating physical circuits

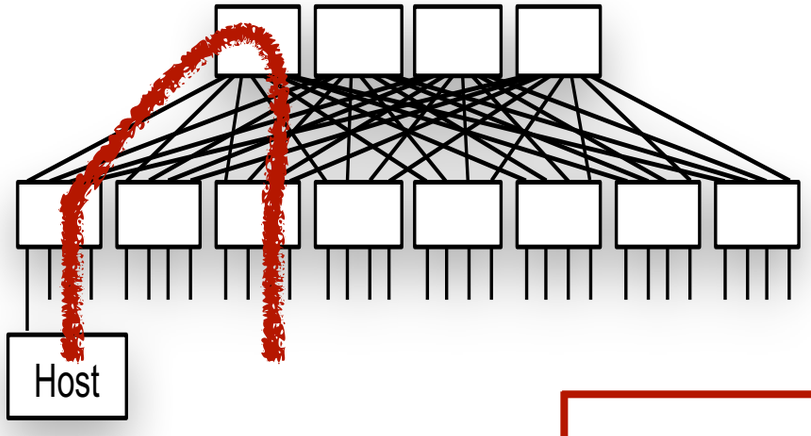
~2010 milliseconds

Today nanoseconds

Control Plane

circuit scheduling

Challenge of Circuit Switching



Circuit Configuration

Data Plane

creating physical circuits

~2010 milliseconds

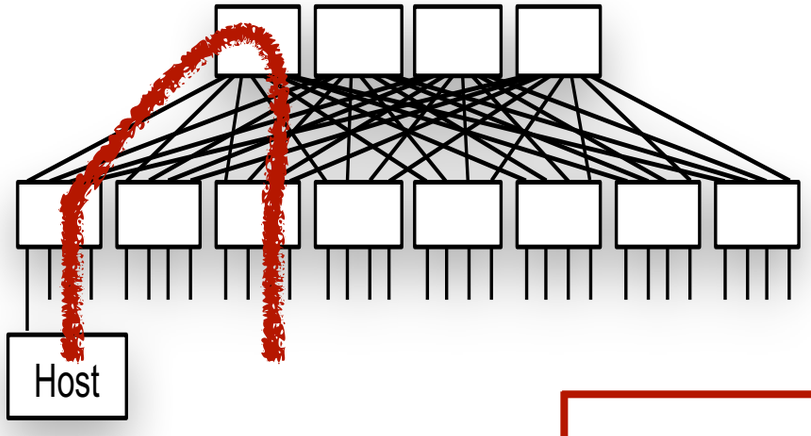
Today nanoseconds

Control Plane

circuit scheduling

Centralized

Challenge of Circuit Switching



Circuit Configuration

Data Plane

creating physical circuits

~2010 milliseconds

Today nanoseconds

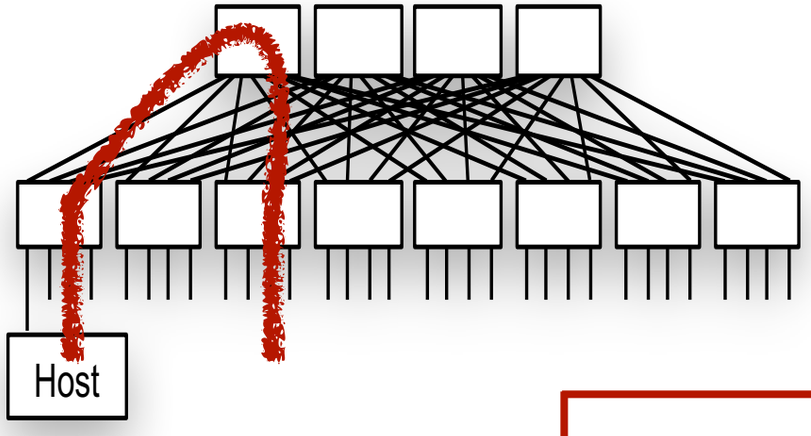
Control Plane

circuit scheduling

Traffic demand →  → Circuits

Centralized

Challenge of Circuit Switching



Circuit Configuration

Data Plane

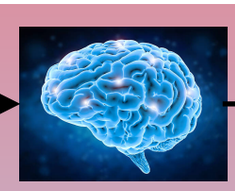
creating physical circuits

~2010 milliseconds

Today nanoseconds

Control Plane

circuit scheduling

Traffic demand →  → Circuits

Centralized

???

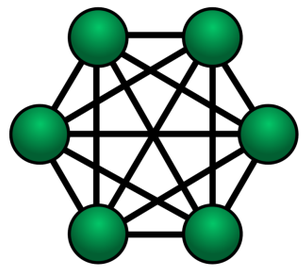
How to build a fast control plane for circuit switching?

nanosecond-scale circuit scheduling with high performance

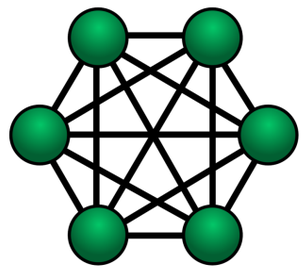
How to build a fast control plane for circuit switching?

nanosecond-scale circuit scheduling with high performance

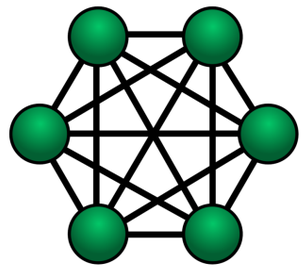
Shoal



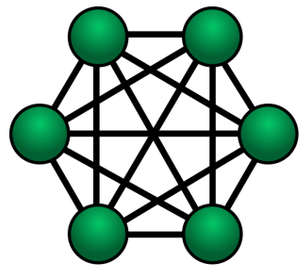
Shoal



Shoal



1. **Physical Layer :** Fast circuit scheduling mechanism
2. **Routing :** Bounded worst-case throughput
3. **Congestion Control :** Bounded worst-case queuing

Shoal 

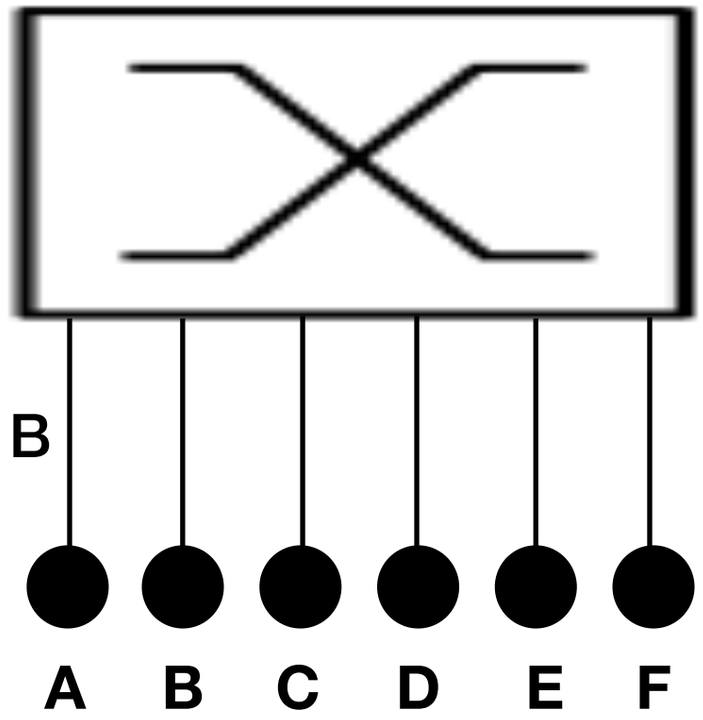
1. Physical Layer : Fast circuit scheduling mechanism

2. Routing : Bounded worst-case throughput

3. Congestion Control : Bounded worst-case queuing

Achieves comparable or better performance than several recent packet-switched network designs

Physical Layer



Physical Topology

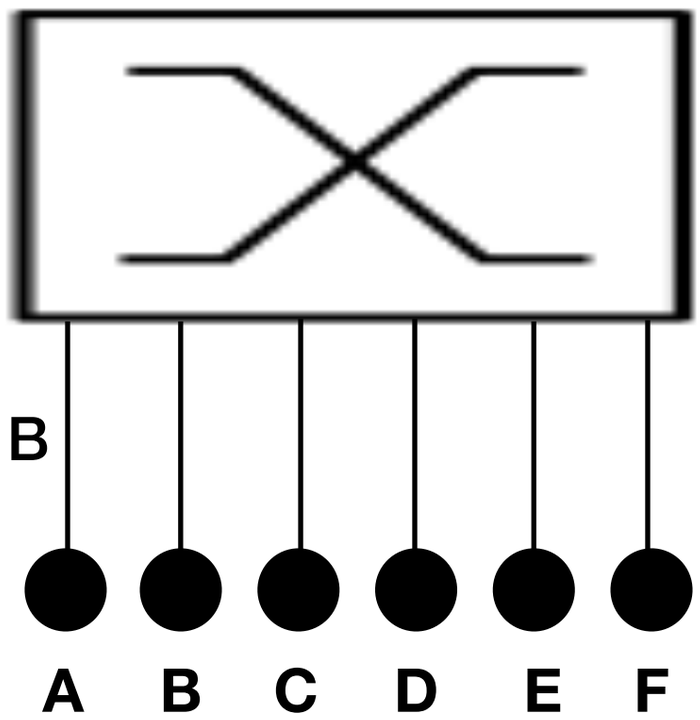
Physical Layer

End-hosts

	1	2	3	4	5
A					
B					
C					
D					
E					
F					

static, pre-defined schedule

+



Physical Topology

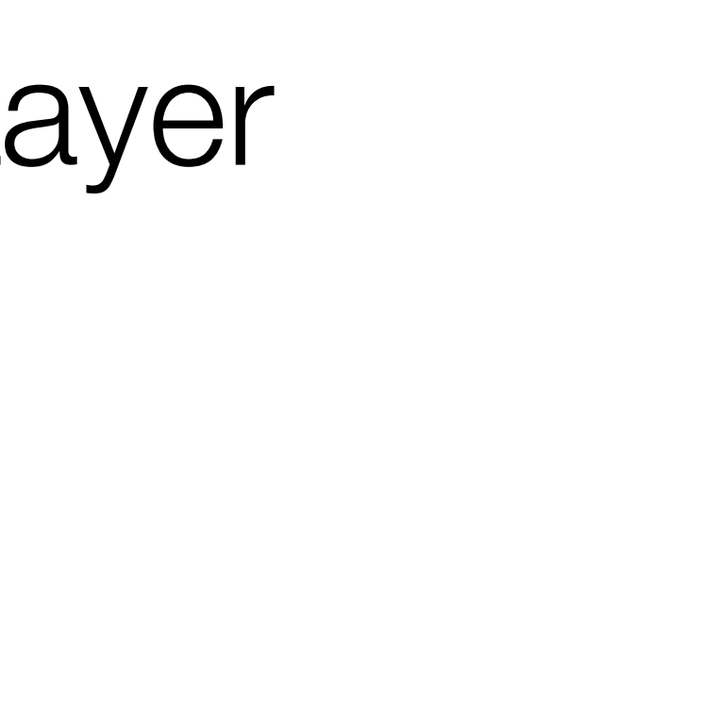
Physical Layer

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A					
B					
C					
D					
E					
F					

static, pre-defined schedule

+



Physical Topology

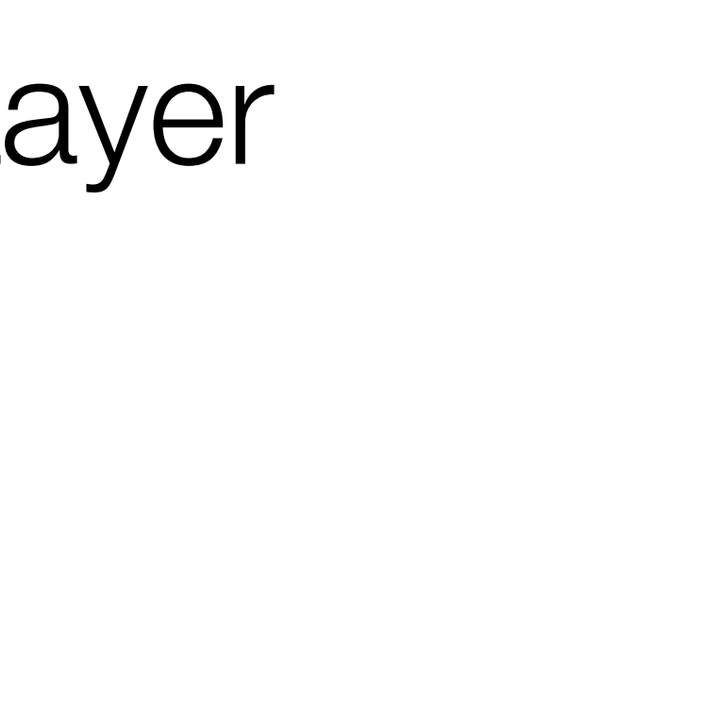
Physical Layer

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B				
B	C				
C	D				
D	E				
E	F				
F	A				

static, pre-defined schedule

+



Physical Topology

Physical Layer

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B				
B	C				
C	D				
D	E				
E	F				
F	A				

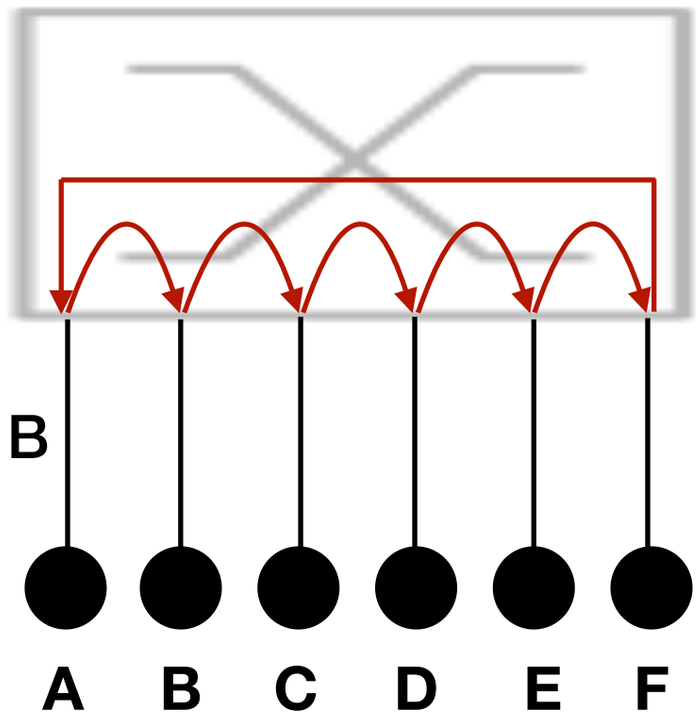
static, pre-defined schedule

+

Synchronous System

ns-precision time sync

DTP [SIGCOMM'16]



Physical Topology

Physical Layer

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B	C	D	E	F
B	C	D	E	F	A
C	D	E	F	A	B
D	E	F	A	B	C
E	F	A	B	C	D
F	A	B	C	D	E

static, pre-defined schedule

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Synchronous System

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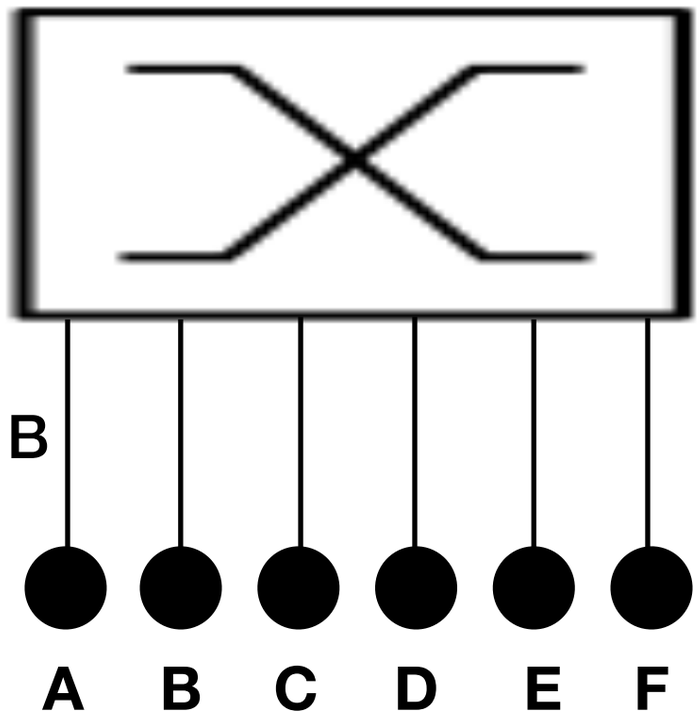

Physical Topology

Physical Layer

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B	C	D	E	F
B	C	D	E	F	A
C	D	E	F	A	B
D	E	F	A	B	C
E	F	A	B	C	D
F	A	B	C	D	E

static, pre-defined schedule

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Synchronous System

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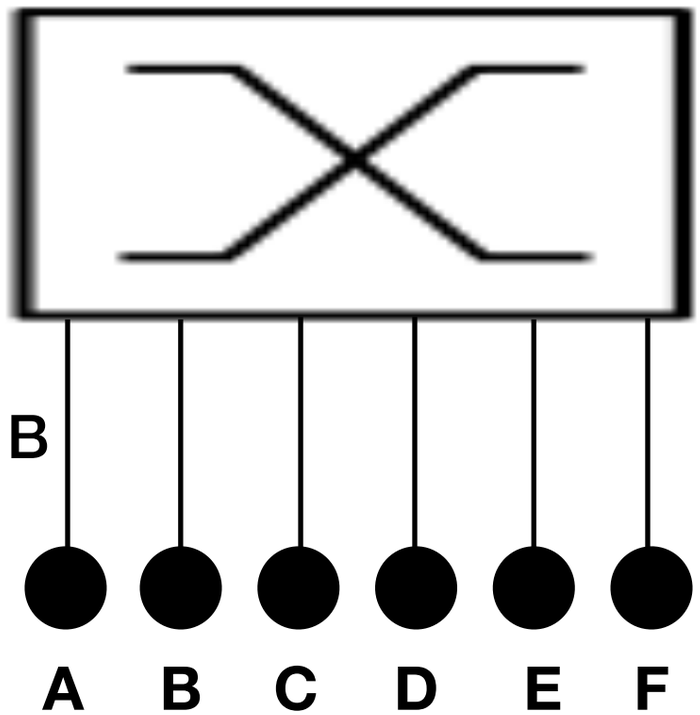
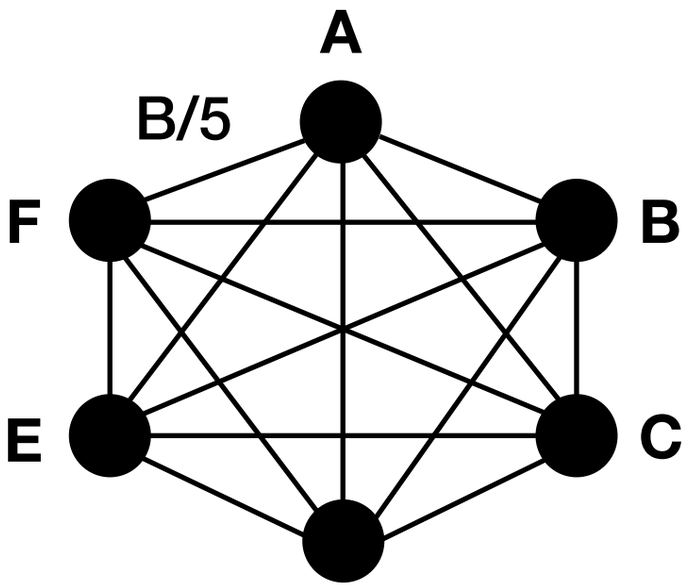
DTP [SIGCOMM'16]



Physical Topology

Physical Layer



Full Mesh
Virtual Topology

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B	C	D	E	F
B	C	D	E	F	A
C	D	E	F	A	B
D	E	F	A	B	C
E	F	A	B	C	D
F	A	B	C	D	E

static, pre-defined schedule

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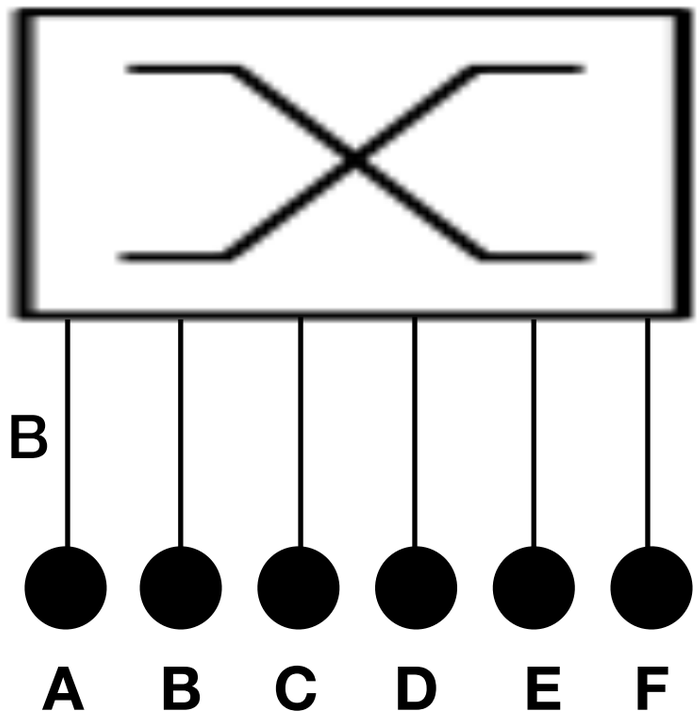
Synchronous System

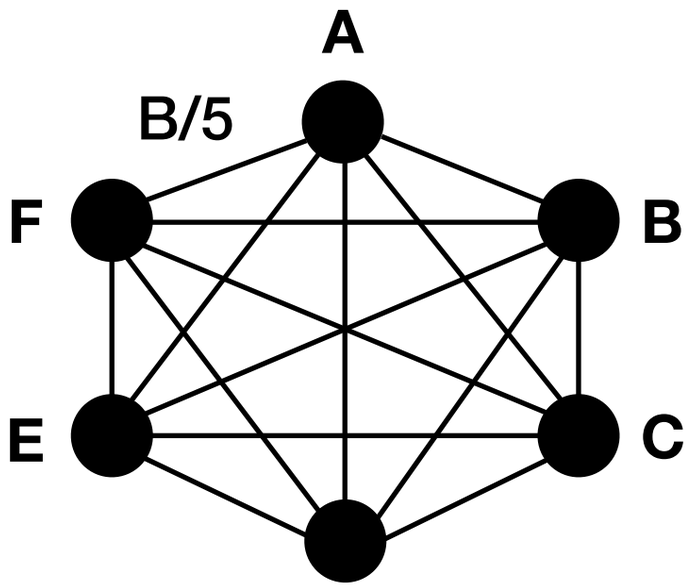
ns-precision time sync

DTP [SIGCOMM'16]



Physical Topology

Physical Layer



Full Mesh
Virtual Topology

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B	C	D	E	F
B	C	D	E	F	A
C	D	E	F	A	B
D	E	F	A	B	C
E	F	A	B	C	D
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static, pre-defined schedule

+

Synchronous System

ns-precision time sync

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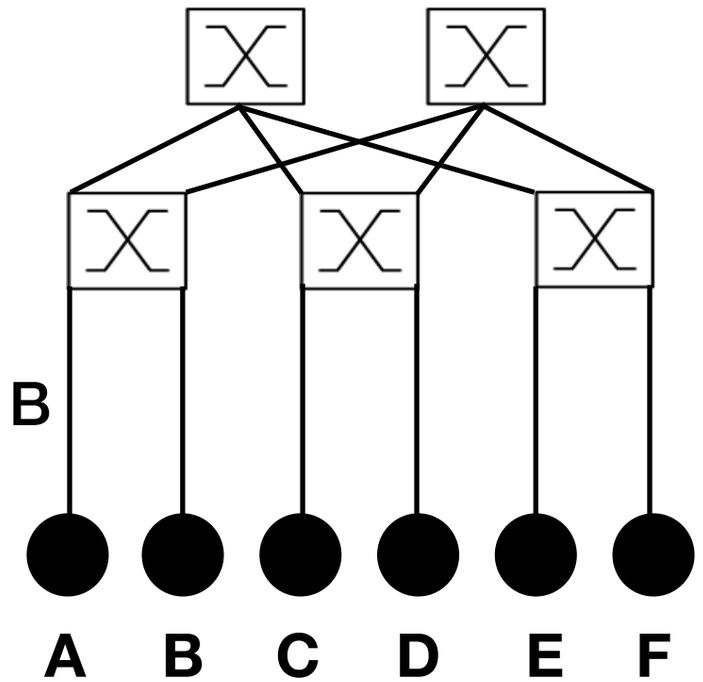
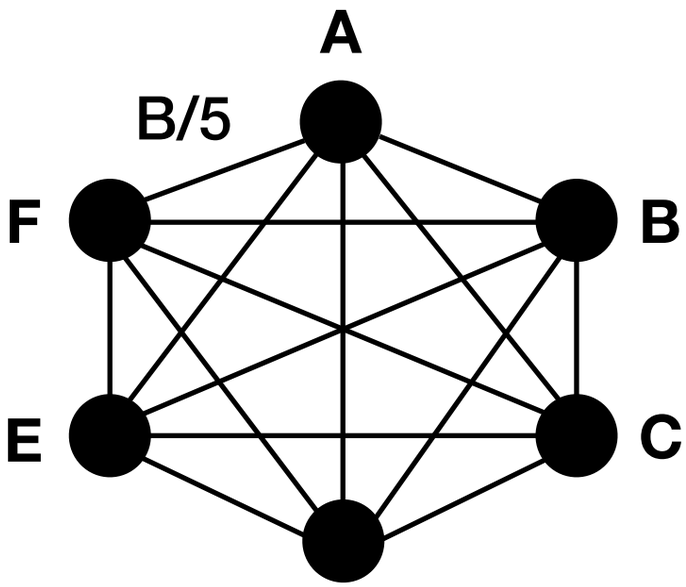


Physical Topology

Physical Layer



Full Mesh
Virtual Topology

N-1 timeslots (epoch)

End-hosts	1	2	3	4	5
A	B	C	D	E	F
B	C	D	E	F	A
C	D	E	F	A	B
D	E	F	A	B	C
E	F	A	B	C	D
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static, pre-defined schedule

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Synchronous System

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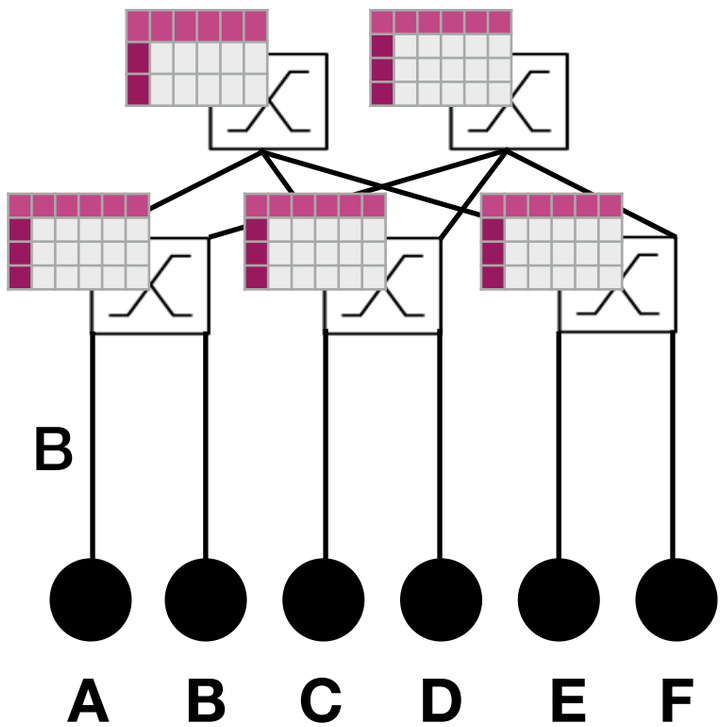
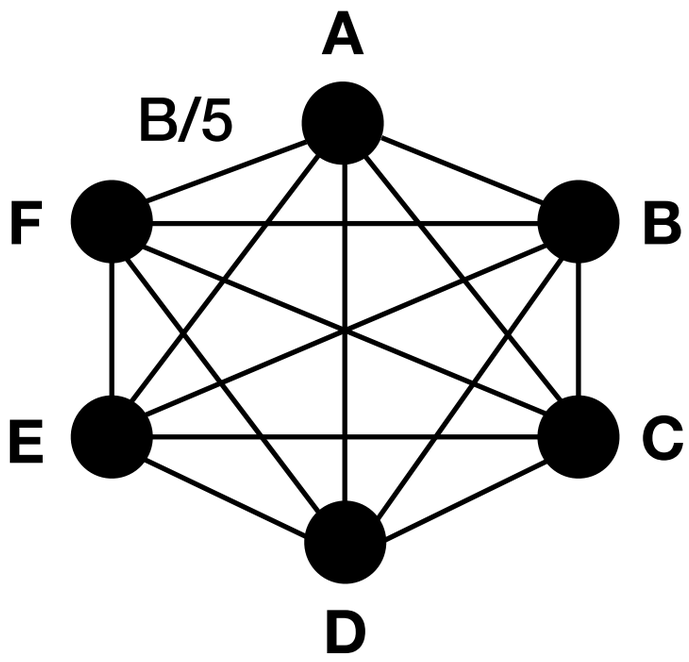
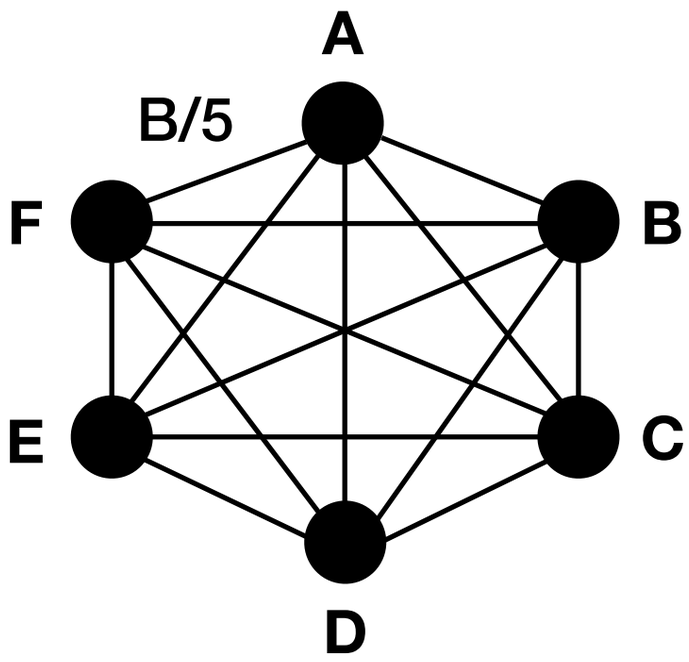


Physical Topology

Routing & Congestion Control

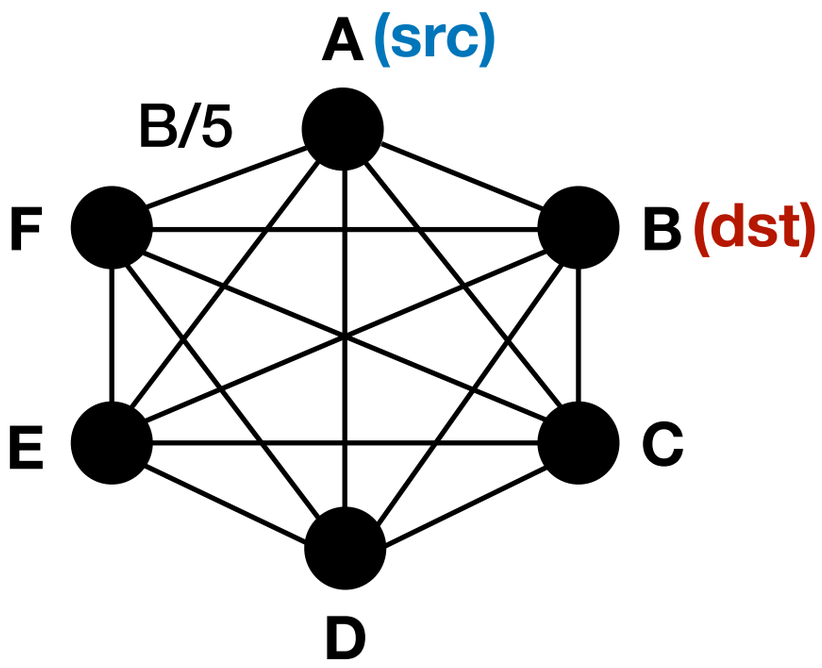


Routing & Congestion Control



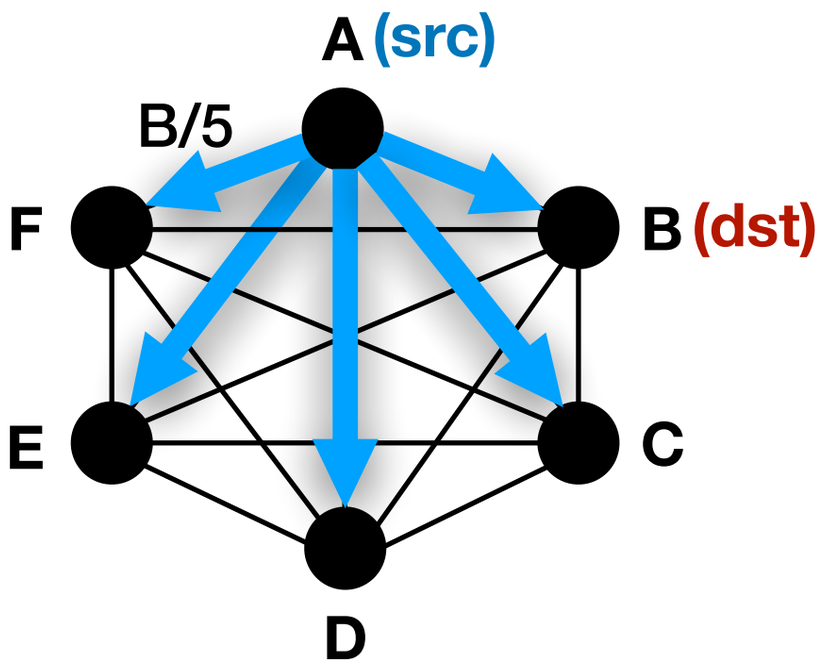
Valiant Load Balancing

Routing & Congestion Control



Valiant
Load
Balancing

Routing & Congestion Control

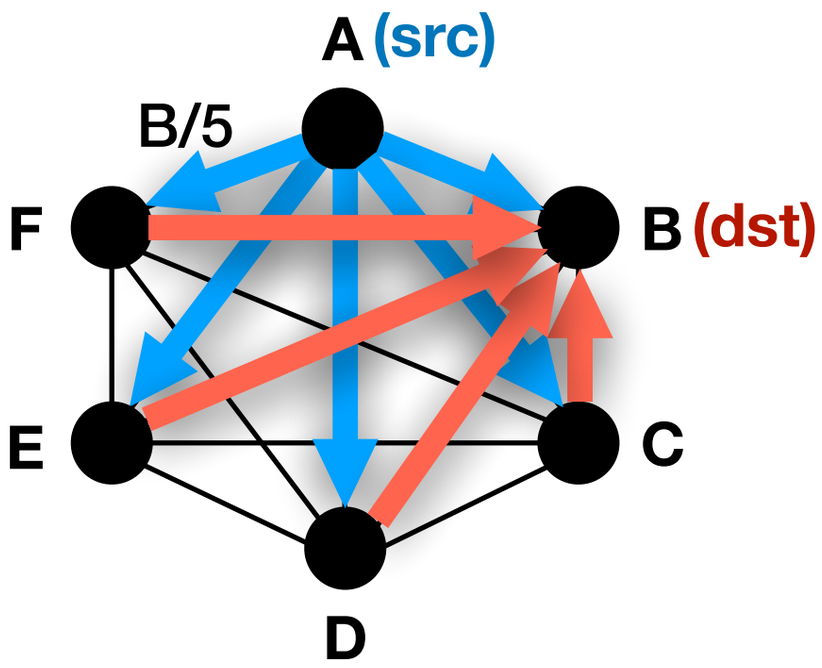


Valiant Load Balancing

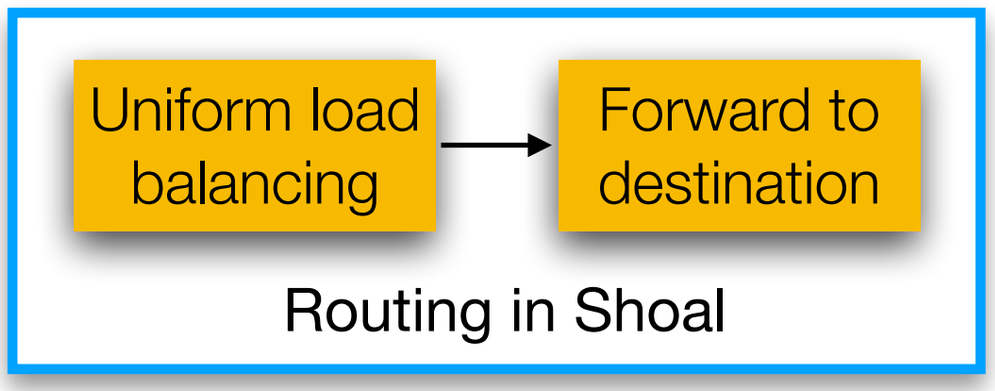
Uniform load balancing

Routing in Shoal

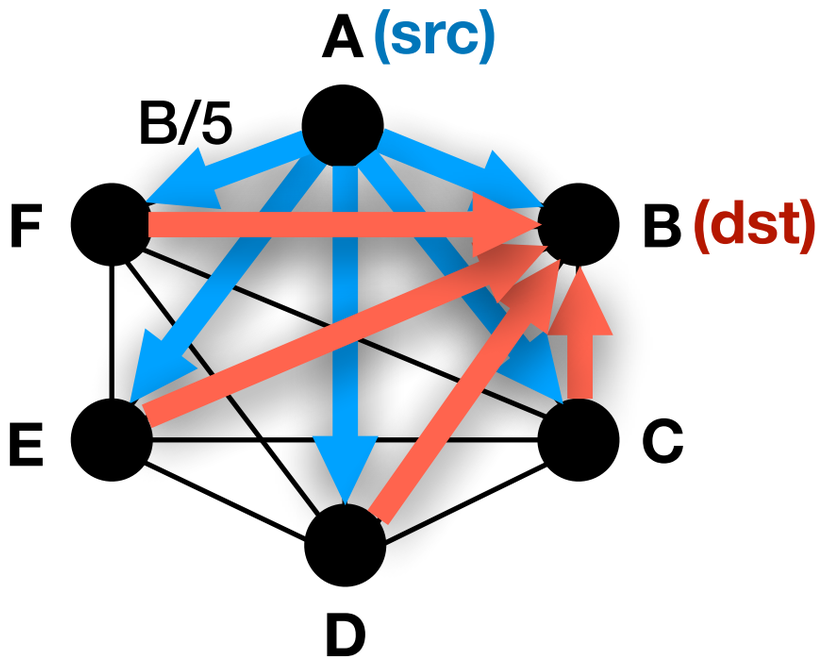
Routing & Congestion Control



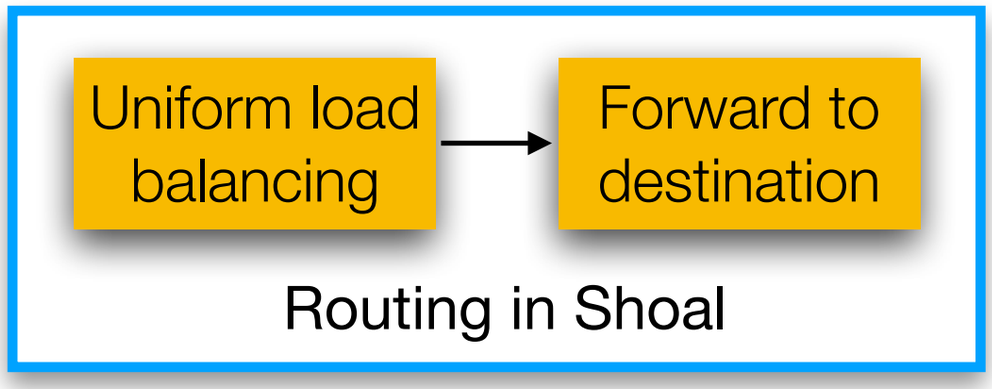
Valiant Load Balancing



Routing & Congestion Control

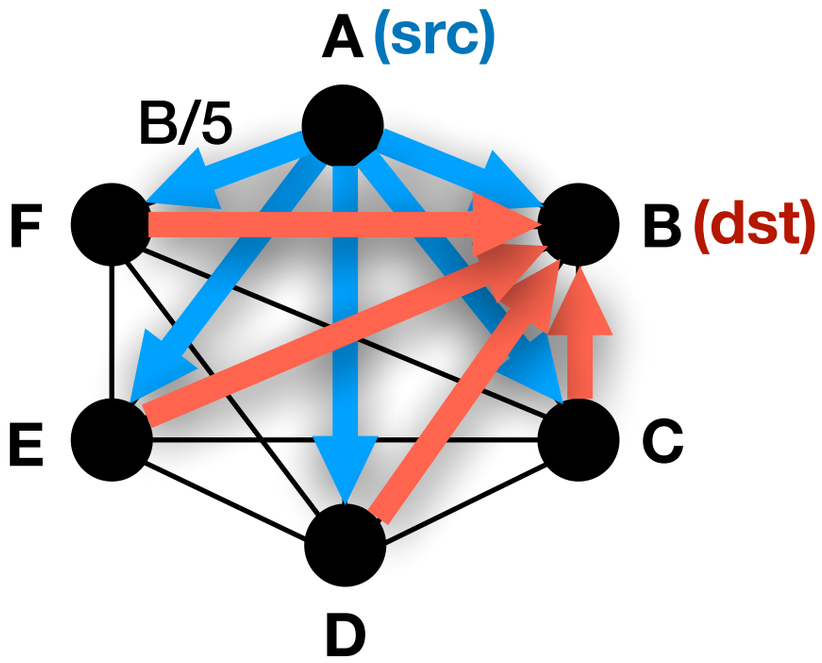


Valiant Load Balancing

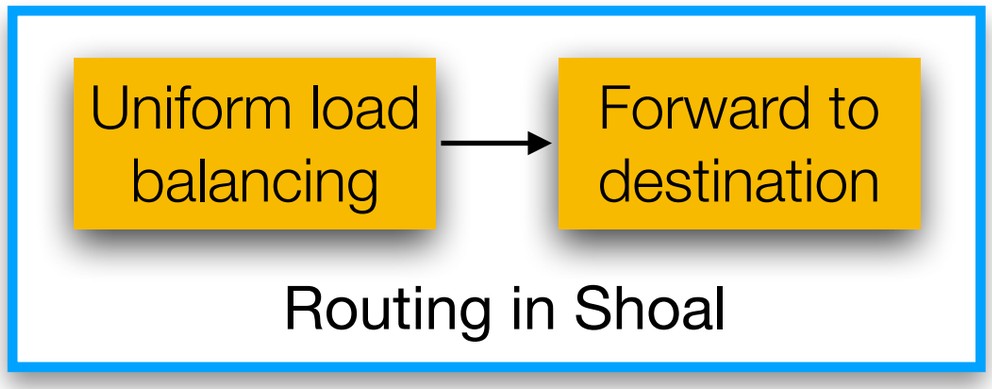


Bounded worst-case throughput of 50%
compared to an ideal packet-switched network

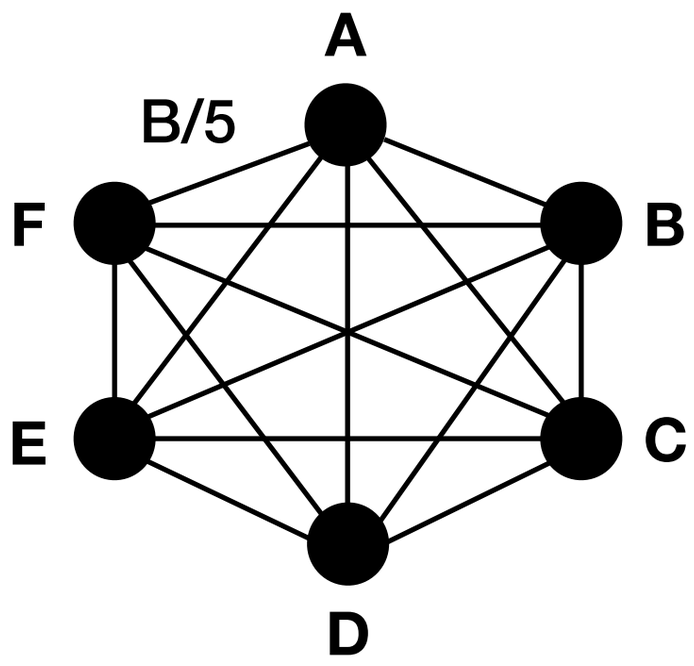
Routing & Congestion Control



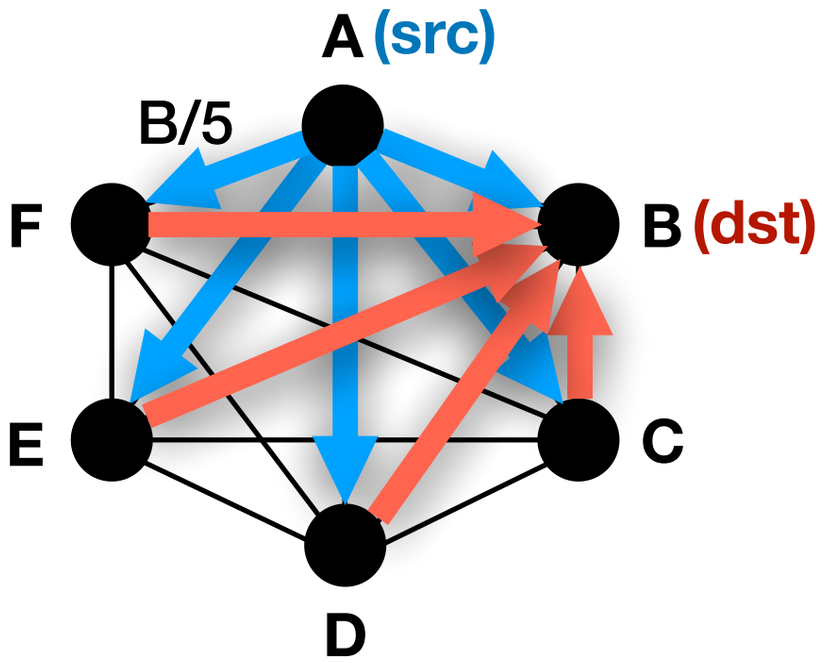
Valiant Load Balancing



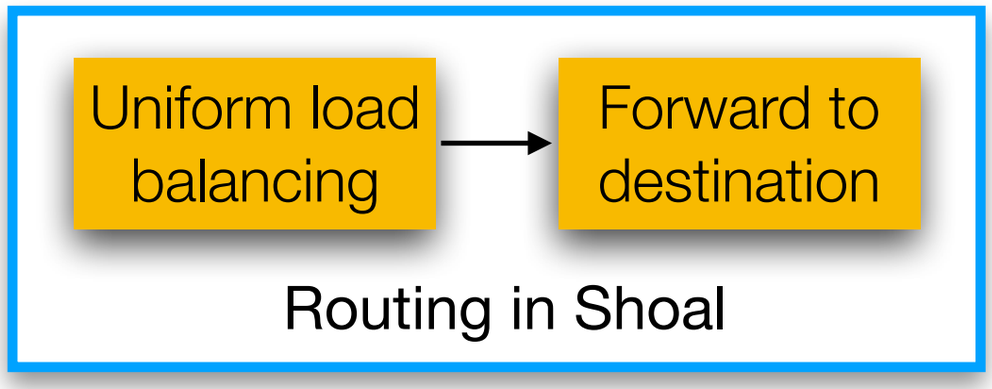
Bounded worst-case throughput of 50% compared to an ideal packet-switched network



Routing & Congestion Control



Valiant Load Balancing



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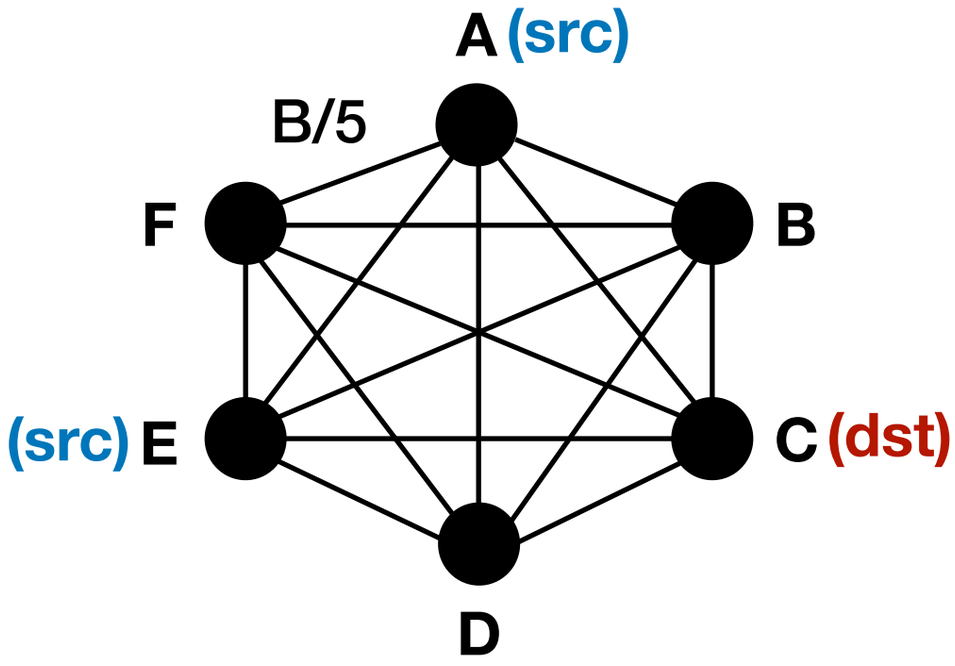
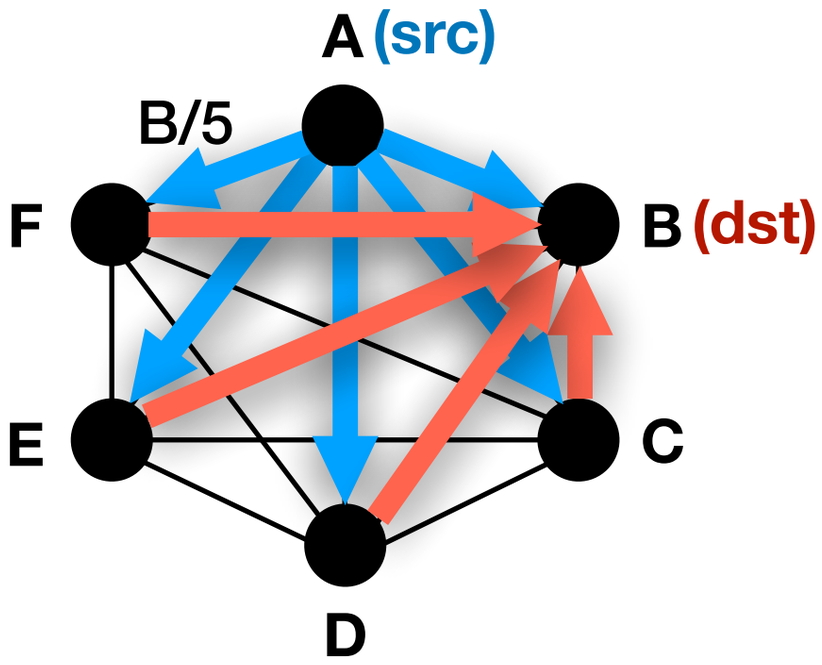
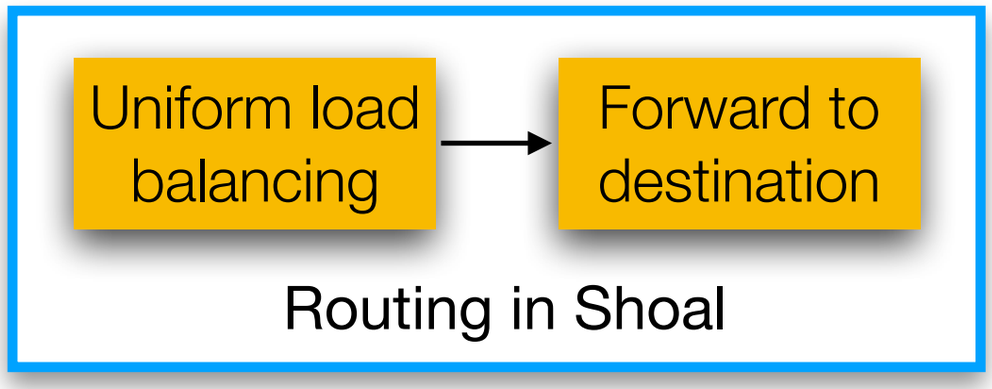


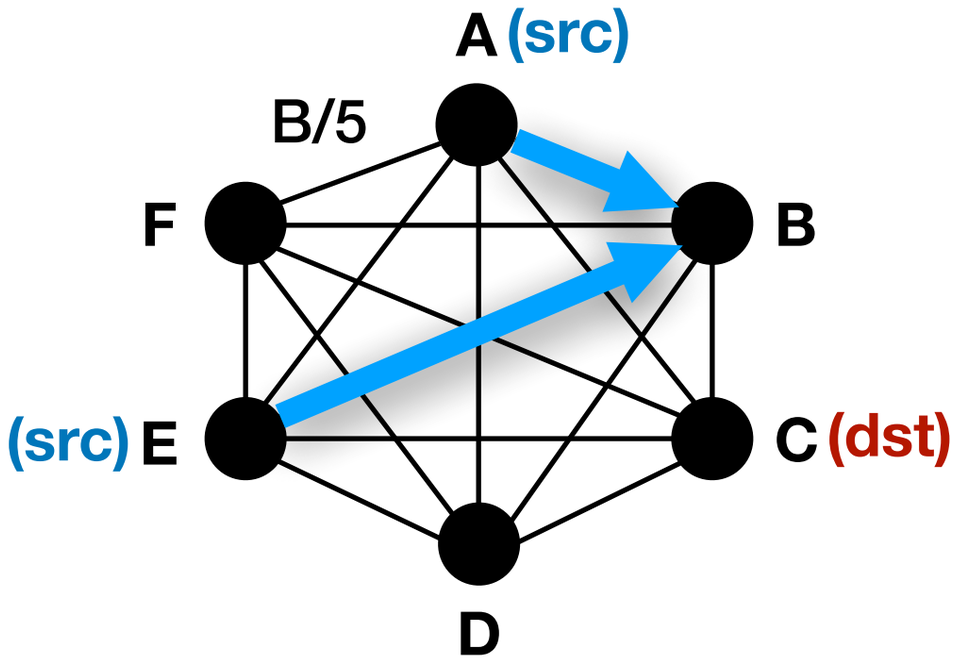
Routing & Congestion Control



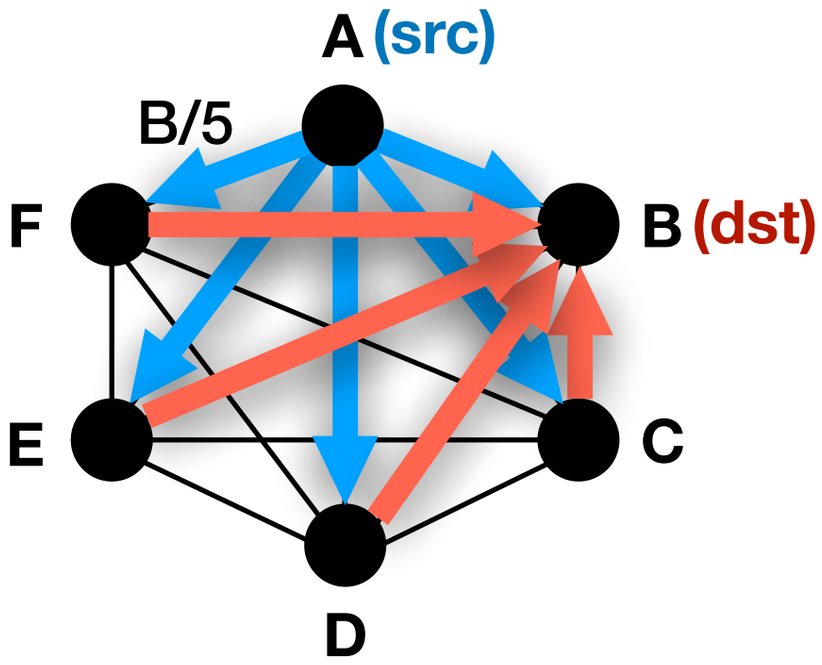
Valiant Load Balancing



Bounded worst-case throughput of 50% compared to an ideal packet-switched network



Routing & Congestion Control



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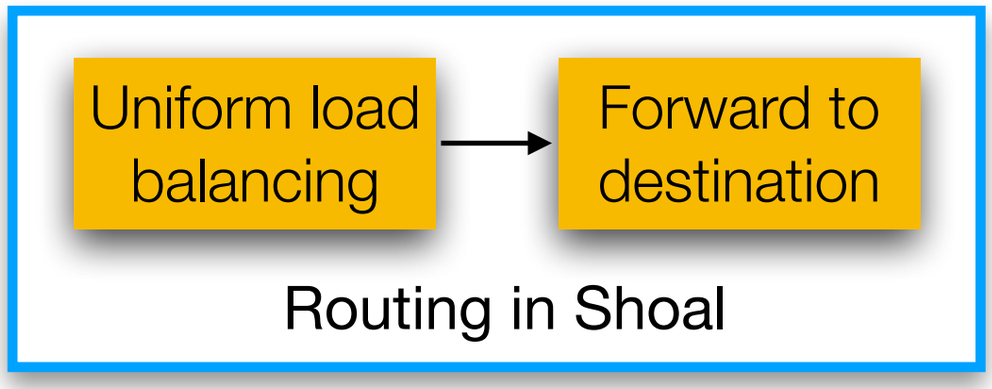

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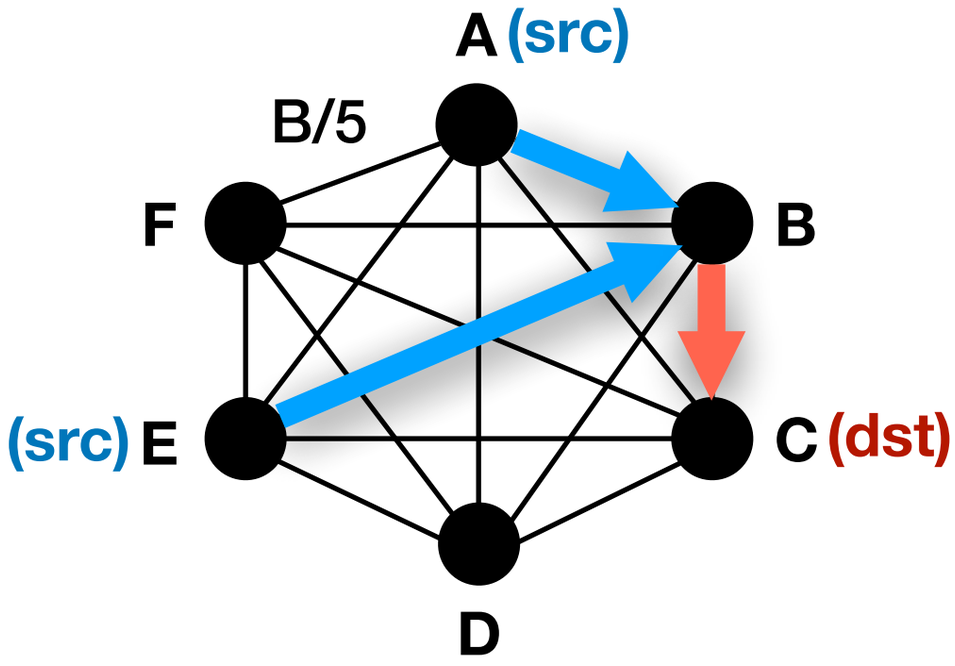
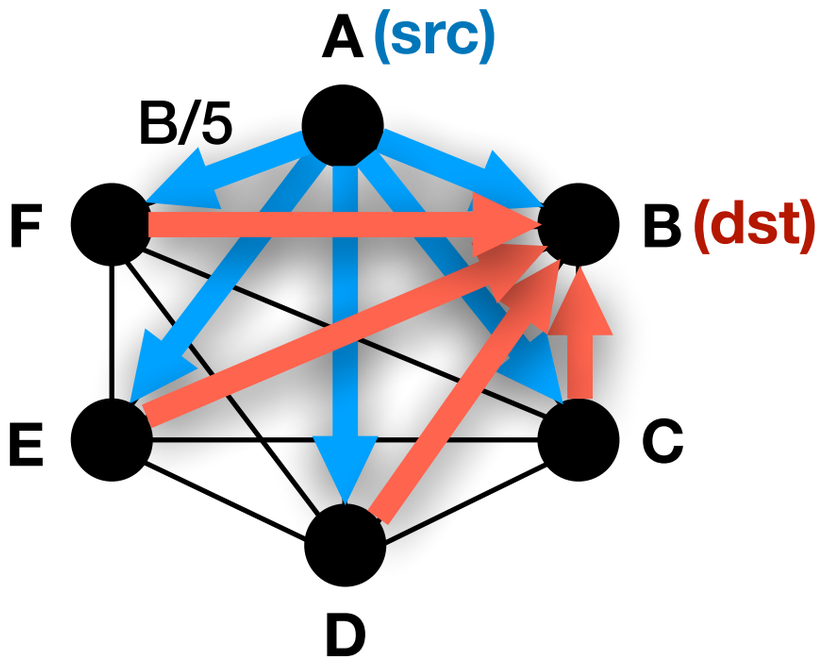
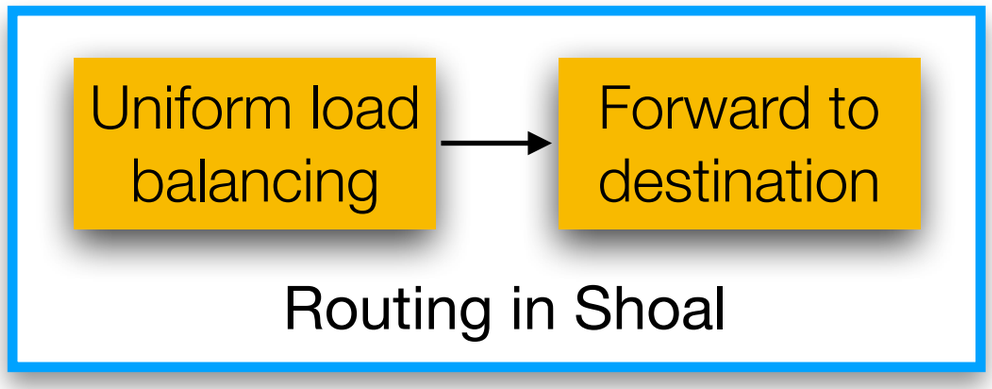


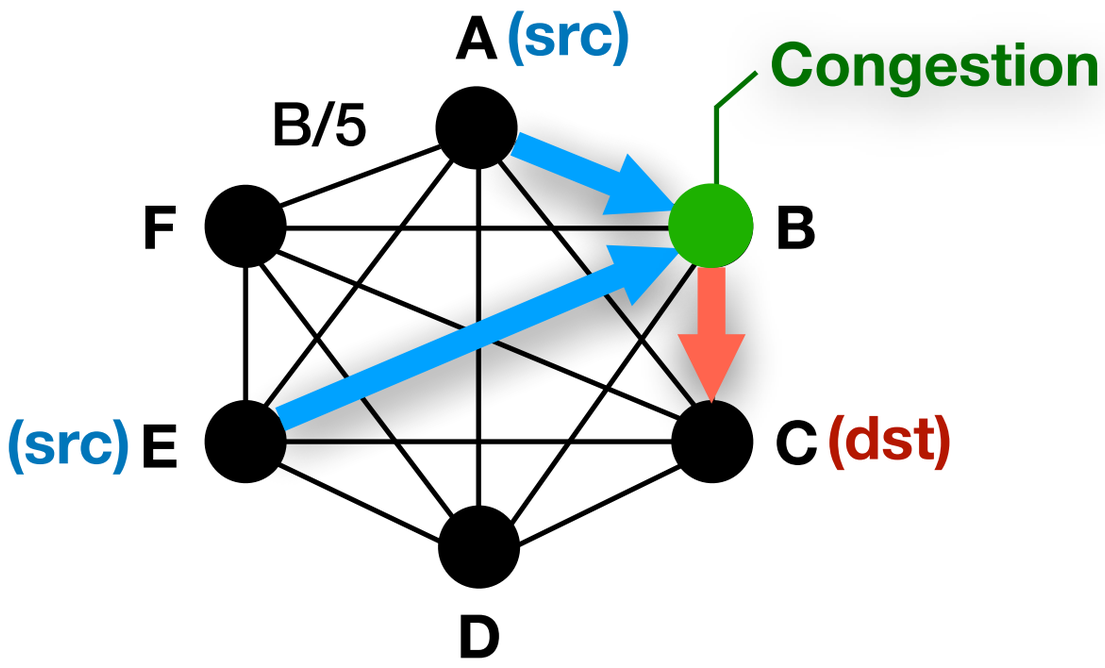
Routing & Congestion Control



Valiant Load Balancing



Bounded worst-case throughput of 50% compared to an ideal packet-switched network



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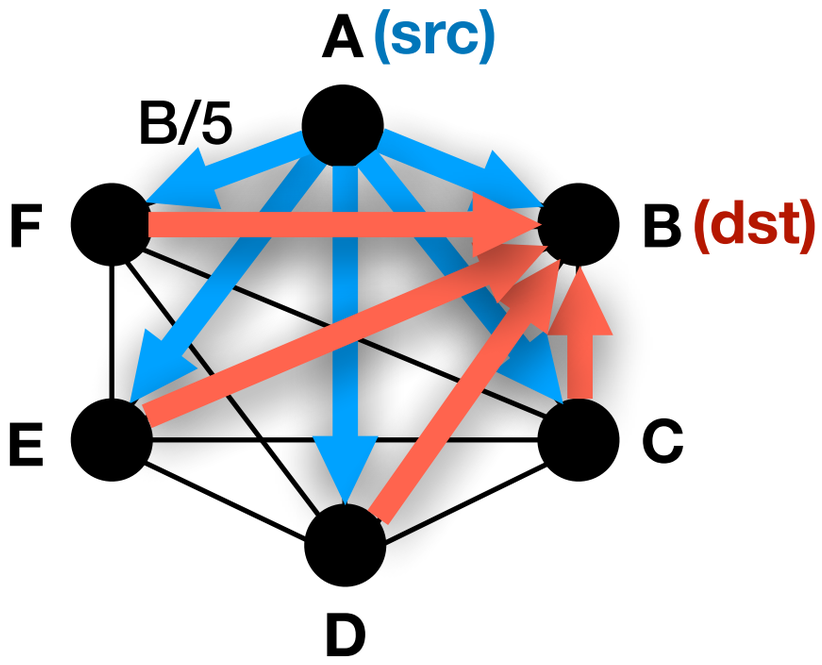

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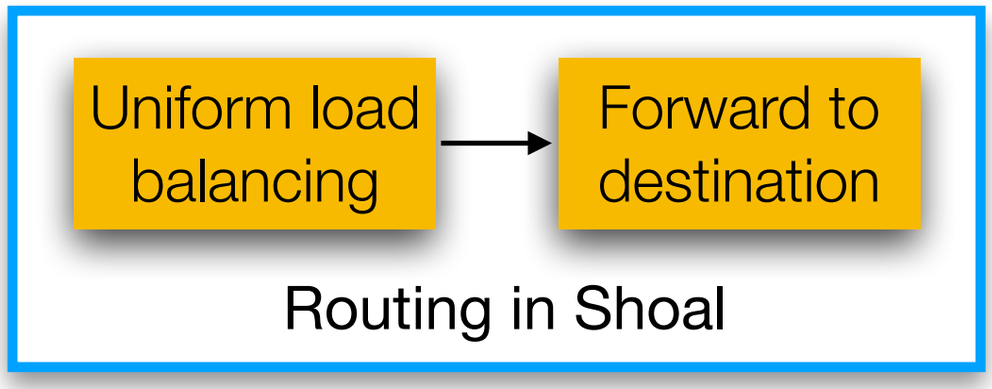

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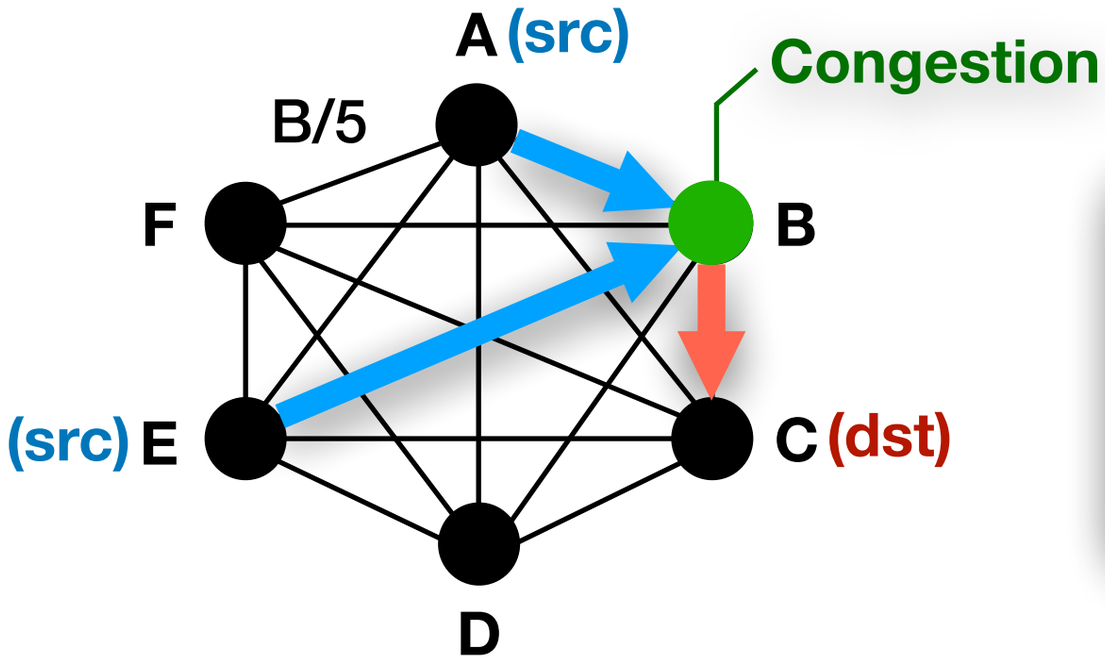

Congestion Control

Each per-destination queue Q_i for each destination i is bounded!

$len(Q_i) \leq 1 + incast\_degree(i)$ **packets**

Key Properties of Shoal

- Fast, de-centralized, and traffic-agnostic **circuit scheduling**
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Implementation

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Stratix V FPGA

- Circuit Switch
  - re-configures in < 6.4ns
- End-host NIC
  - fully pipelined design

FPGA code for the implementation of Shoal is available at:
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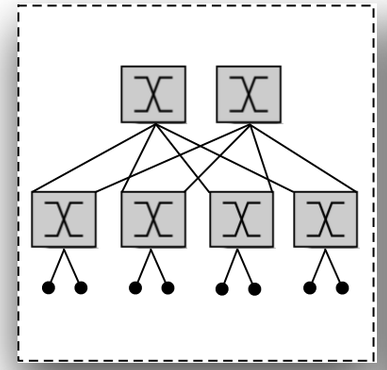

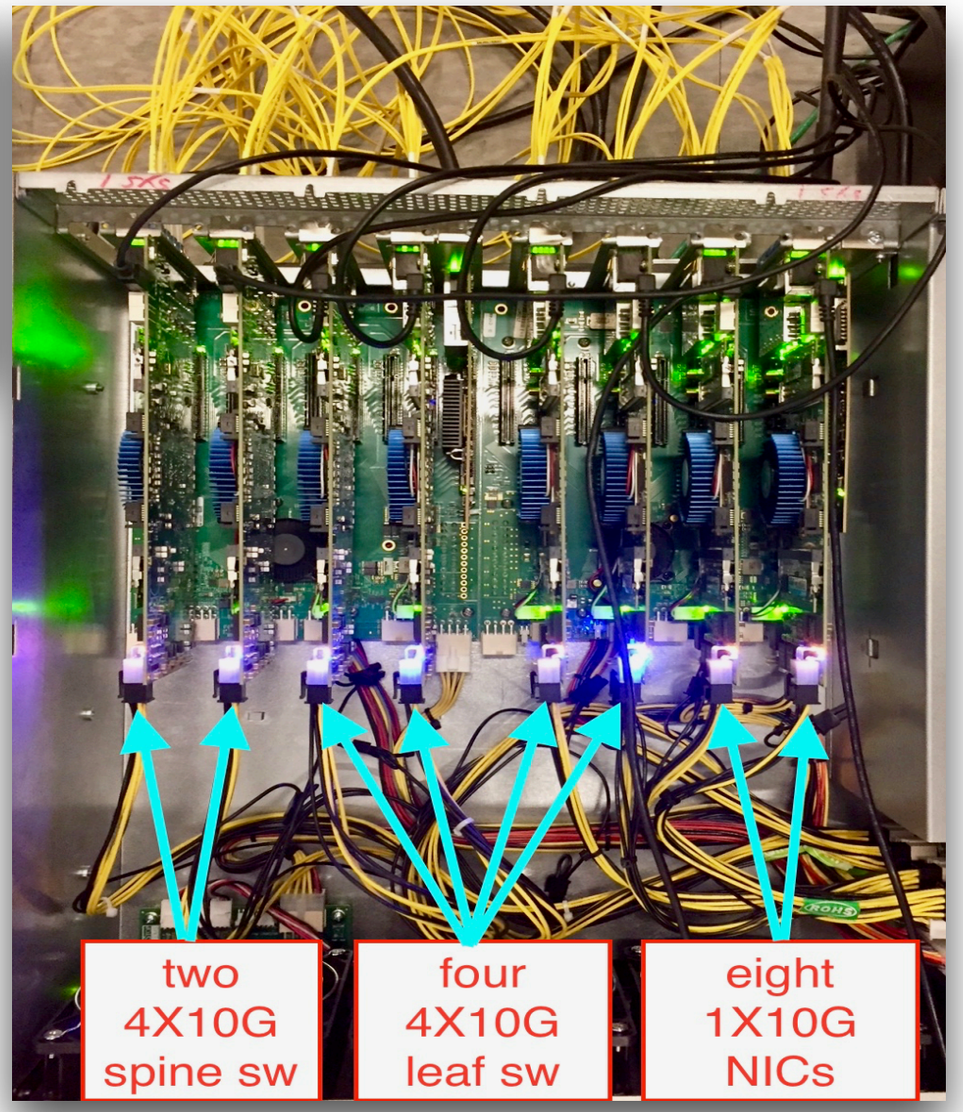

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- Packet-level simulator in C
- 512 end-hosts
- Shoal has 2x bandwidth
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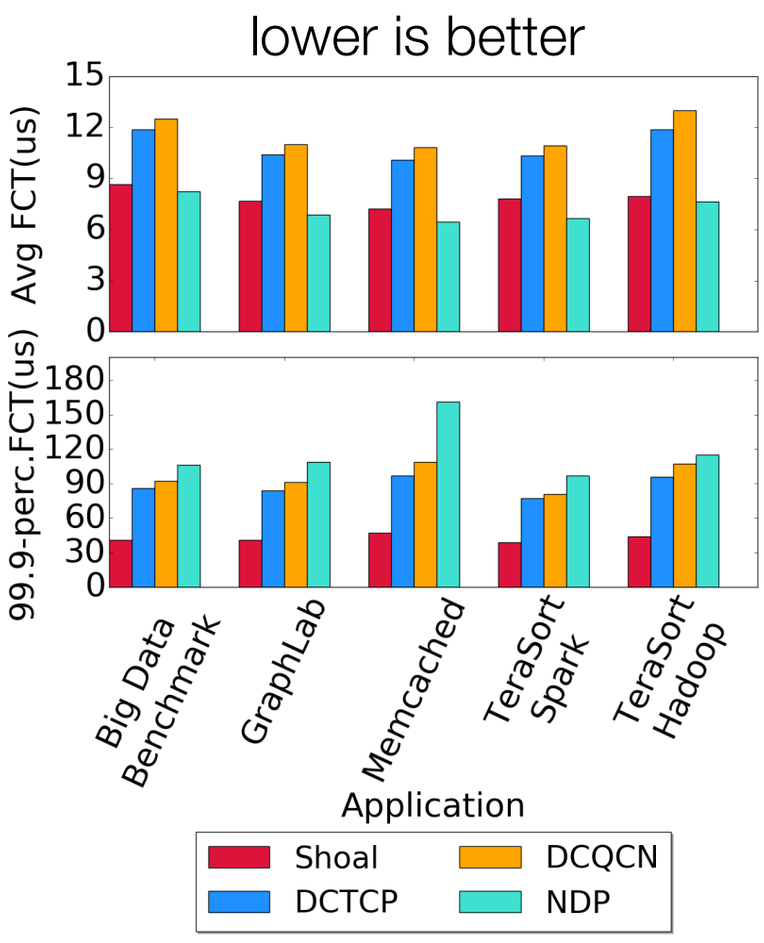
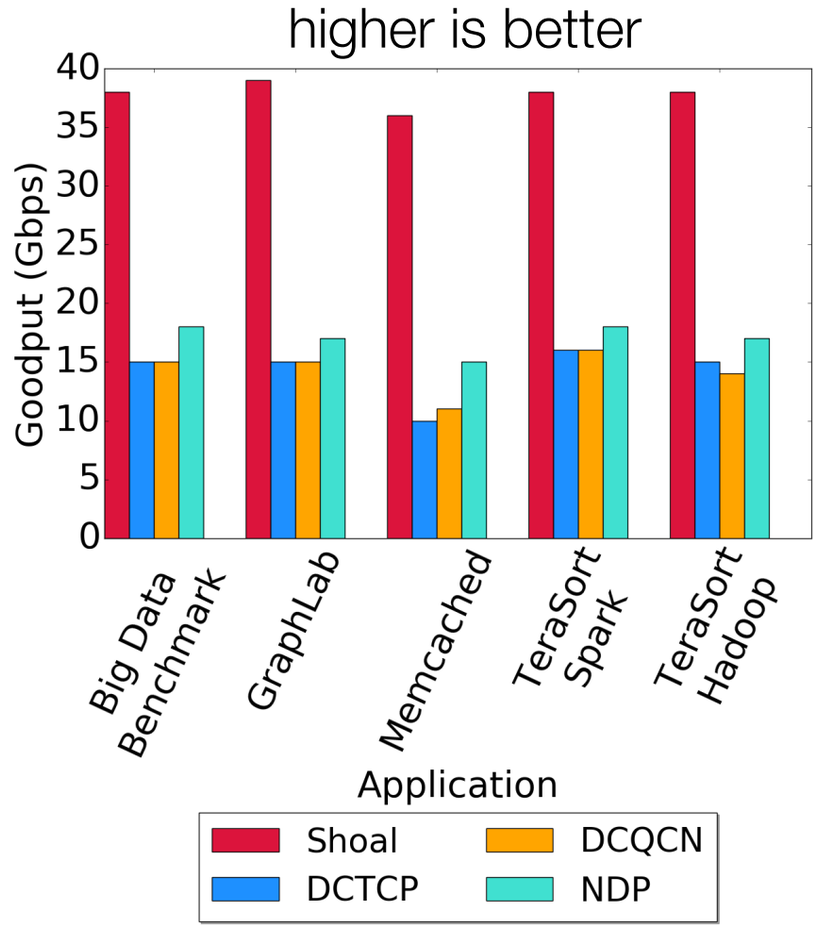


Short Flows (<100KB)



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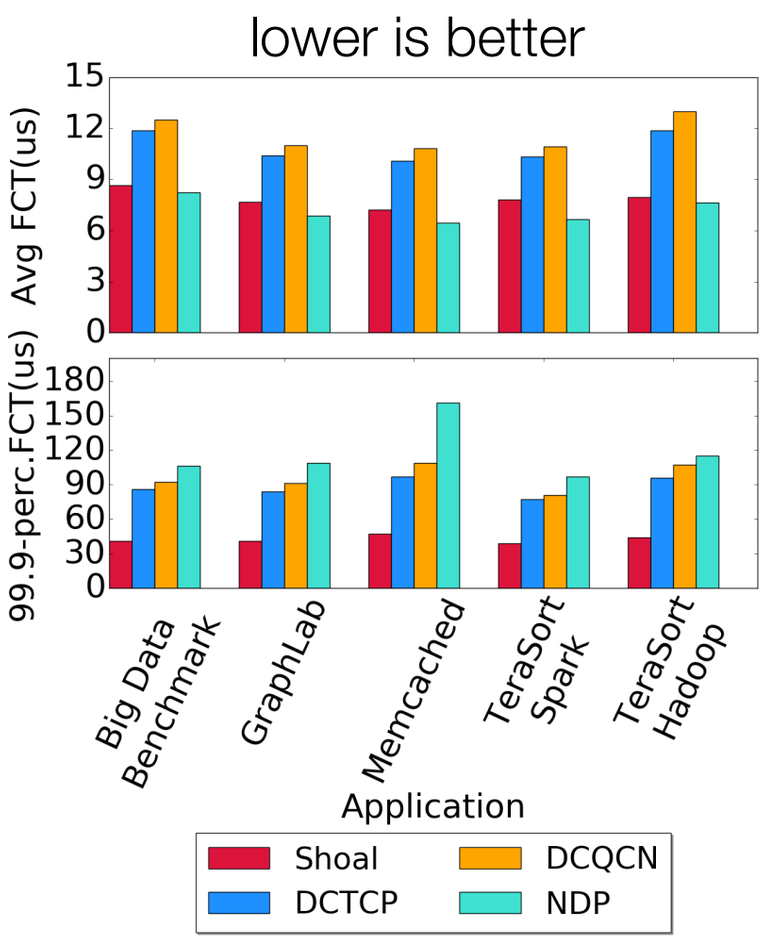

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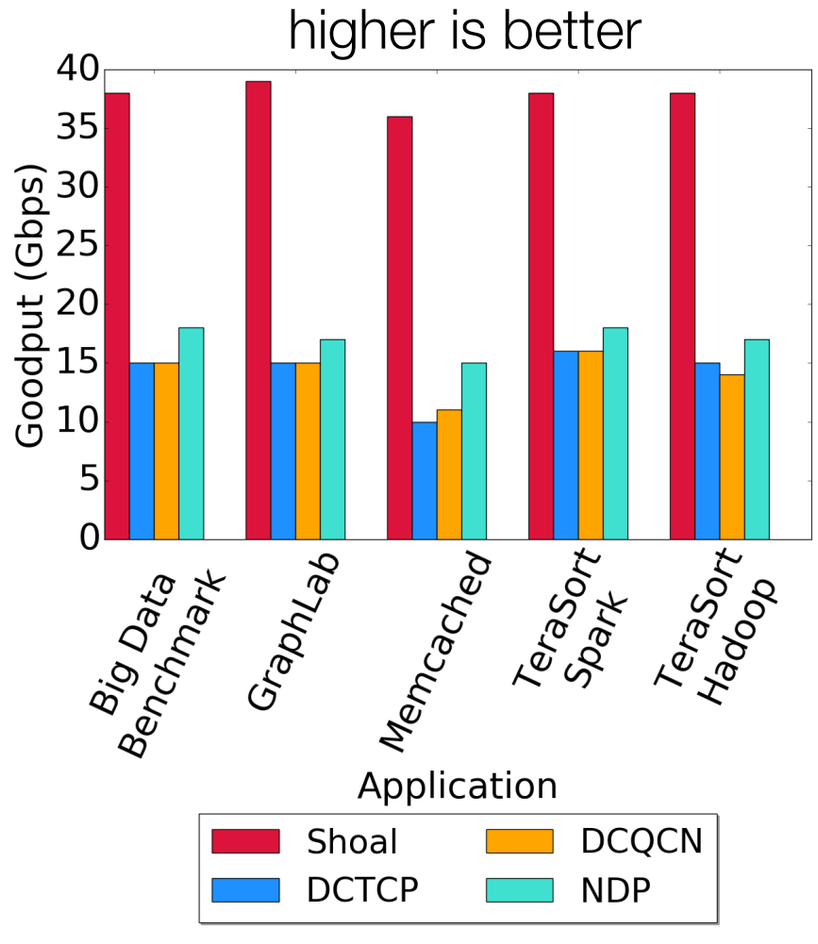
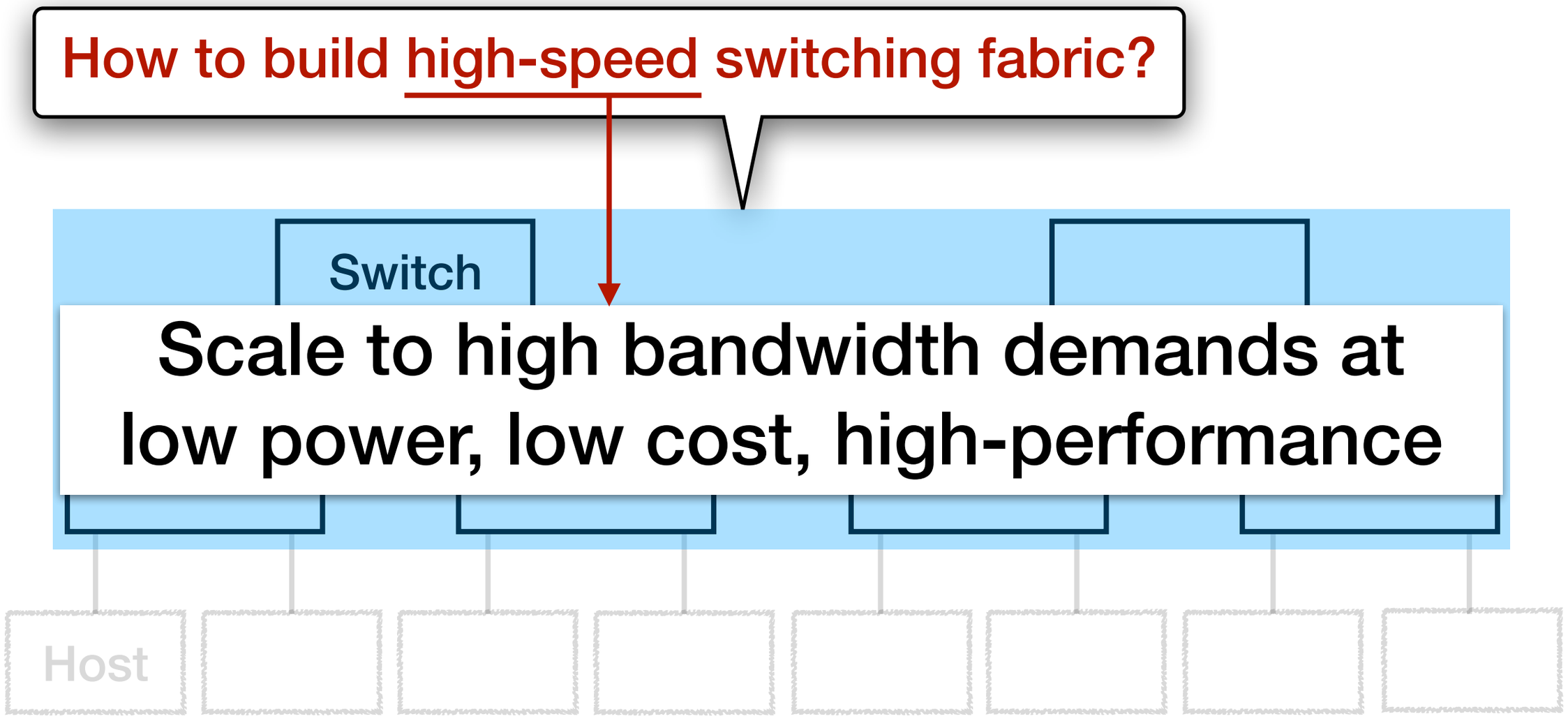


Long Flows (>1MB)

Shoal performs comparable or better than several recent packet-switched network designs

Part II : Summary



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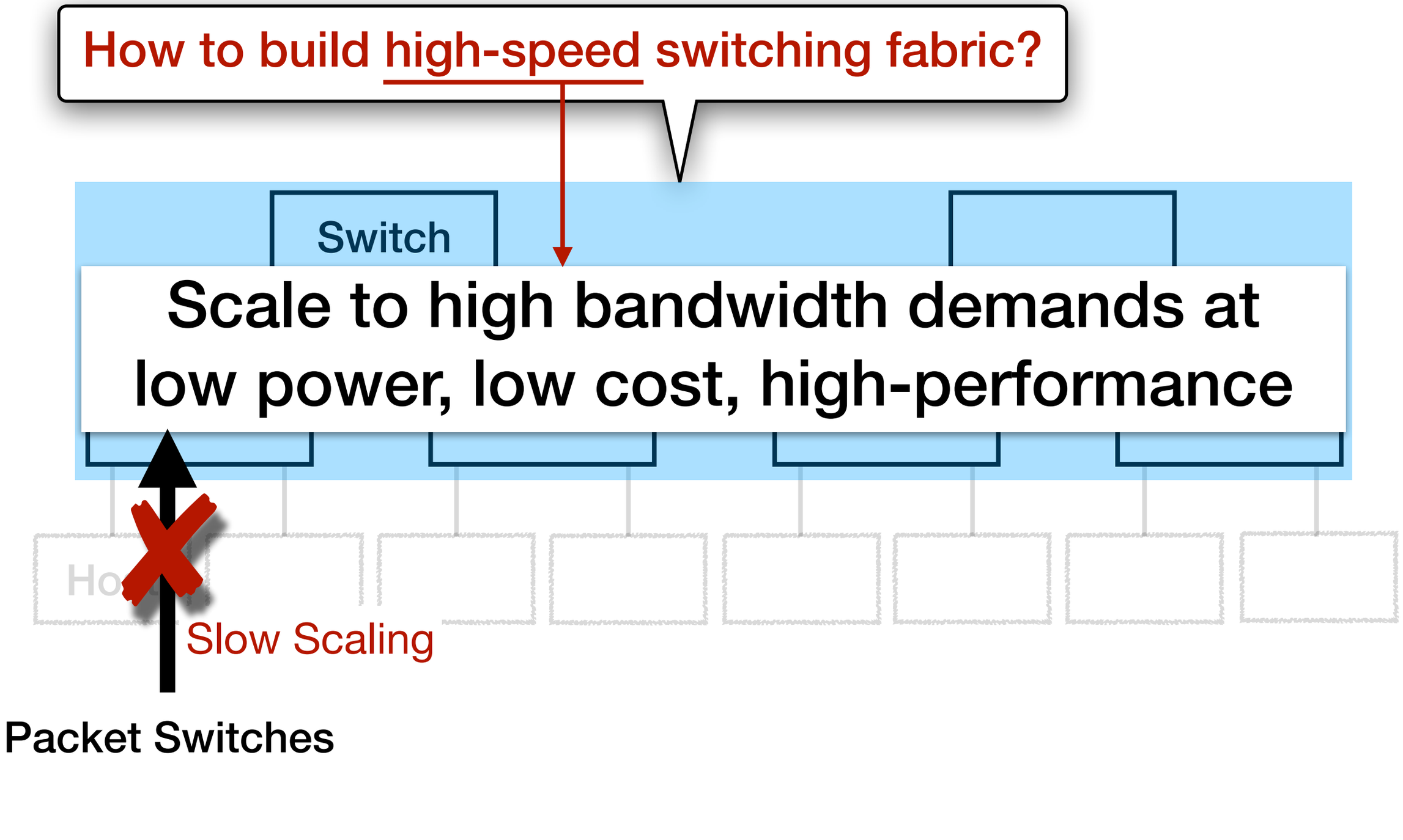

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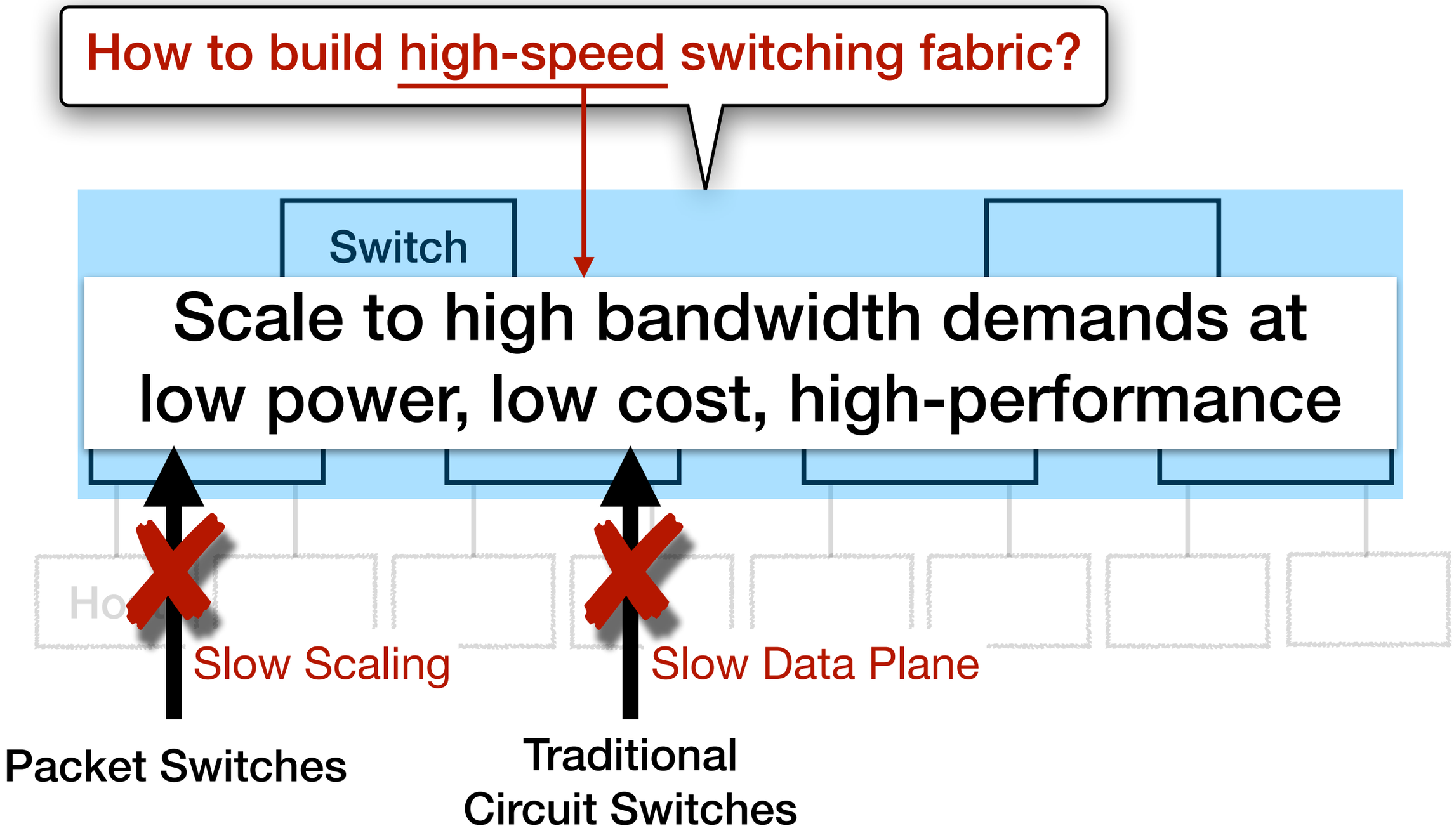

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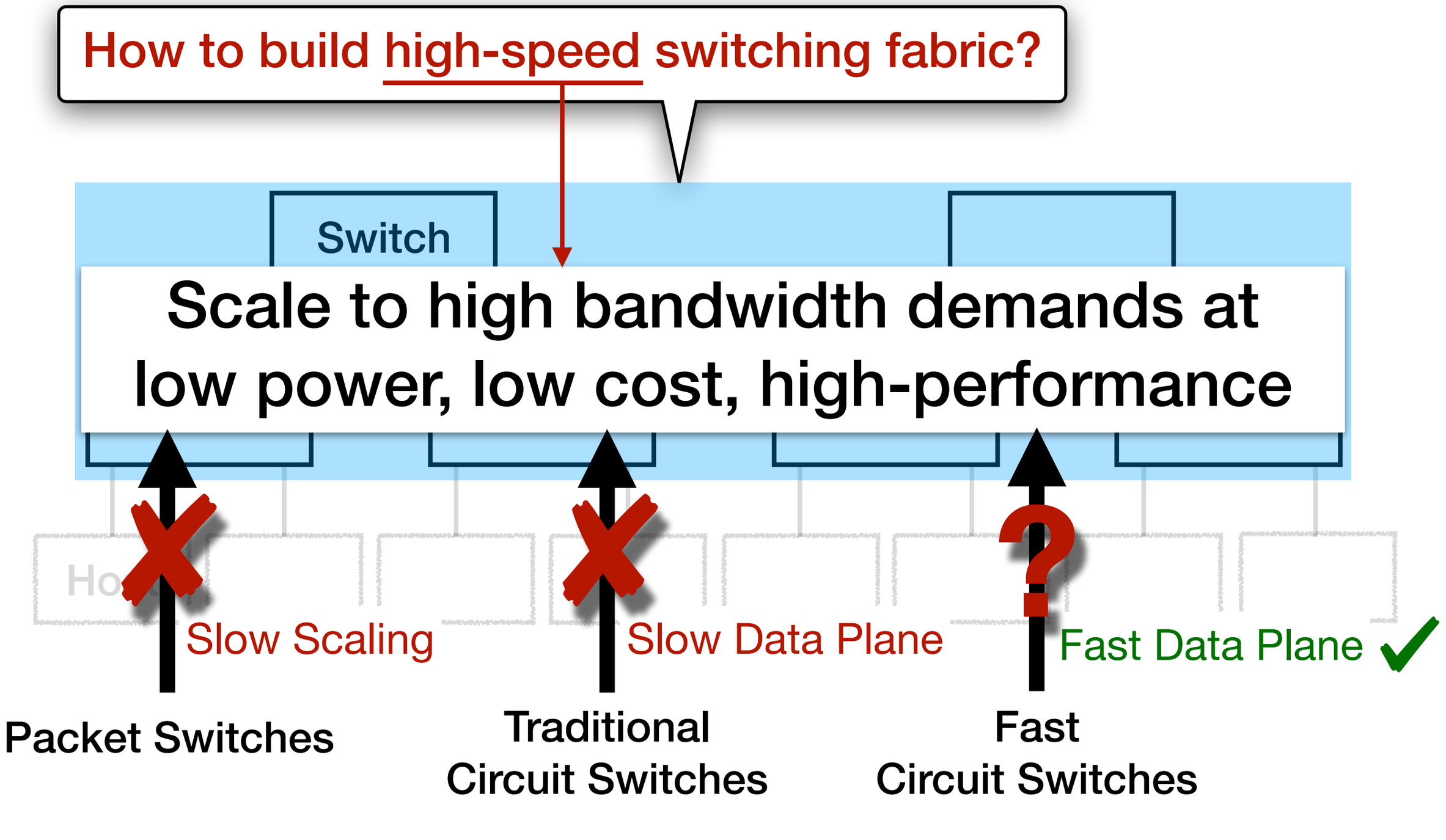

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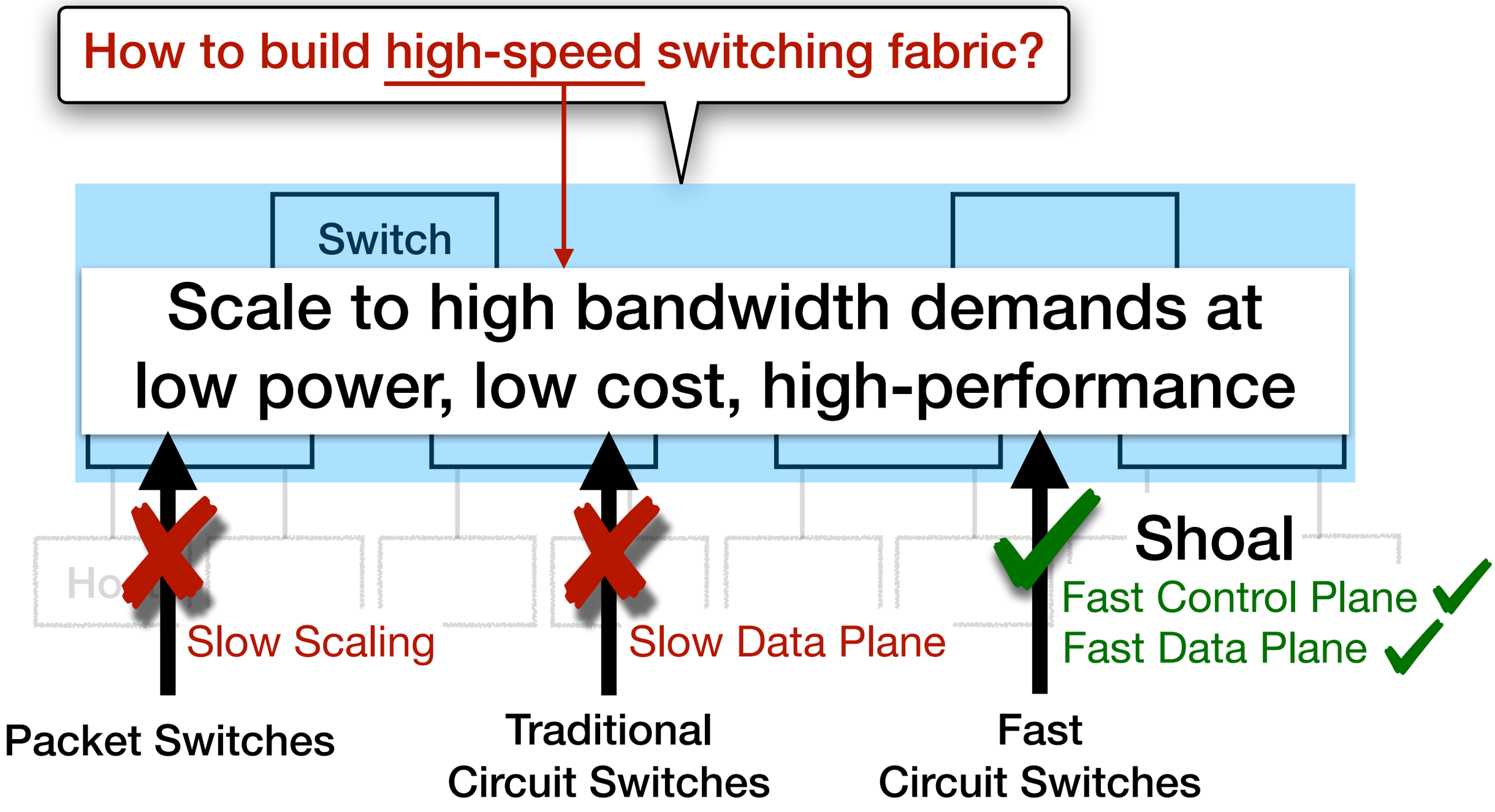

Future Directions

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High-speed and Programmable Processors for (stateful) Network Functions

e.g., load balancers, firewalls, deep packet inspectors

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Low latency Optical Circuit Switching

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Networking Infrastructure Speed

end-host

General-purpose Processor

switching fabric

Packet Switch

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How to build high-speed networking infrastructure in the Post-Moore era?

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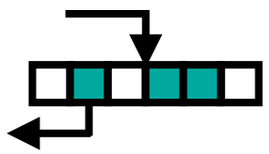
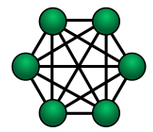
PIEO  Programmable and high-performance domain-specific processor for packet scheduling	**Contributions**	**Shoal**  High-performance, ns-granularity control plane for circuit switching

Thank you!