SIGCOMM 2022
Amsterdam

Artifacts Available V1.1
Artifacts Evaluated Functional V1.1
Results Reproduced V1.1

Stateful Multi-Pipelined Programmable Switches

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Motivating Example

Consider a packet processing program:

- Switch maintains packet counters for each destination IP
- If the counter value for destination d exceeds a threshold
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$\Big\downarrow$ **Code**

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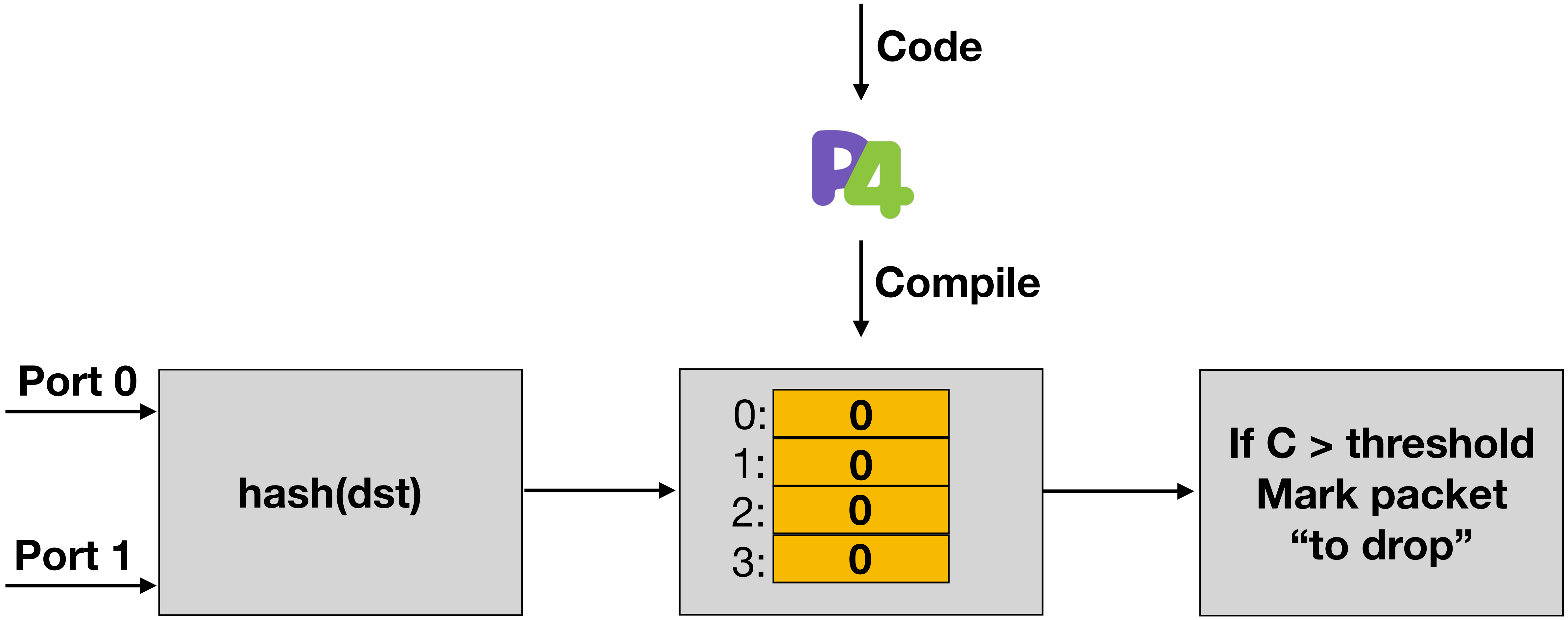

Switch Pipeline

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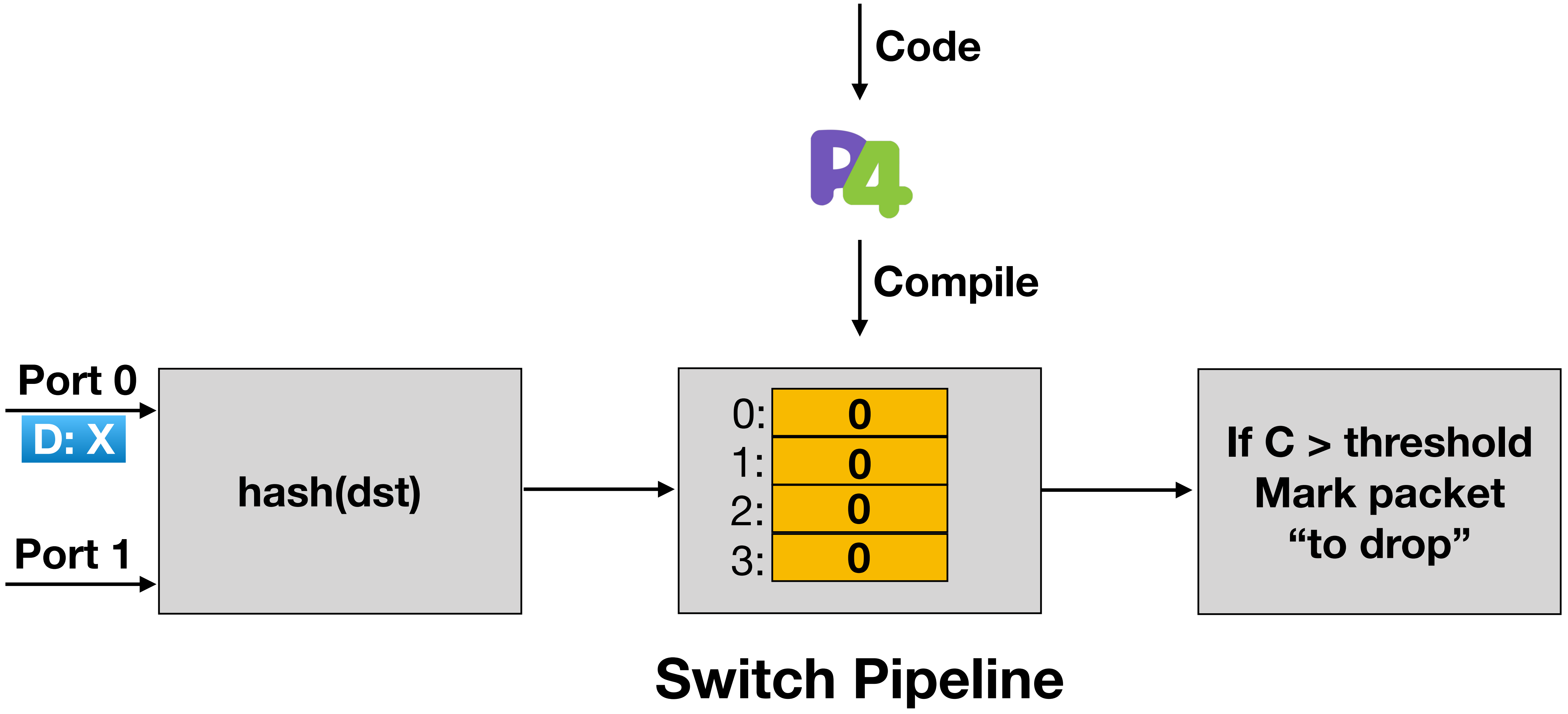

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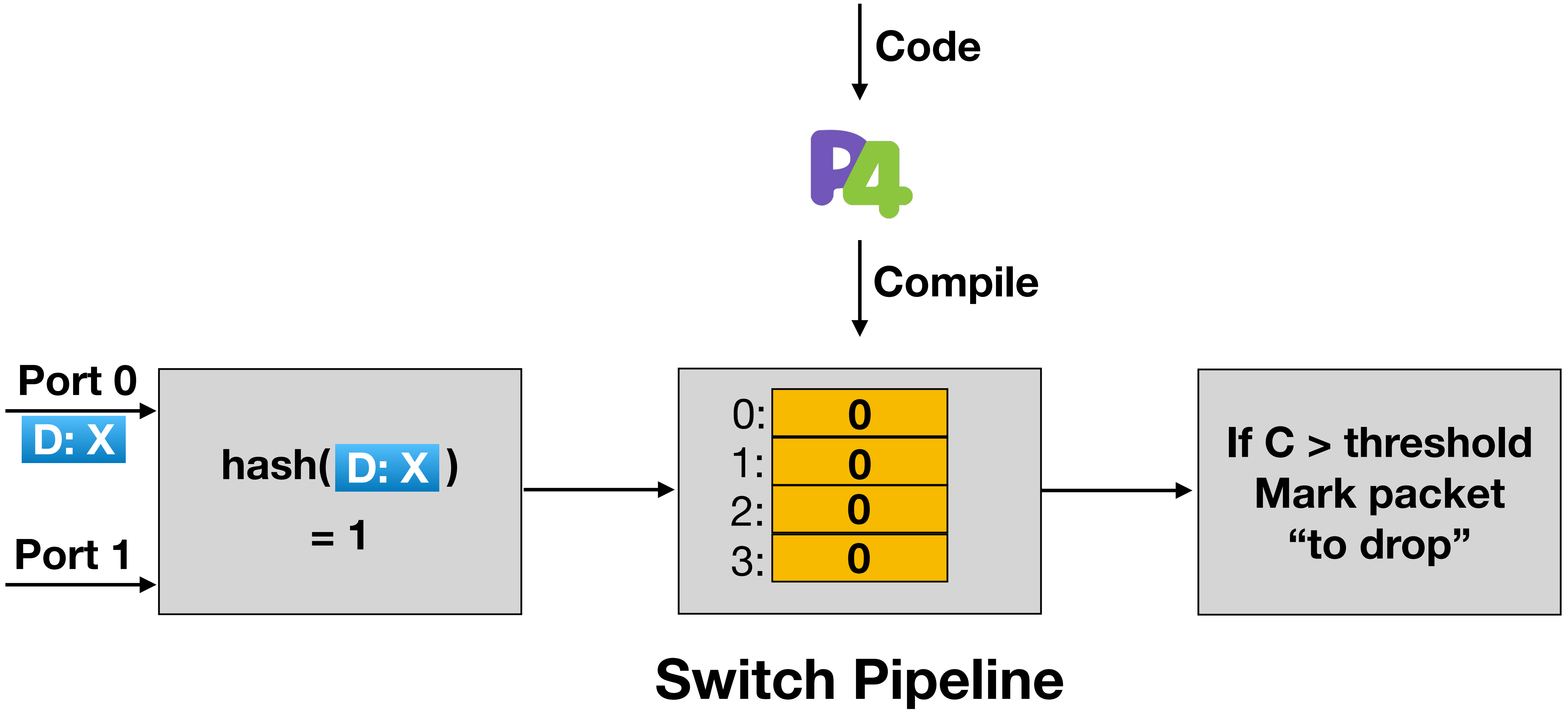

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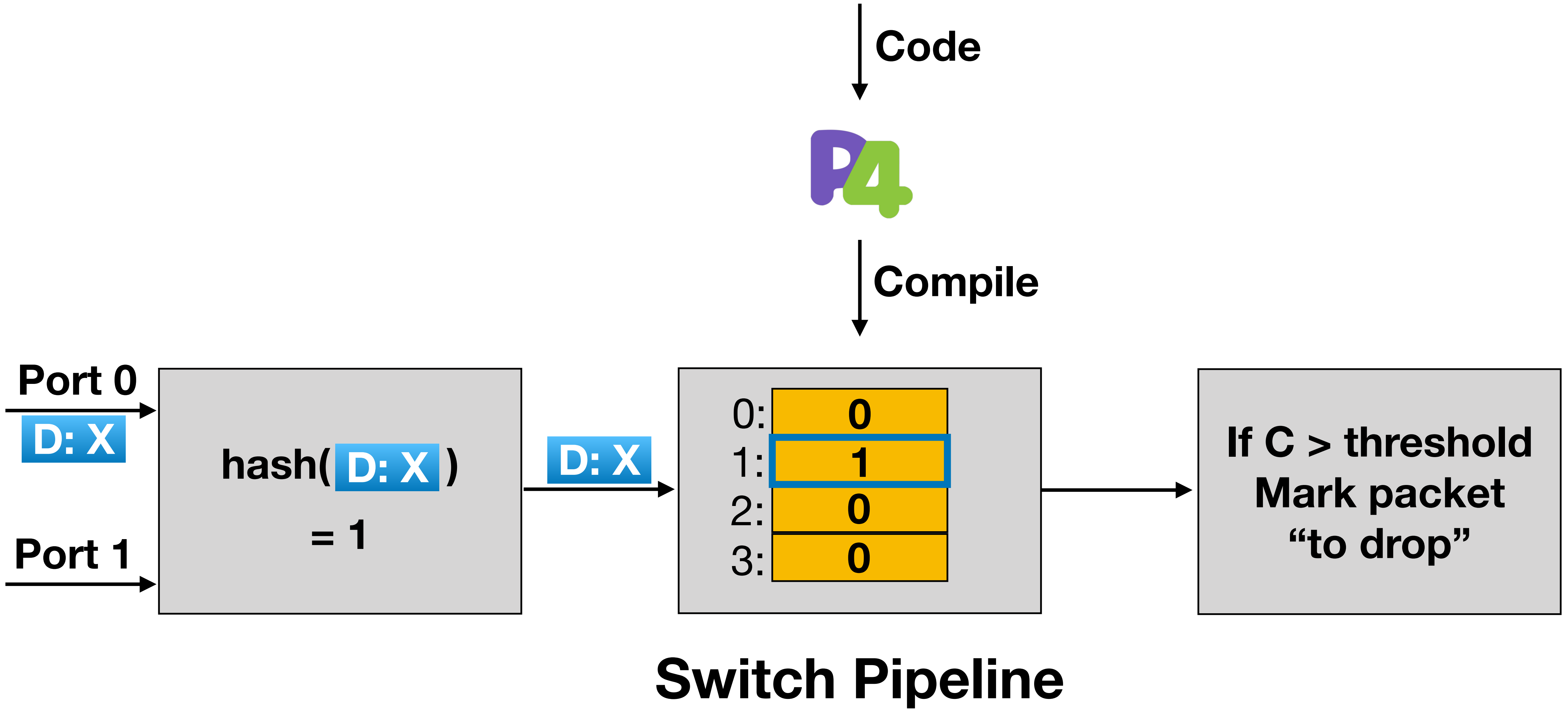

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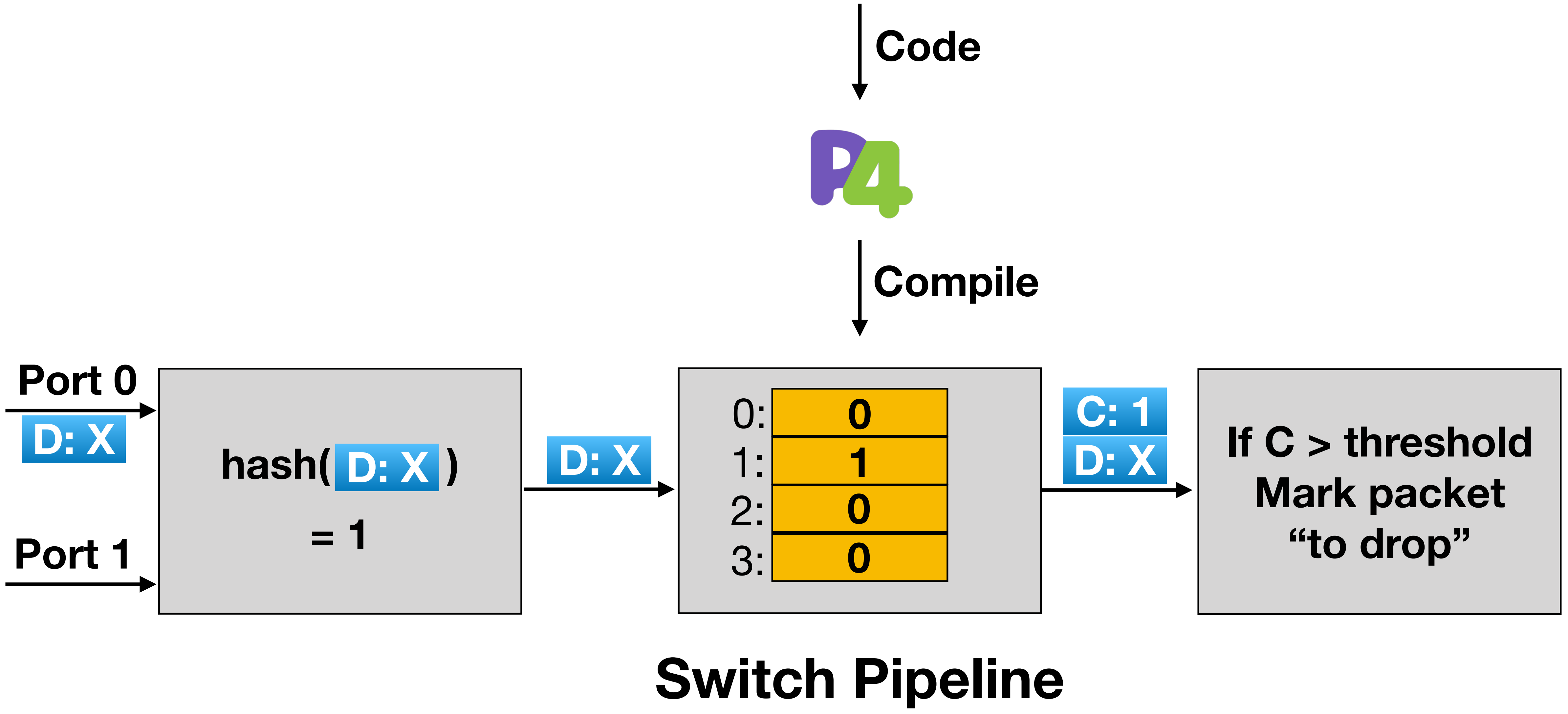
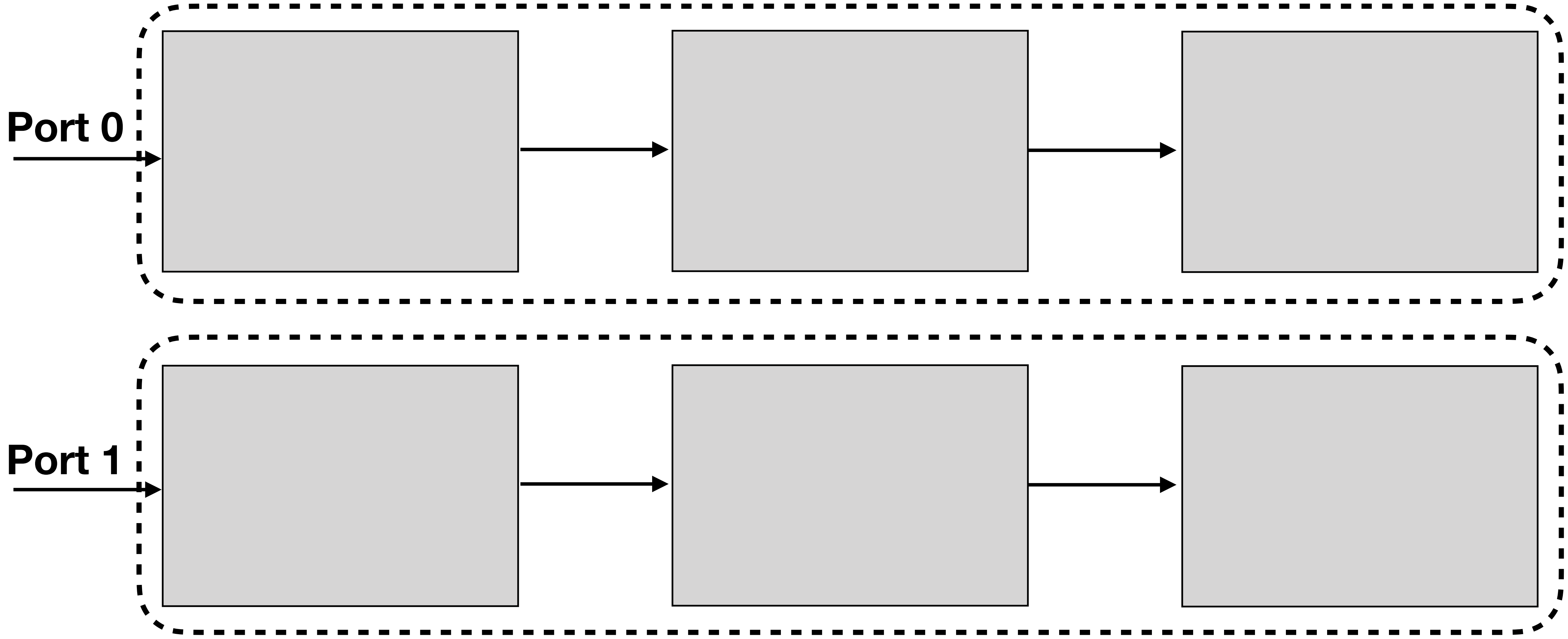
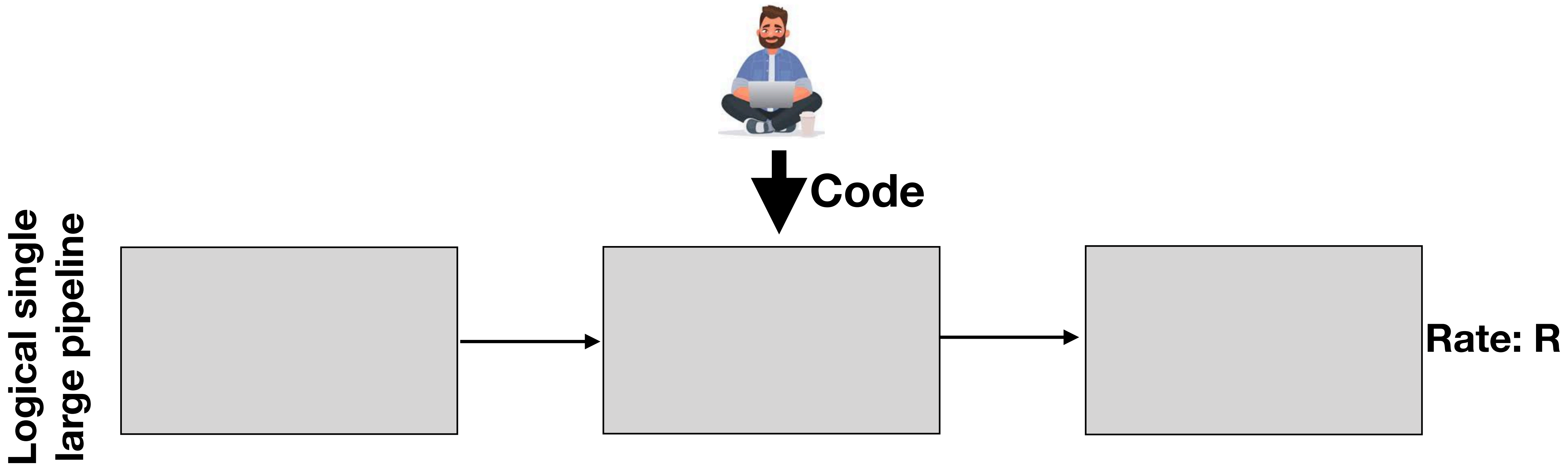


Reality of Today's Switch Hardware

- Clock speed of a single pipeline has saturated
  - Limits the line rate
- Employ multiple **parallel pipelines** to sustain multi-tbps line rate
  - Each pipeline processes packets **independently** — No co-ordination



Goal



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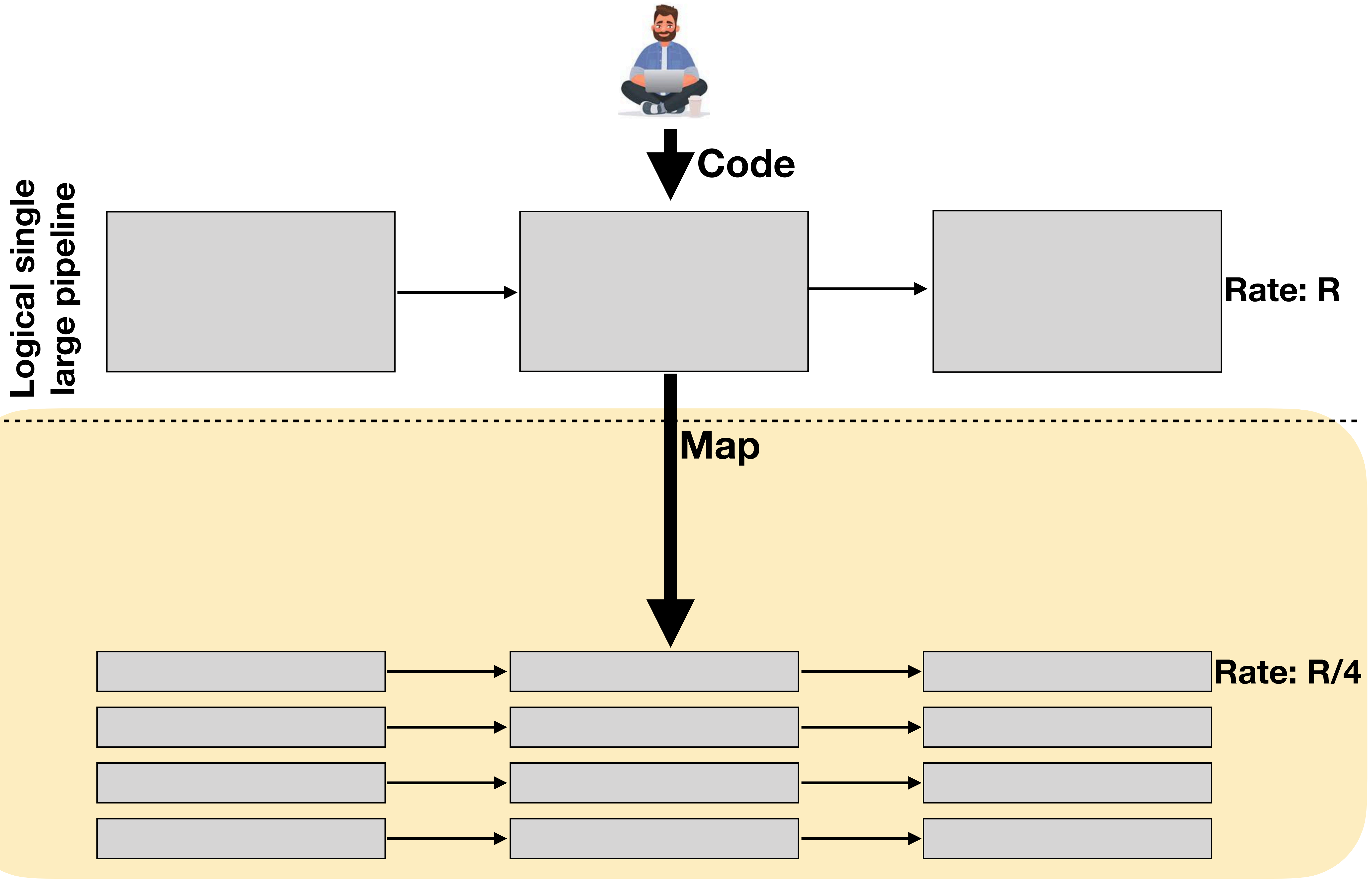

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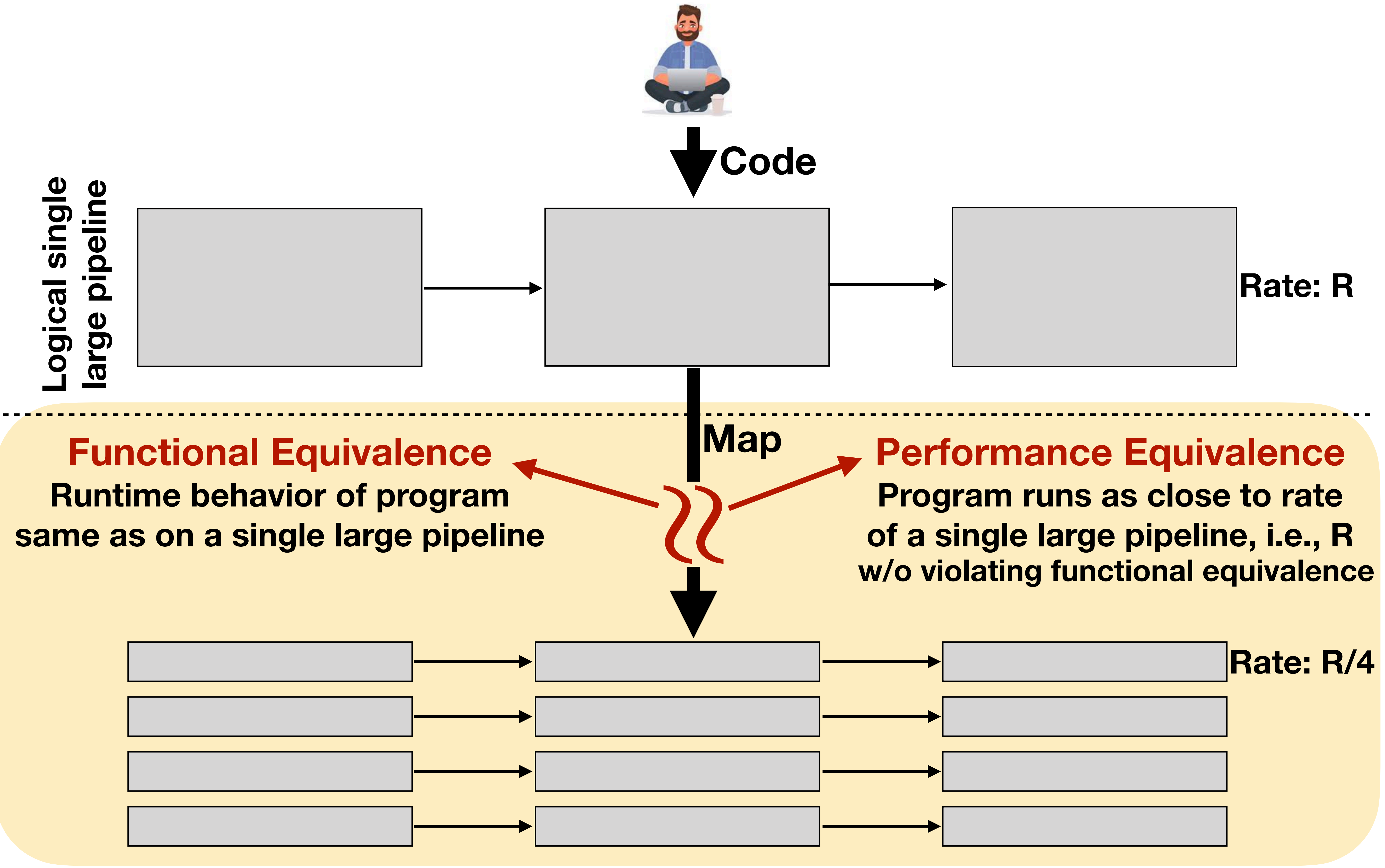

Code
Logical single large pipeline
Rate: R
Map
Functional Equivalence
Runtime behavior of program same as on a single large pipeline
Performance Equivalence
Program runs as close to rate of a single large pipeline, i.e., R w/o violating functional equivalence
Rate: R/4

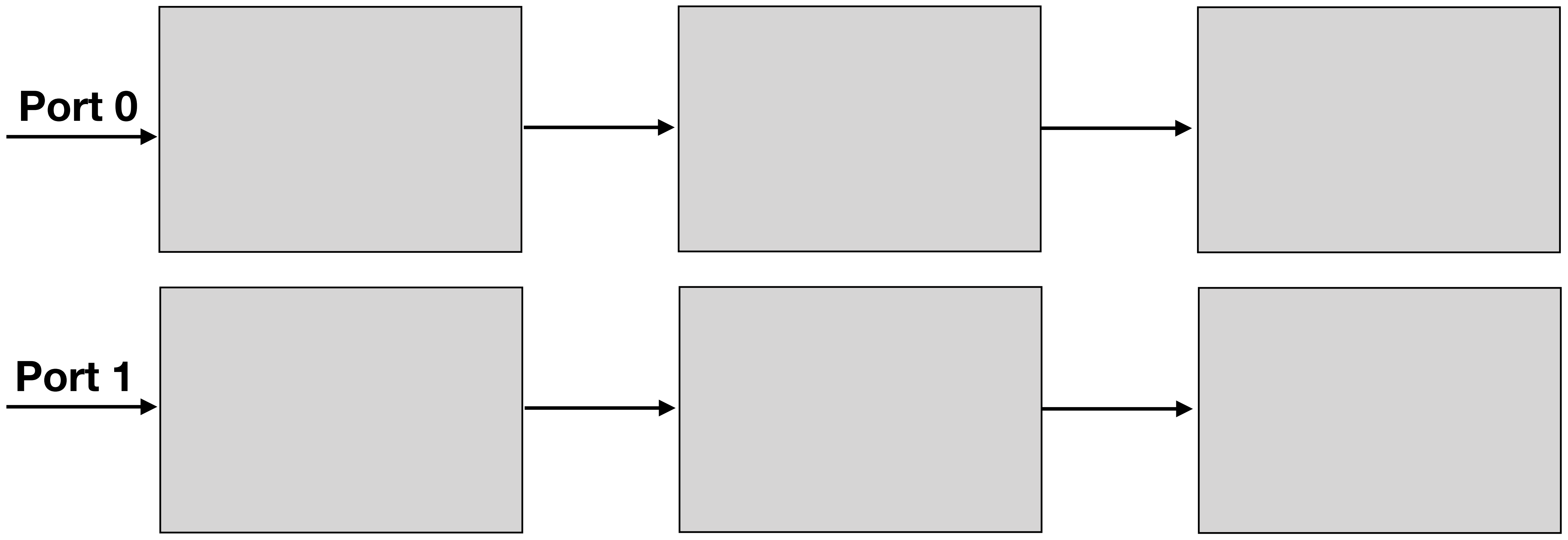
Our Contribution

We present a new switch design **MP5** that extends current programmable switch's **architecture, compiler,** and **runtime** to guarantee **functional equivalence** with **high performance**

Naive Approaches

Consider a *stateless* packet processing program:

- Switch increments the ttl value in packet header by 1
- If ttl value exceeds a threshold
    - Switch drops the packet



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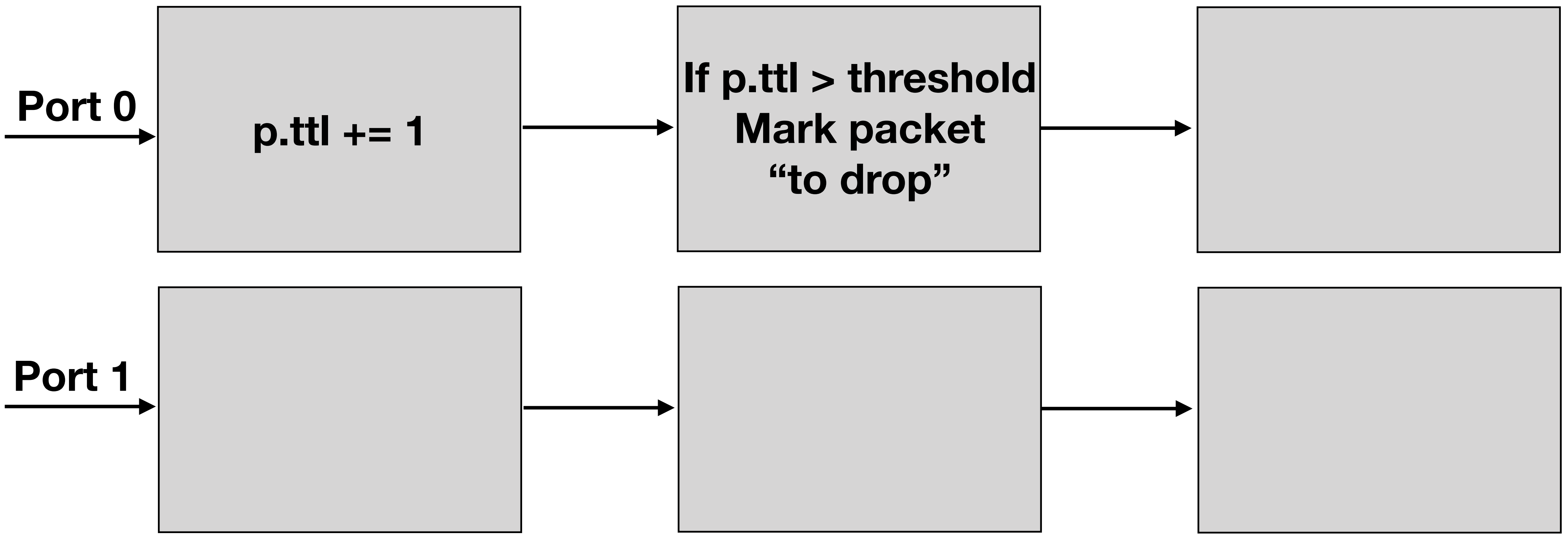

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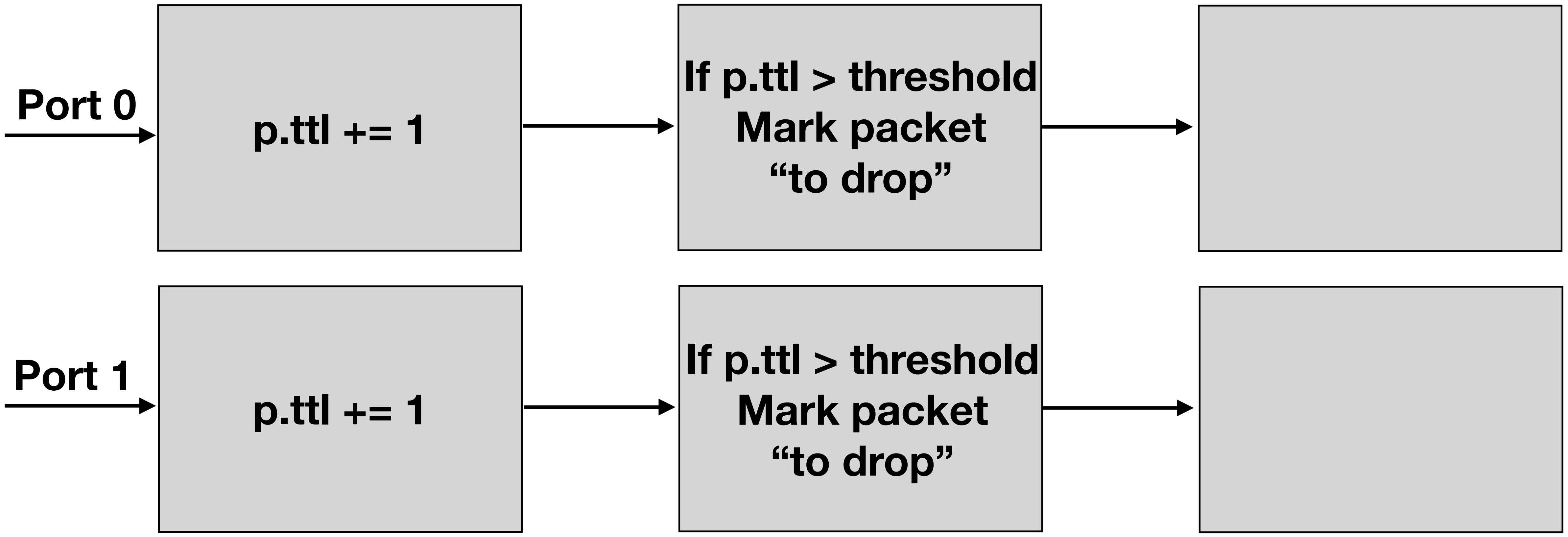
Try 1: Replicate stateless processing on all pipelines


Port 0
p.ttl += 1
If p.ttl > threshold Mark packet "to drop"
Port 1
p.ttl += 1
If p.ttl > threshold Mark packet "to drop"

Goals and Techniques

Techniques	Functional Equivalence		Performance	
	Stateless	Stateful	Stateless	Stateful
Replicate stateless processing	✓		✓	

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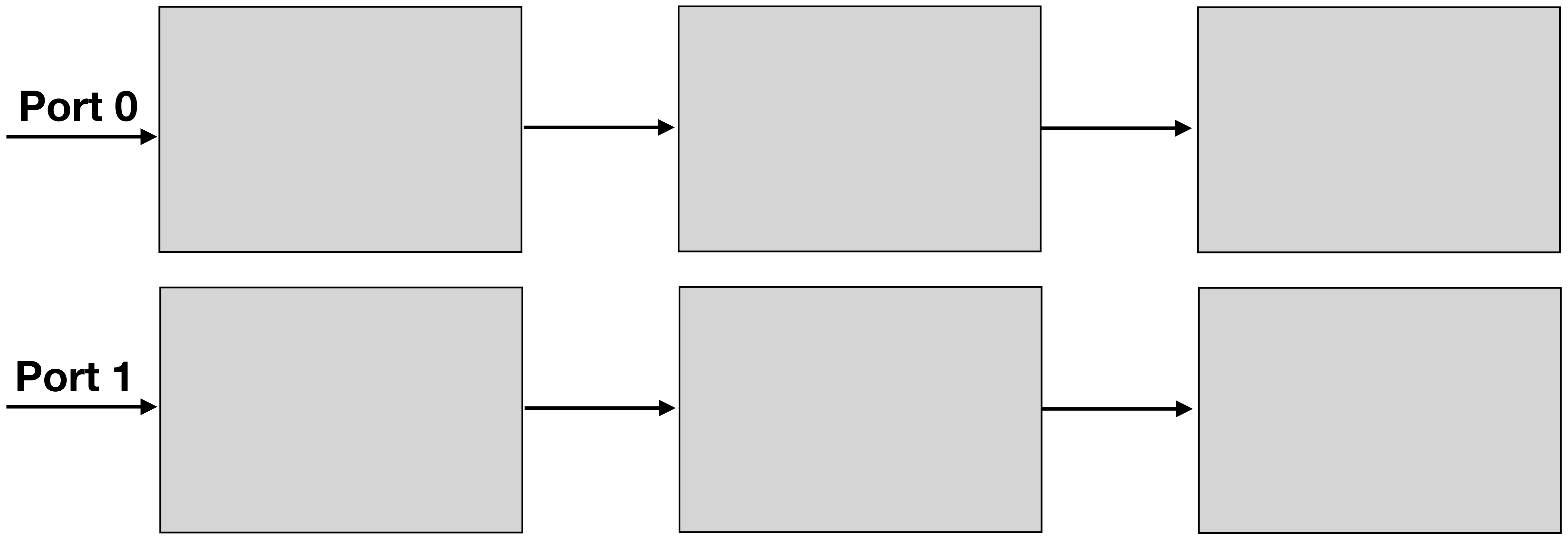

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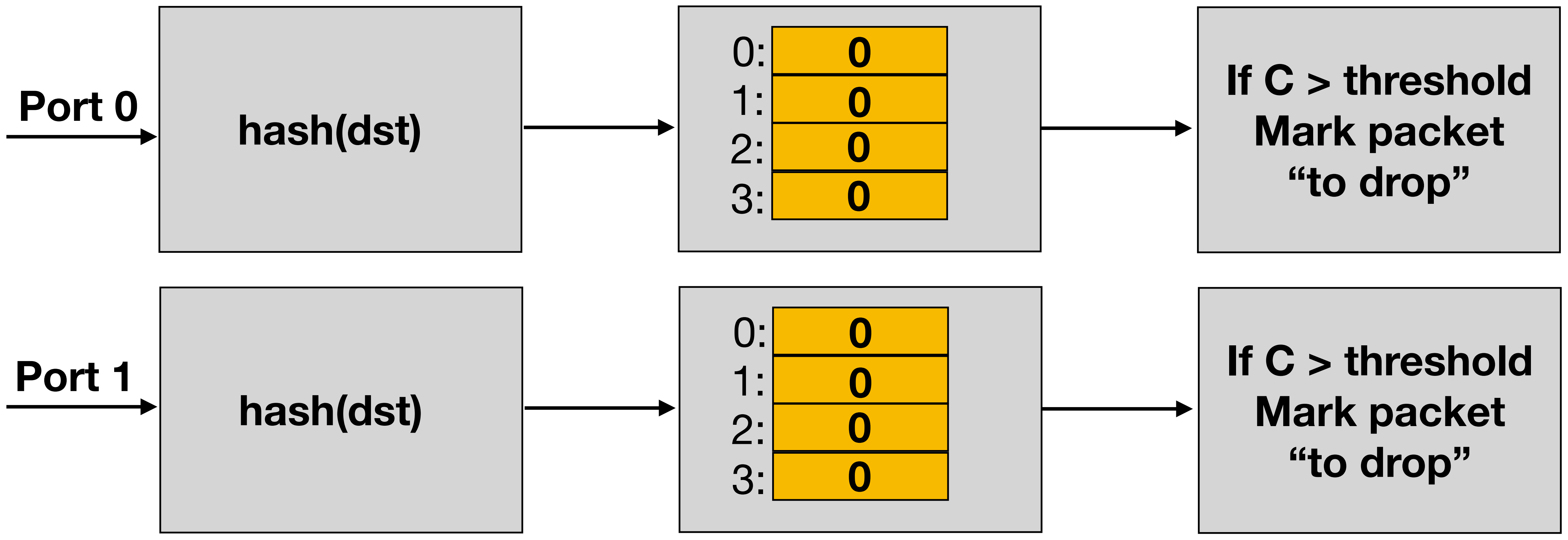

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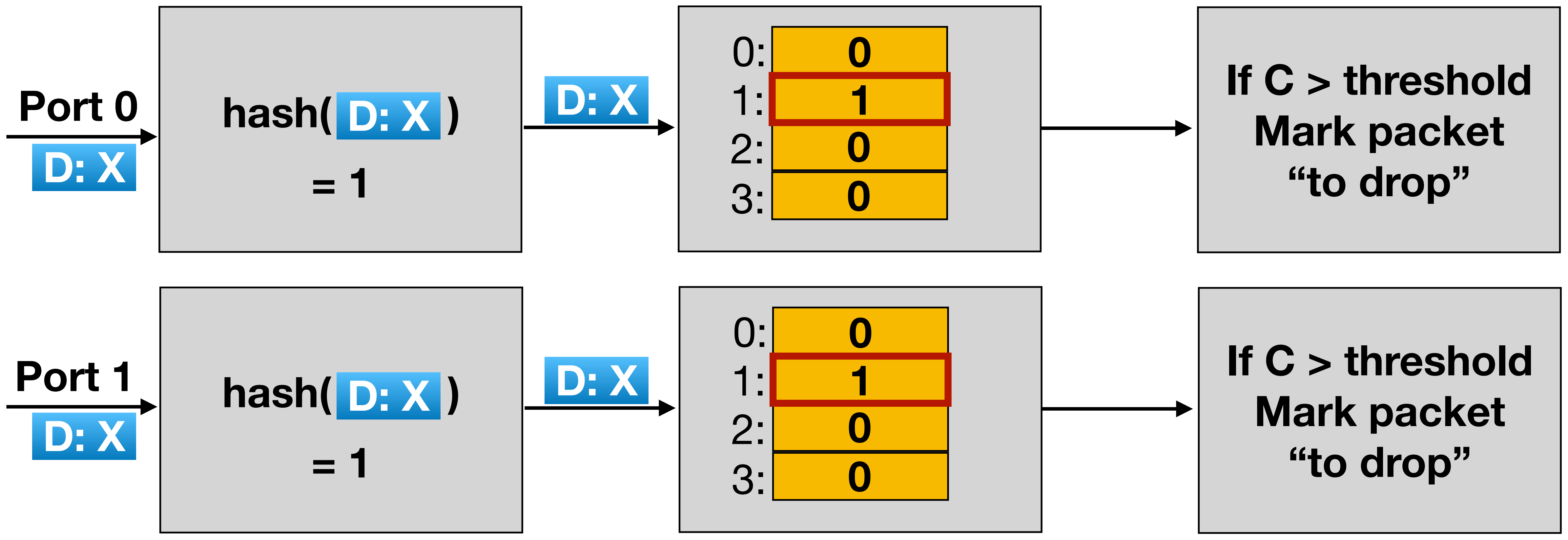
Violates functional equivalence!



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Consider a *stateful* packet processing program:

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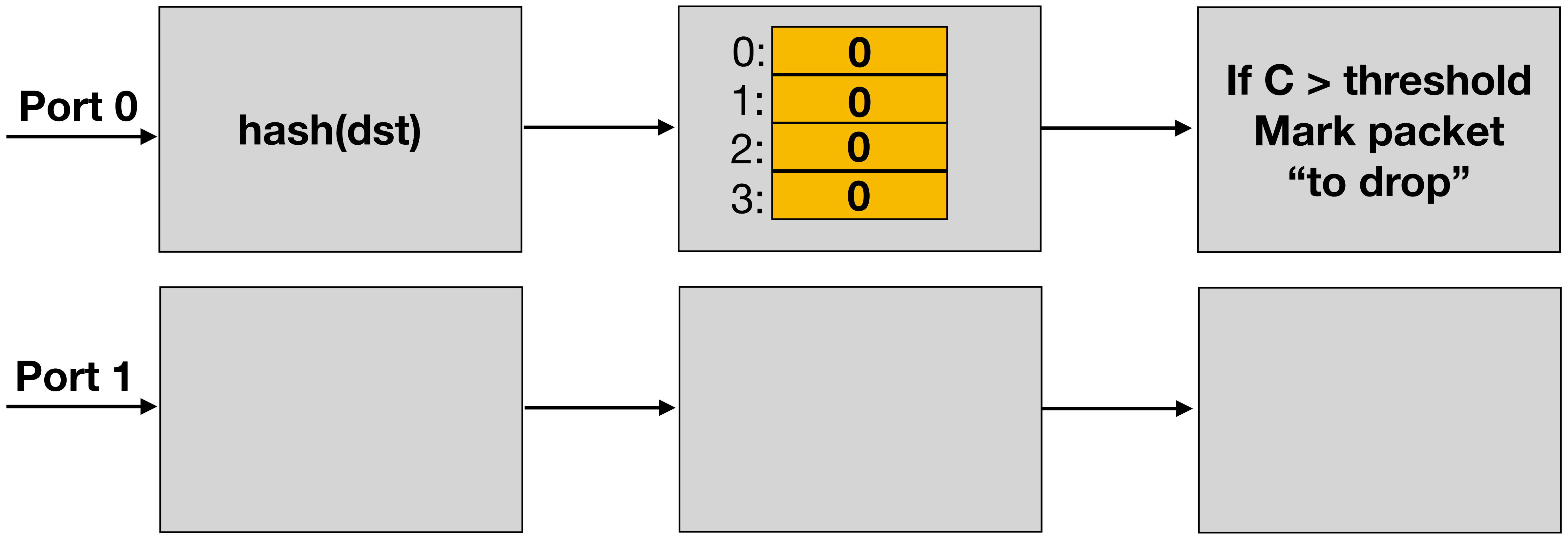
Try 2: Limit stateful processing to a single "shared" pipeline



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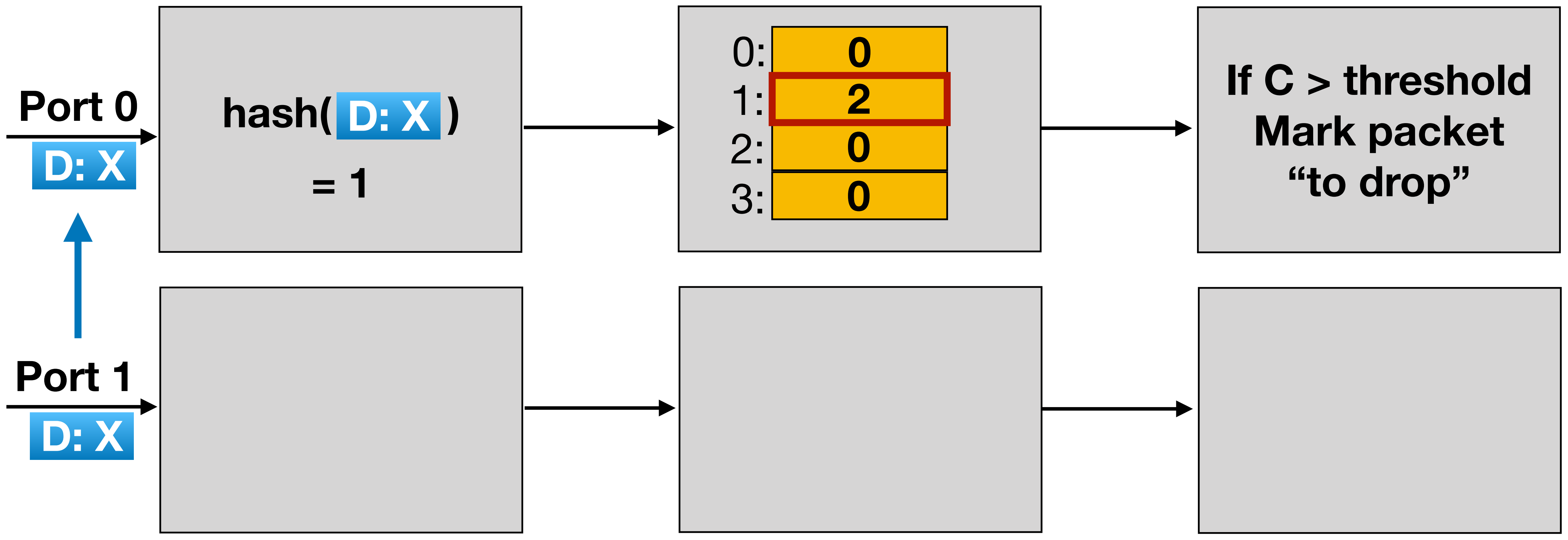

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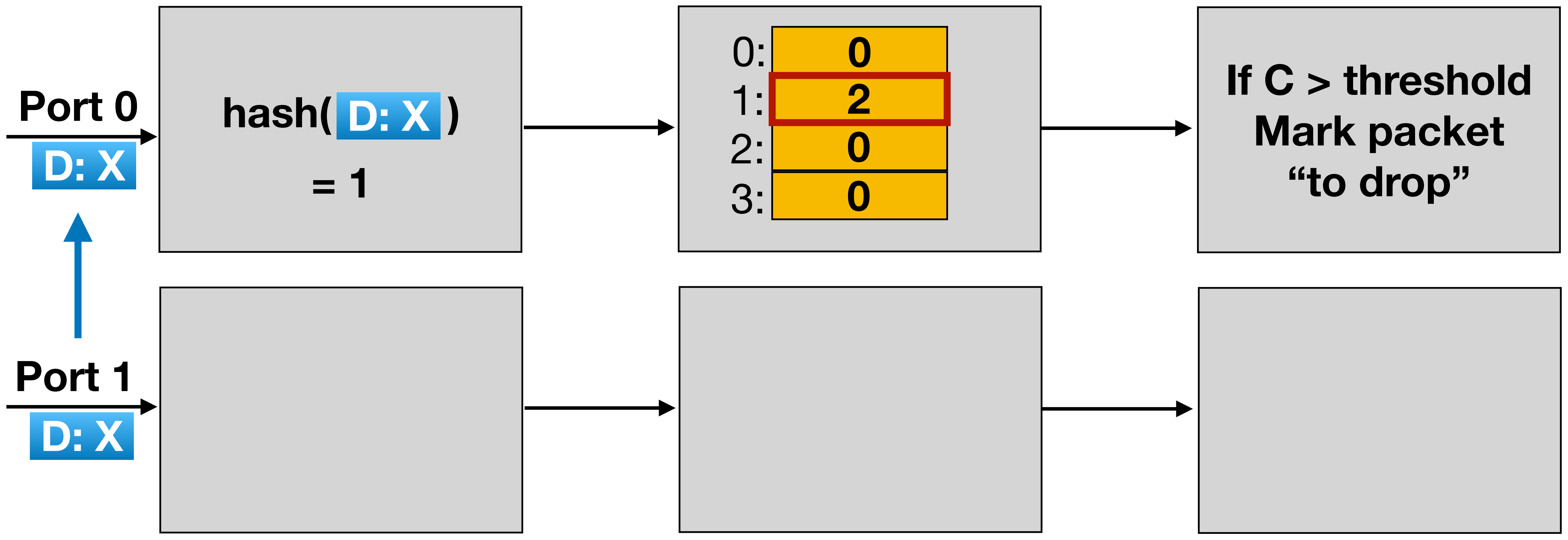
Limits speed of stateful processing!



Goals and Techniques

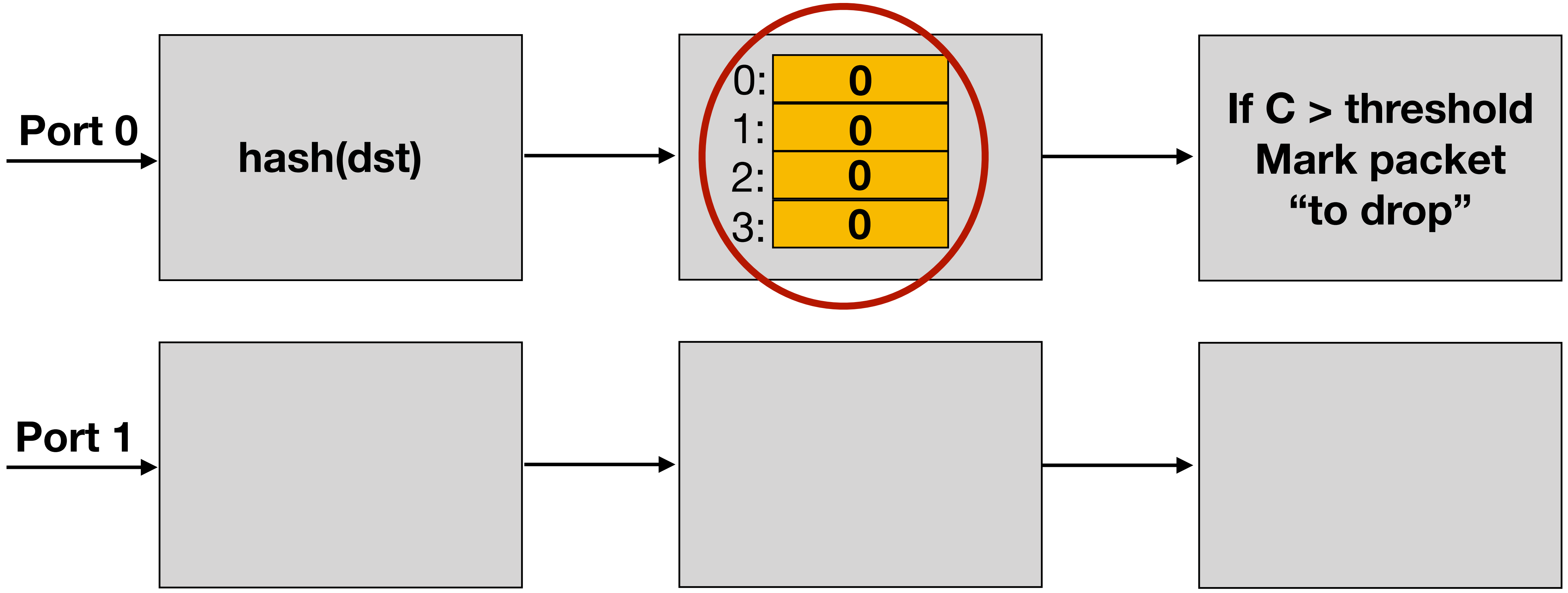
Techniques	Functional Equivalence		Performance	
	Stateless	Stateful	Stateless	Stateful
Replicate stateless processing	✓		✓	
+ Limit stateful processing to single pipeline	✓	✓	✓	✗

Question

How to improve performance?
(without violating functional equivalence)

Problem

How to store shared state that enables high packet processing throughput?



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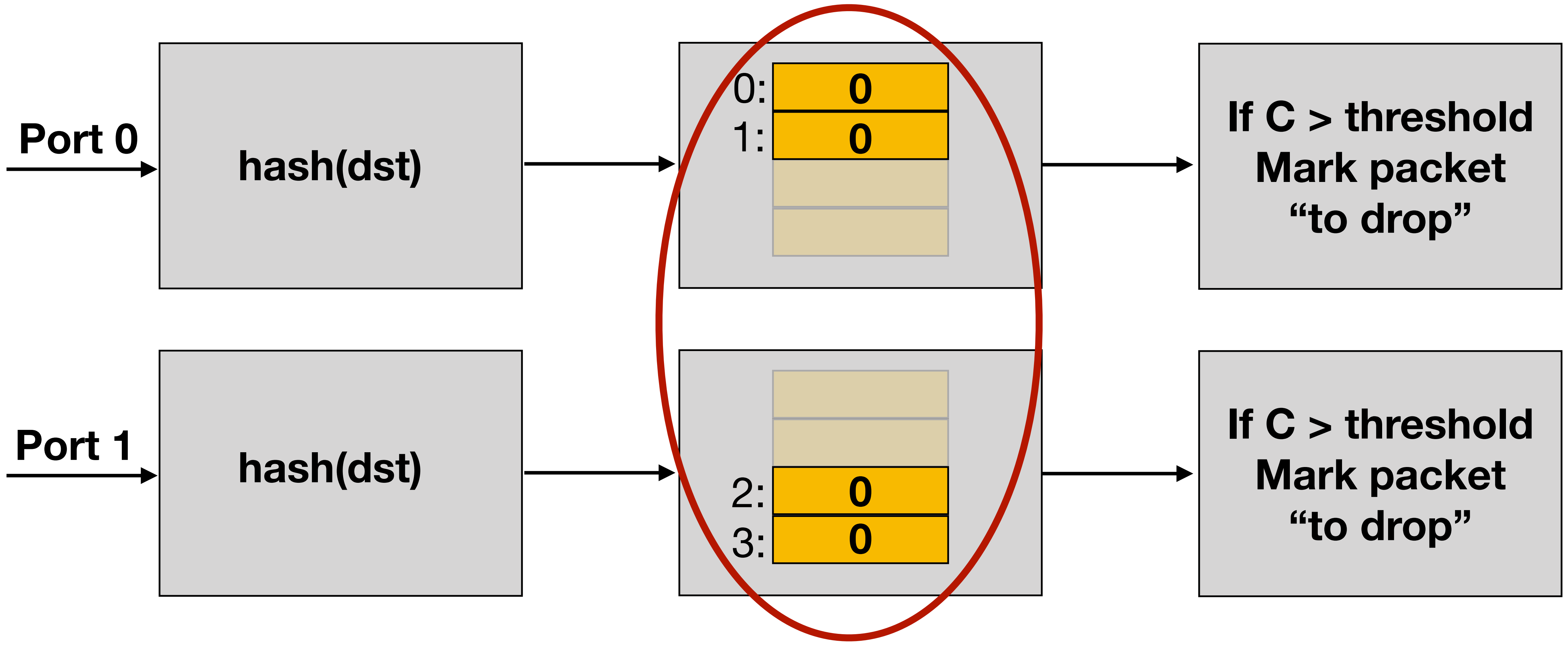

Shard the shared state across pipelines

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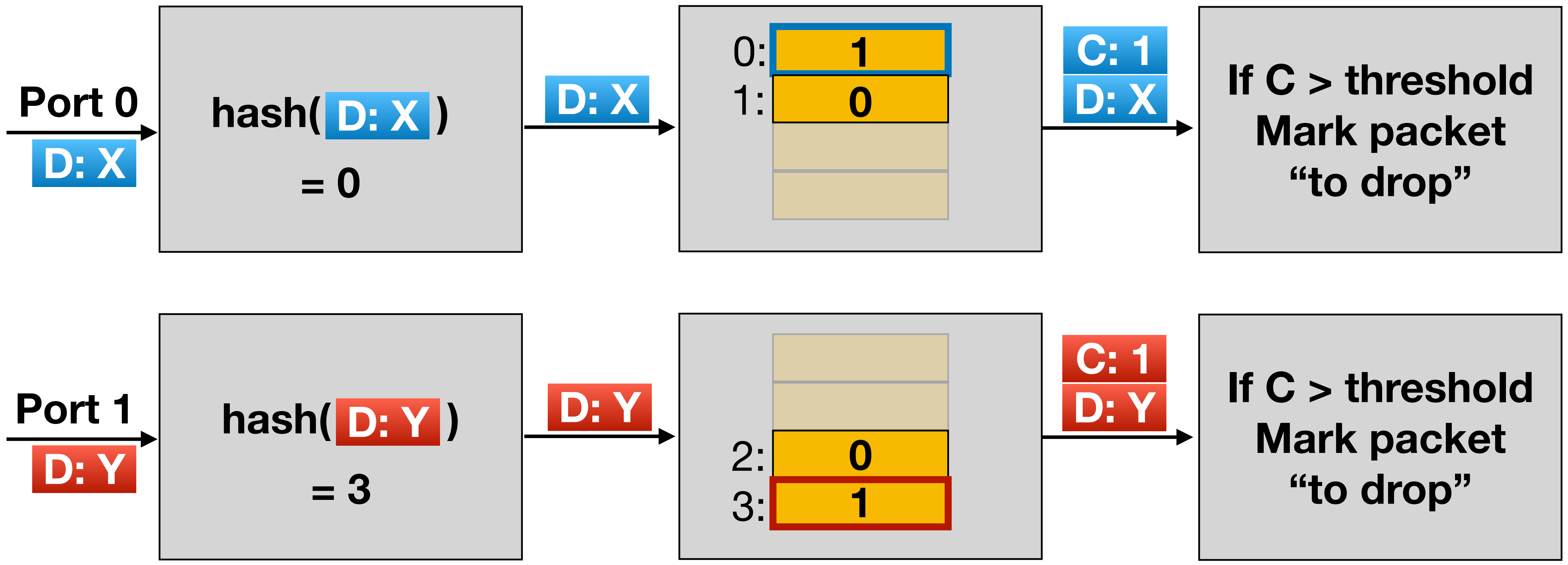

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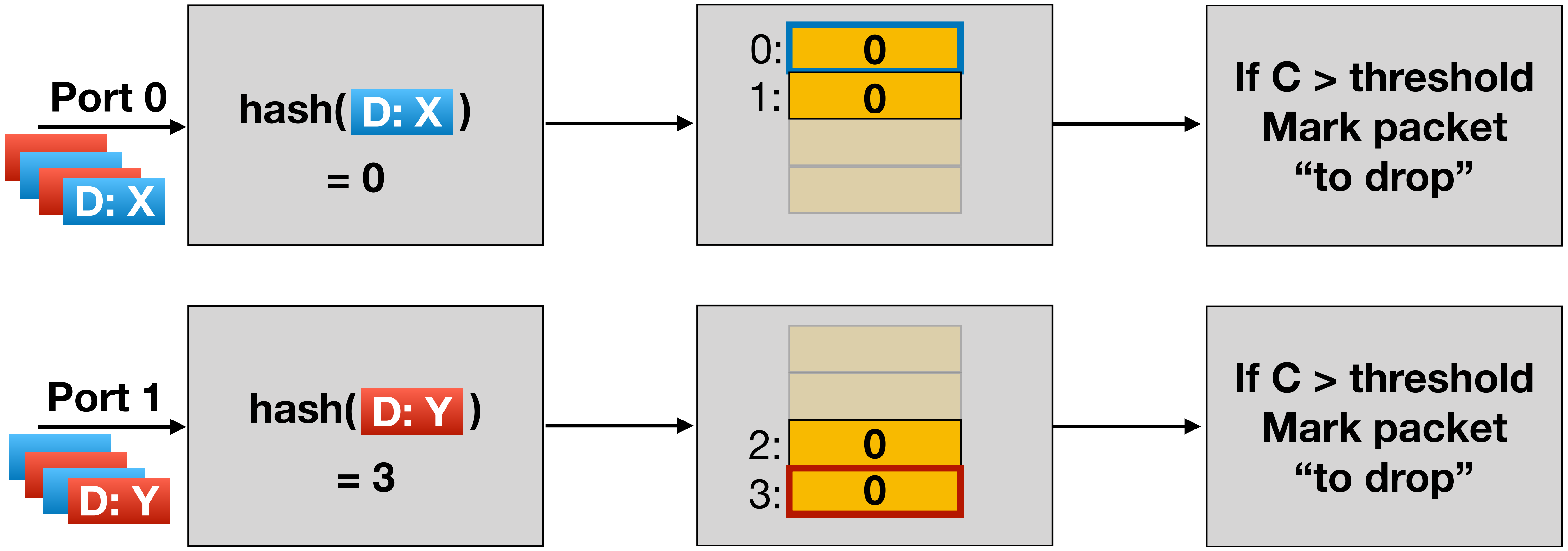

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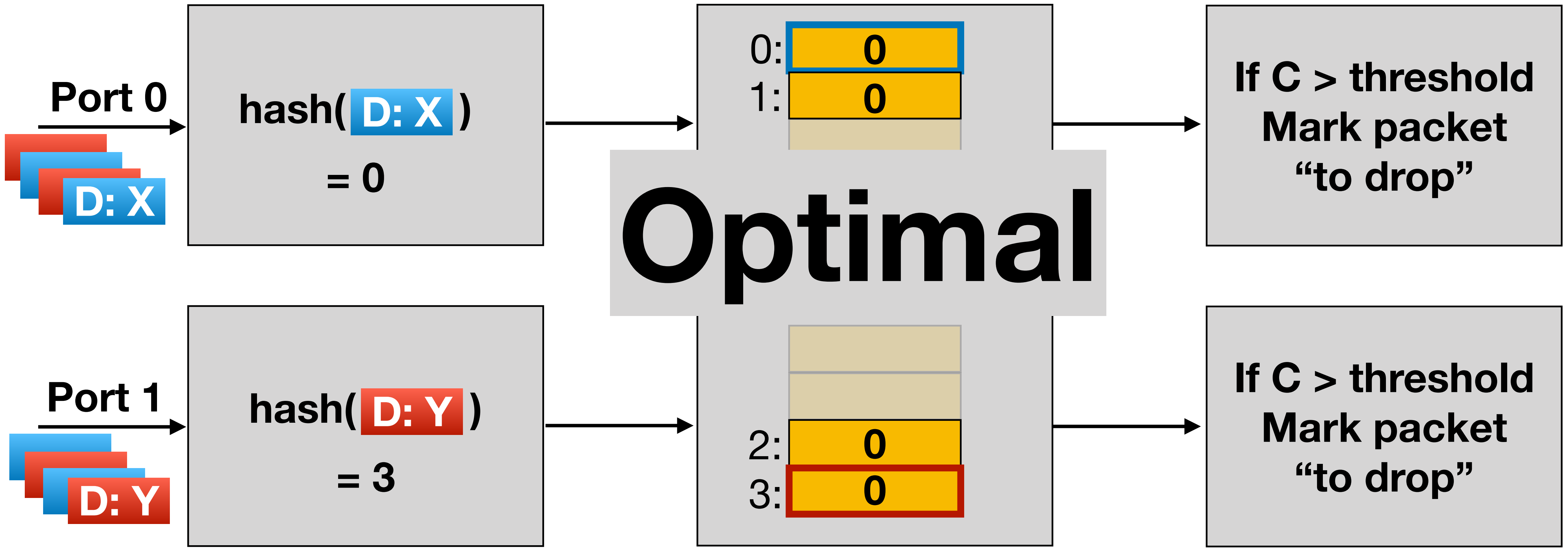

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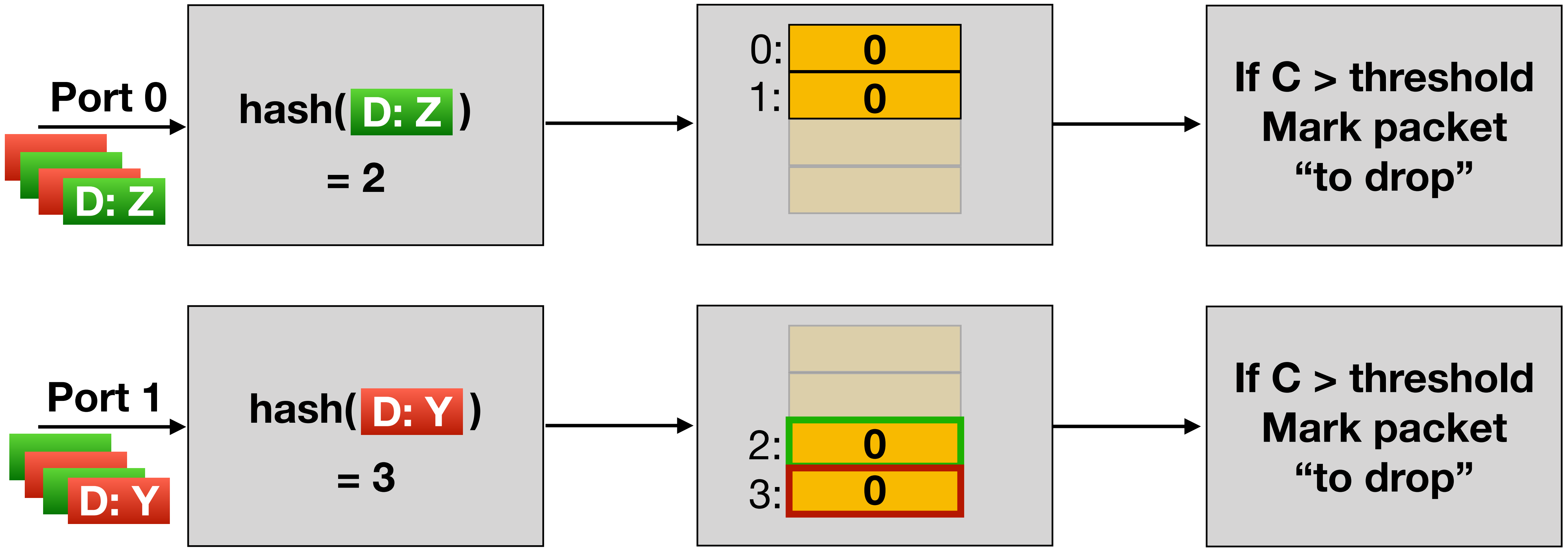

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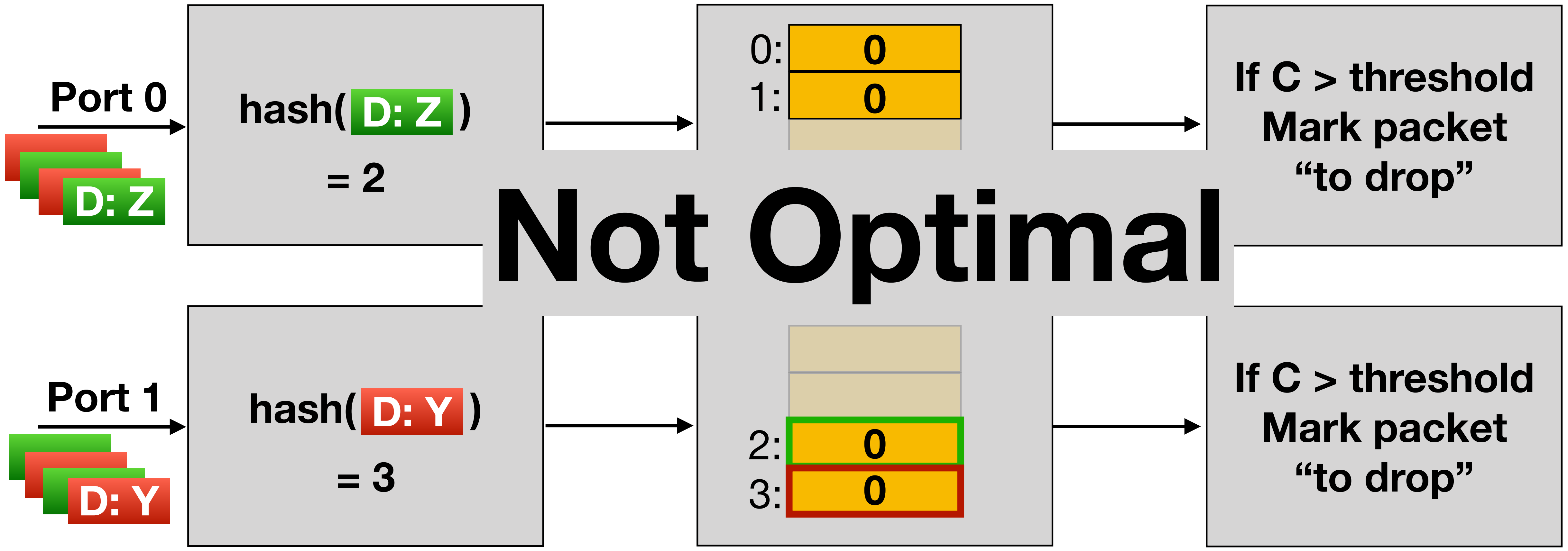

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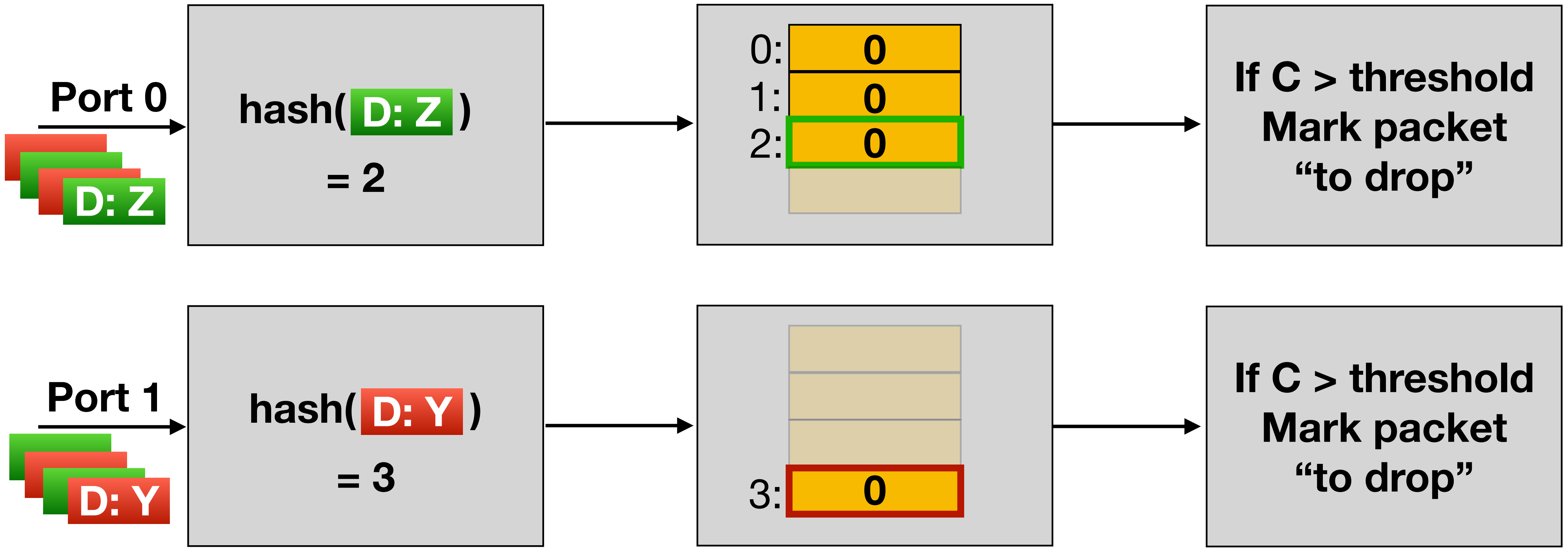

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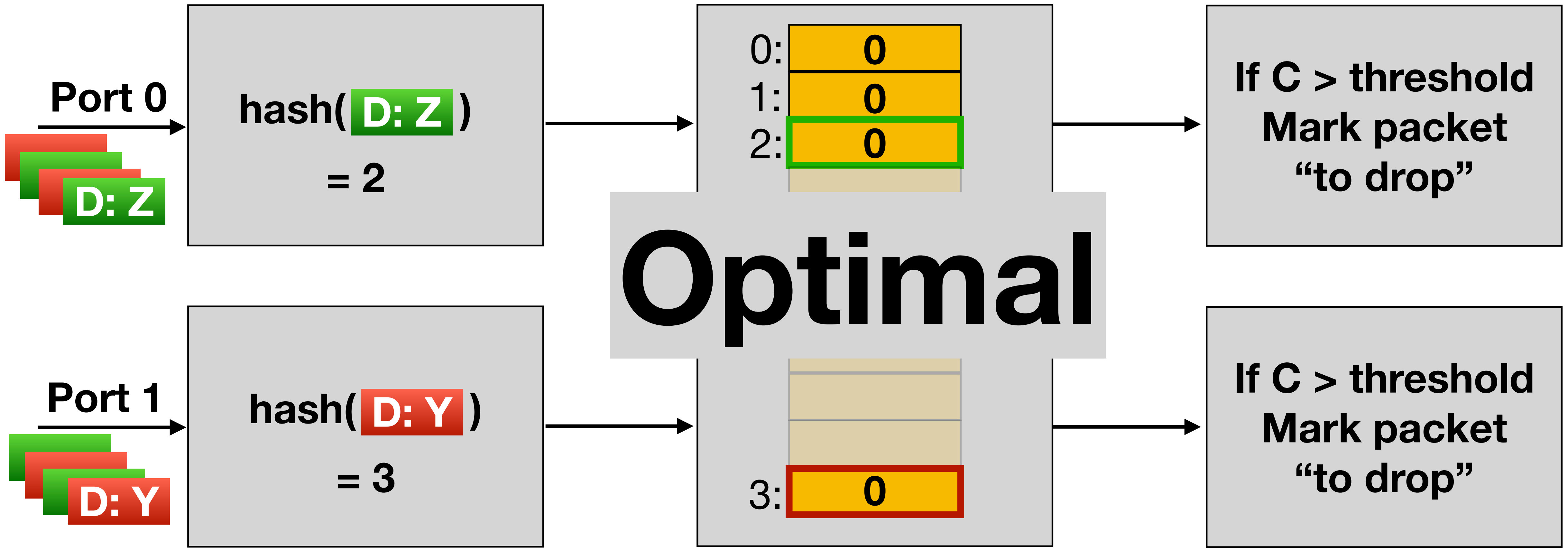

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Reduces to a variant of **bin packing** problem
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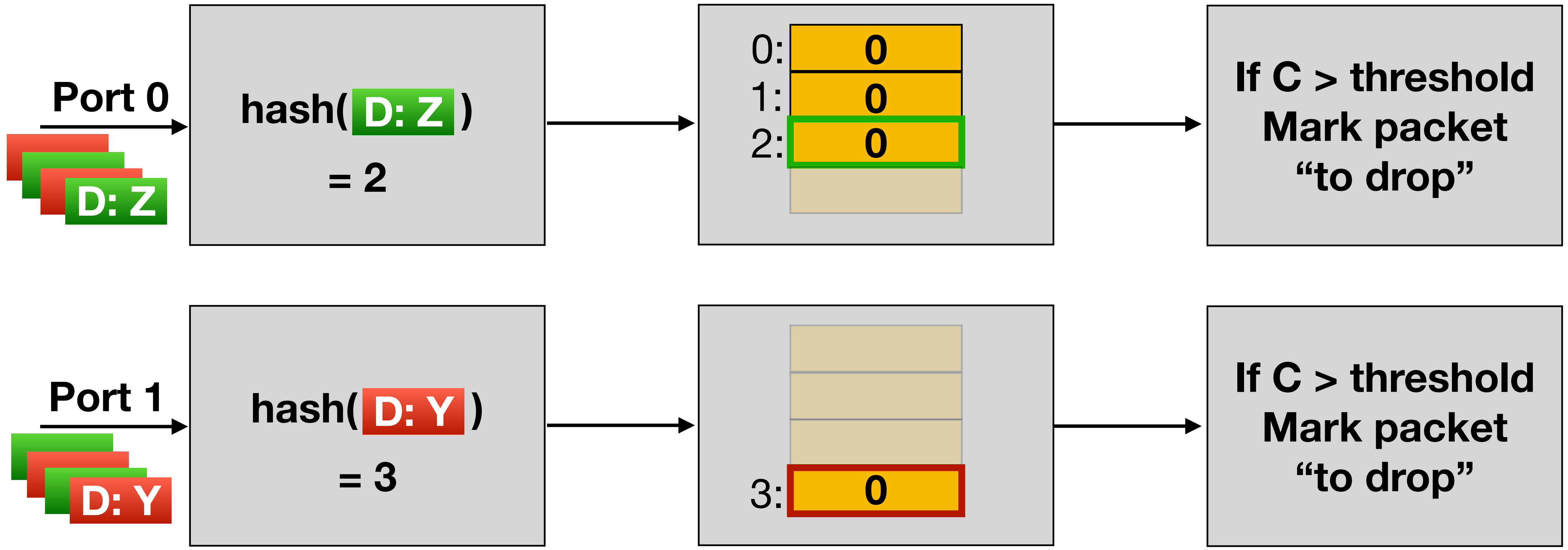
Dynamically shard the shared state across pipelines by **monitoring** the state access patterns at runtime

Reduces to a variant of **bin packing** problem (NP-Hard!)

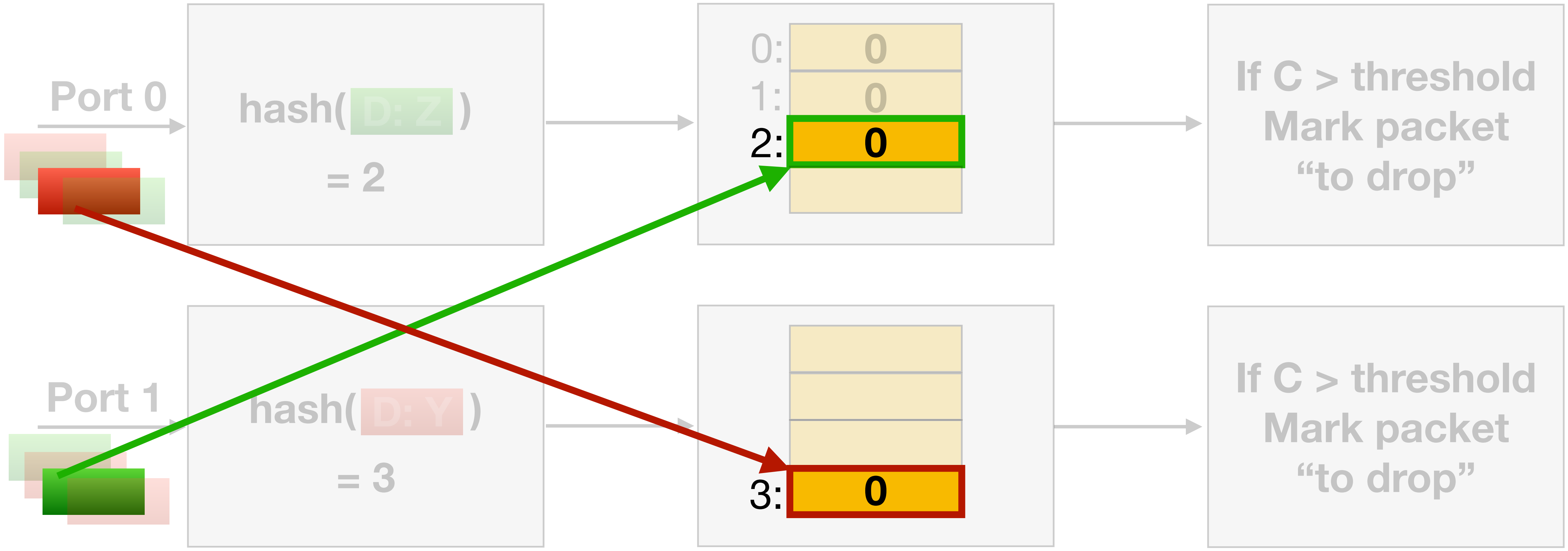
MP5 uses a heuristic to approximates bin packing that is amenable to fast hardware implementation

One Missing Detail



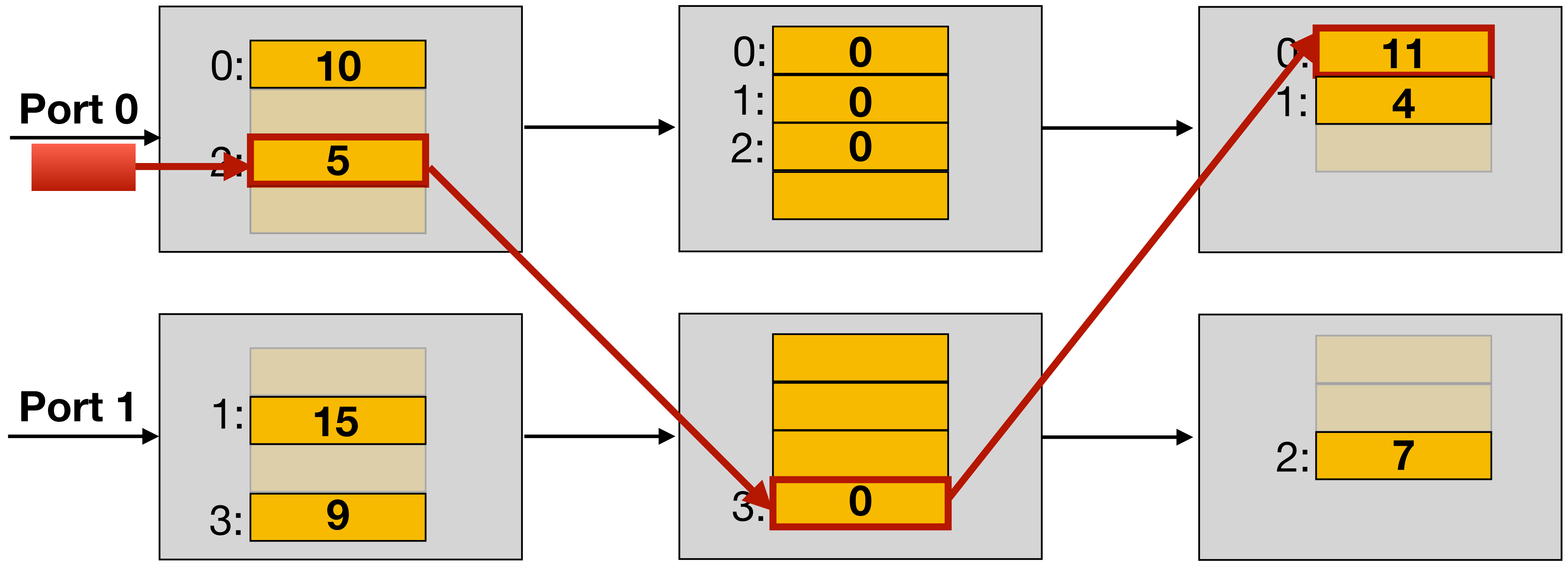
One Missing Detail

Packet and the corresponding shared state may be on different pipelines!



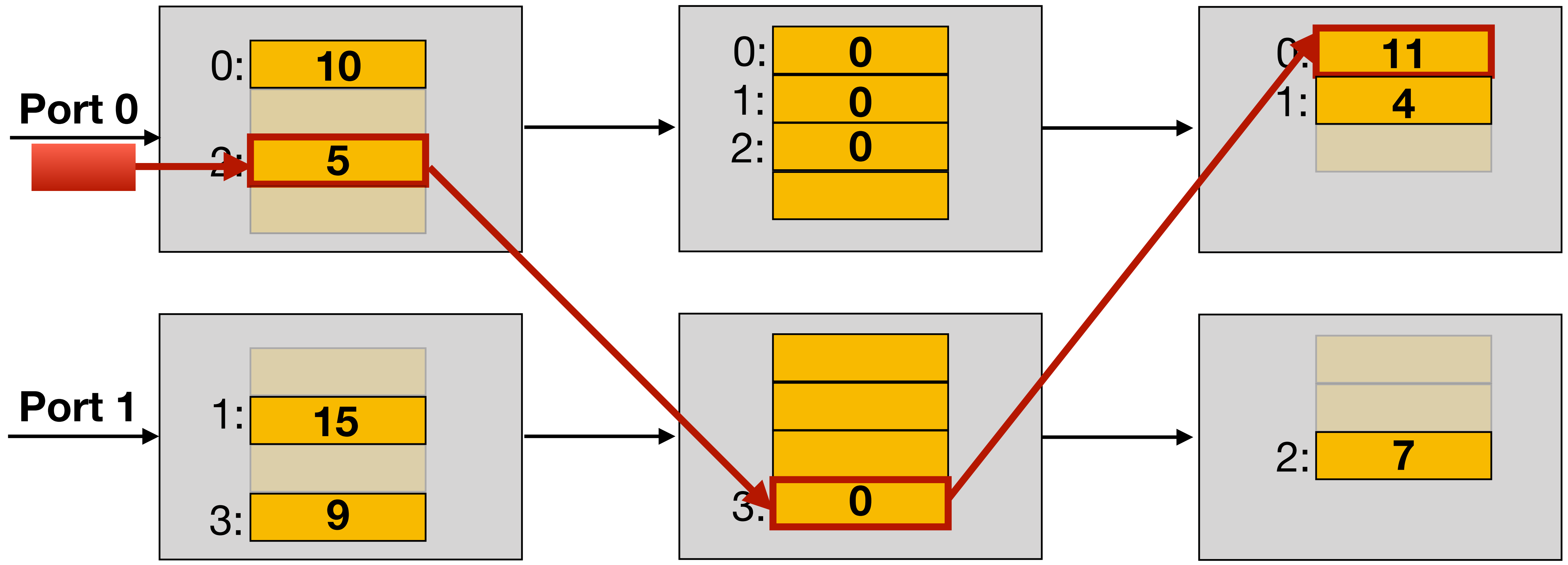
One Missing Detail

Packet may need to go back and forth between pipelines to access the shared states!



One Missing Detail

How to steer packets to a shared state in a remote pipeline?



Existing Solution

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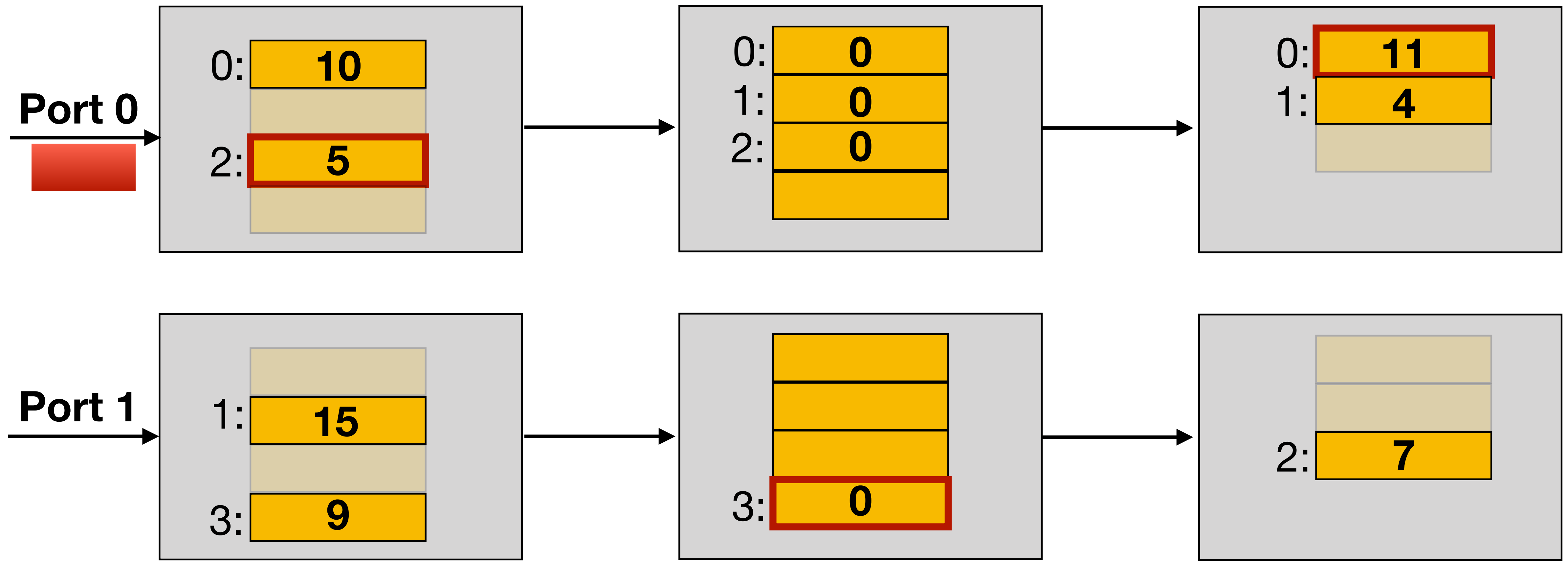

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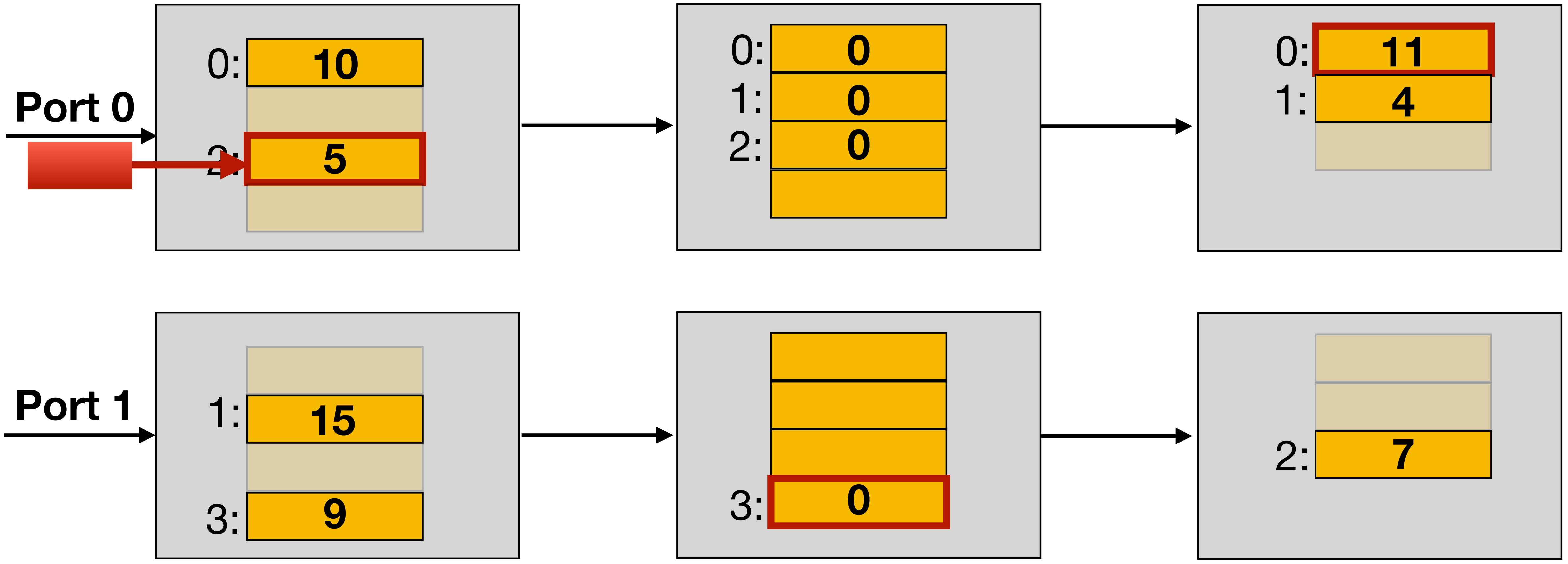

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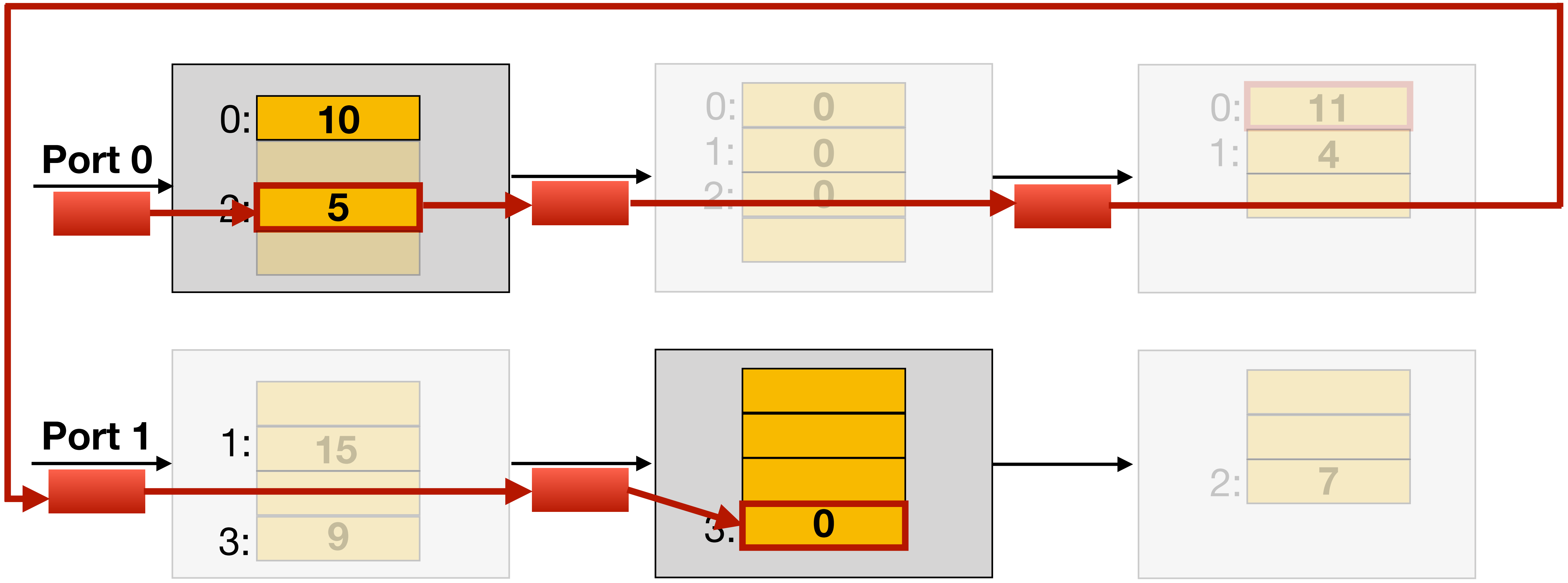

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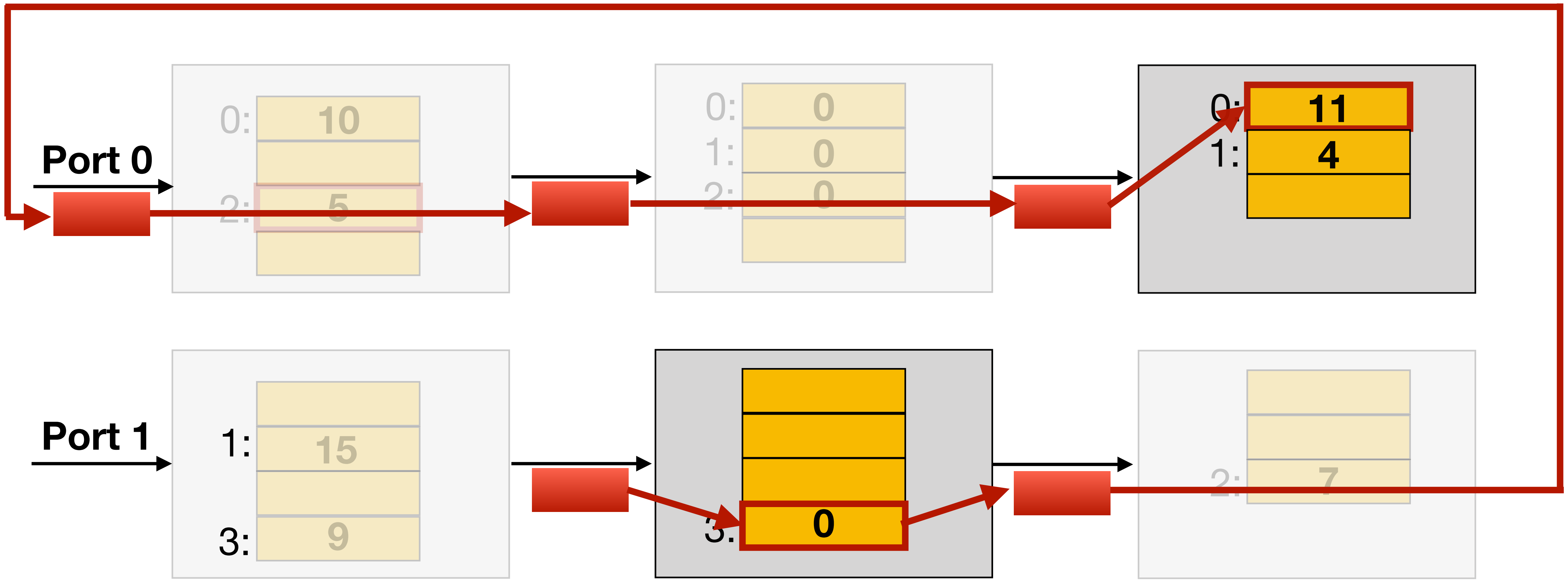

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How to steer packets to a shared state in a remote pipeline?

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results in **throughput penalty** and **increased latency**

…because packets re-visit same stages multiple times!

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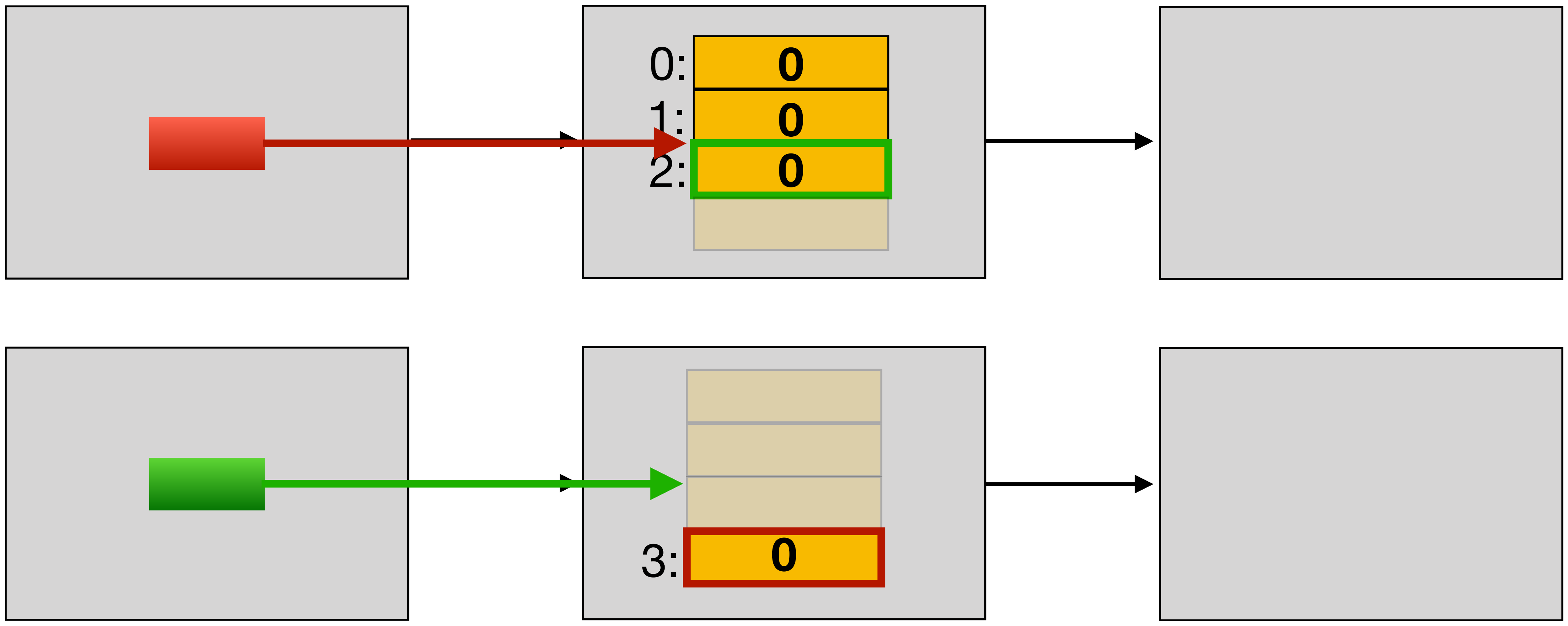
Need a **feed-forward-only** packet steering design

Existing Solution

How to steer packets to a shared state in a remote pipeline?

Current switch design

A packet in stage ***i*** of pipeline ***j*** could move to stage ***i+1*** of only pipeline ***j***



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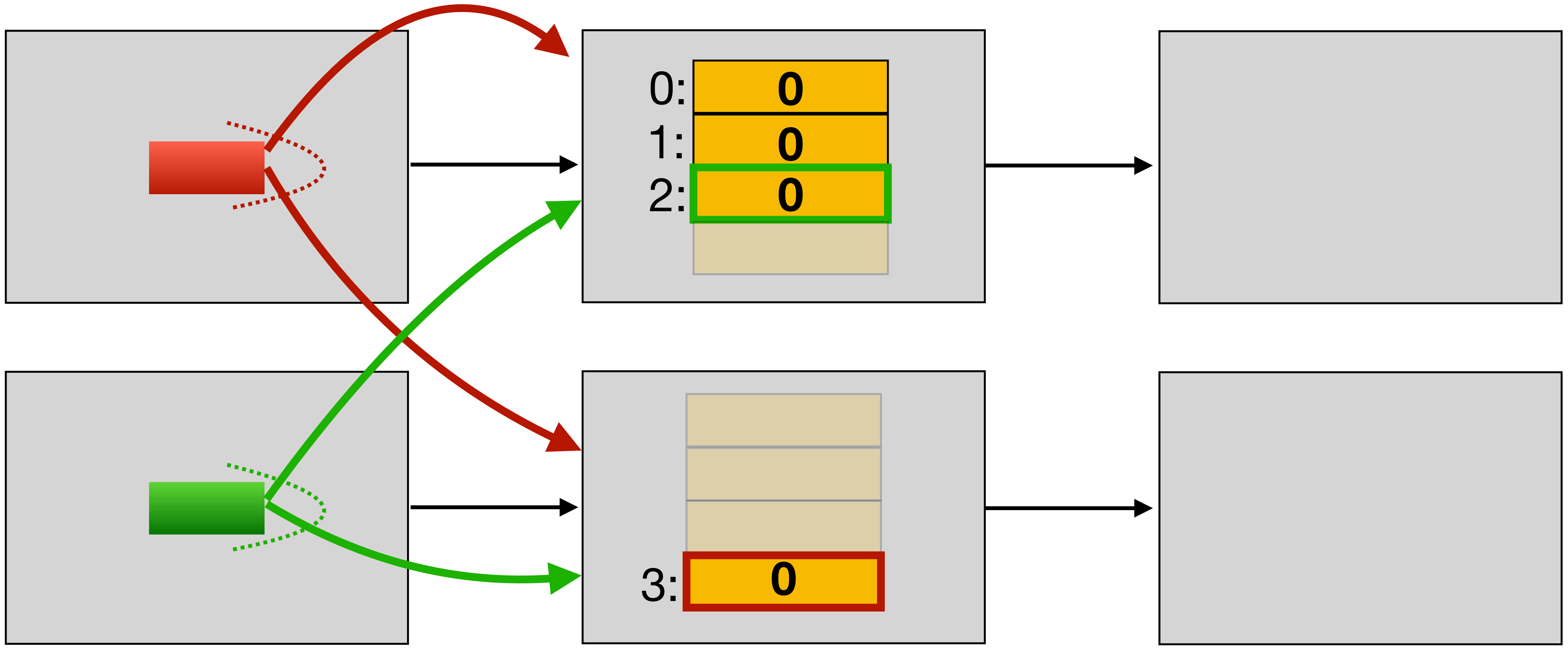
How to steer packets to a shared state in a remote pipeline?

Feed-forward-only packet steering design

A packet in stage ***i*** of pipeline ***j*** could move to stage ***i+1*** of ~~only pipeline *j*~~ ***any*** pipeline



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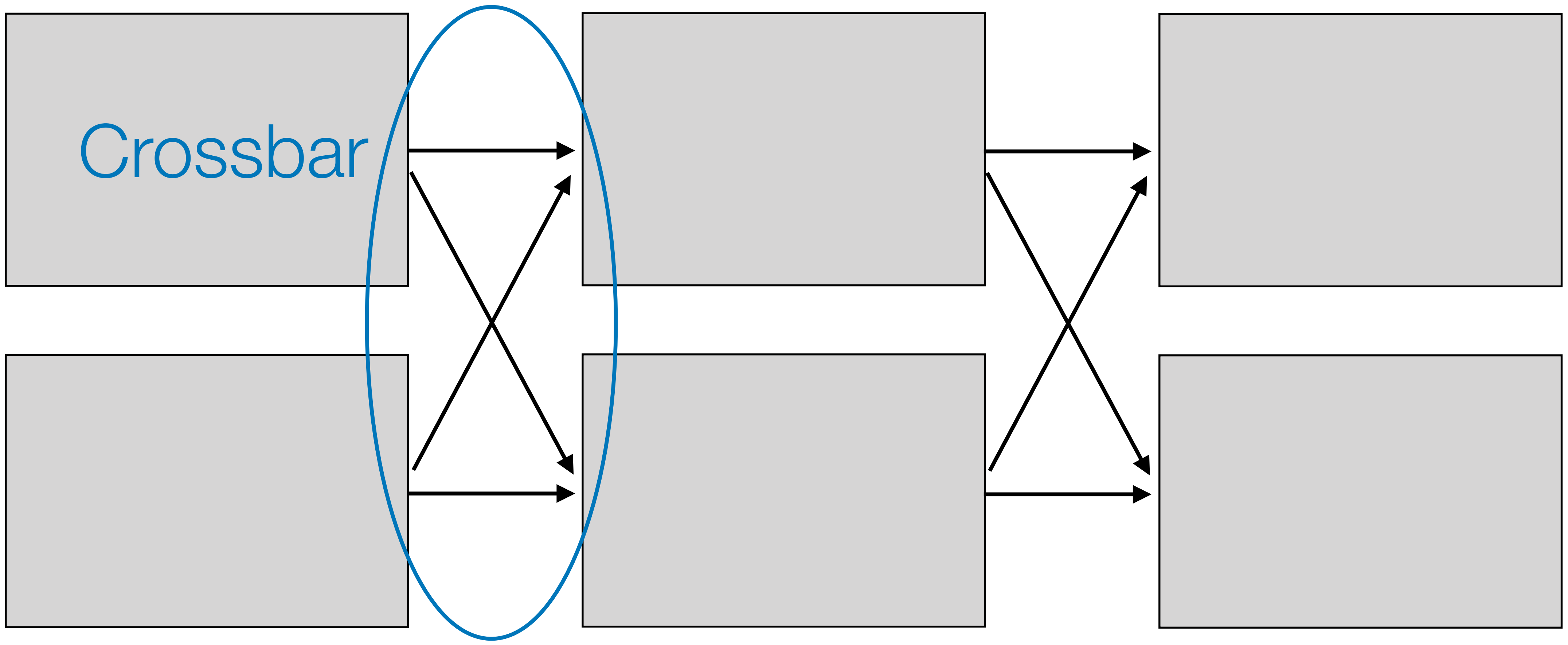

Question Re-visited

How to improve performance?
(without violating functional equivalence)

Goals and Techniques

Techniques	Functional Equivalence		Performance	
	Stateless	Stateful	Stateless	Stateful
Replicate stateless processing	✓		✓	
+				
~~Limit stateful processing to single pipeline~~	~~✓~~	~~✓~~	~~✓~~	~~✗~~
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Dynamic state sharding & Feed-forward pkt steering	✓		✓	✓

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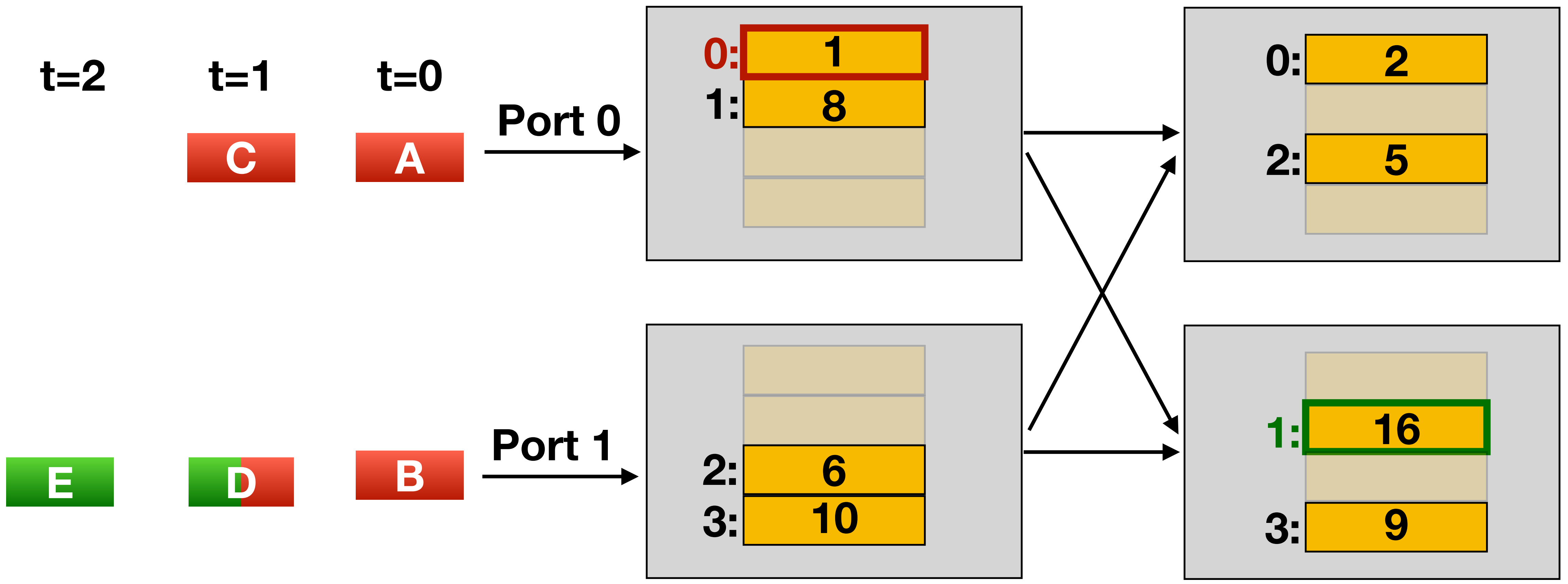
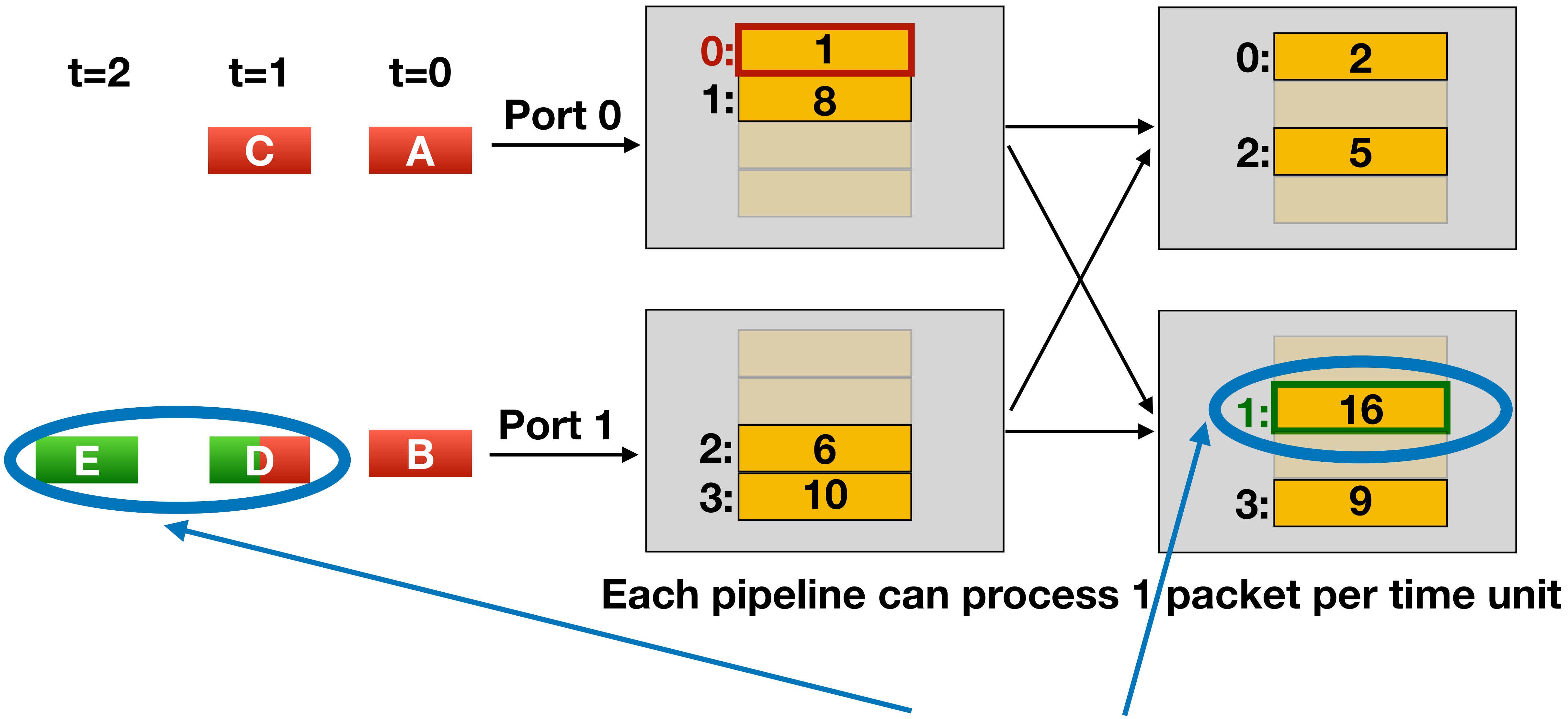


Each pipeline can process 1 packet per time unit

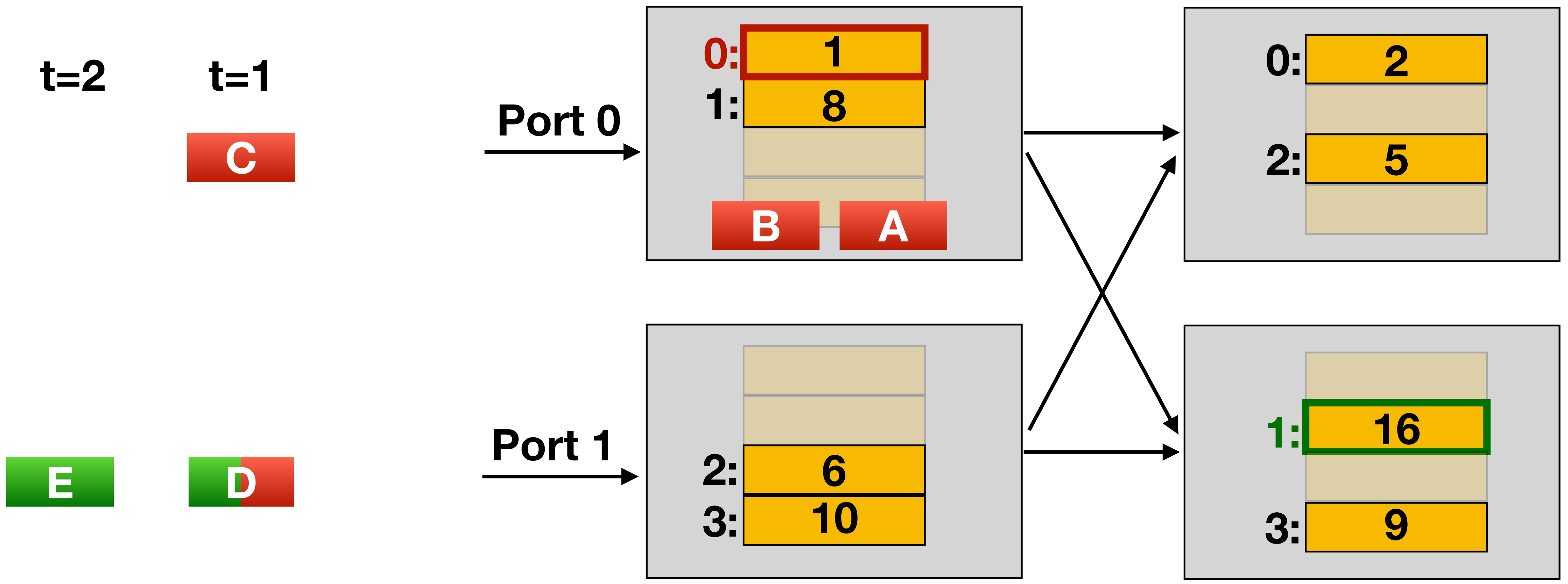
Problem



Each pipeline can process 1 packet per time unit

On a single-pipelined switch, D will always access register index 1 in stage 2 before E

Problem



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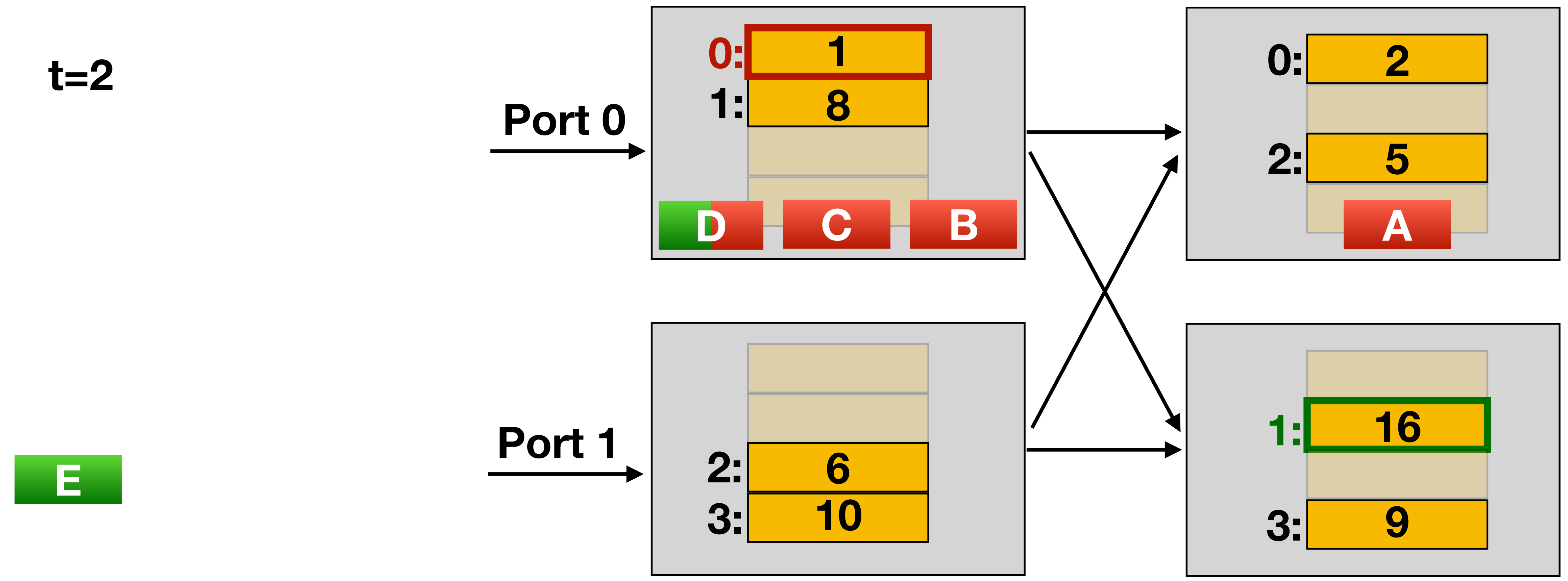

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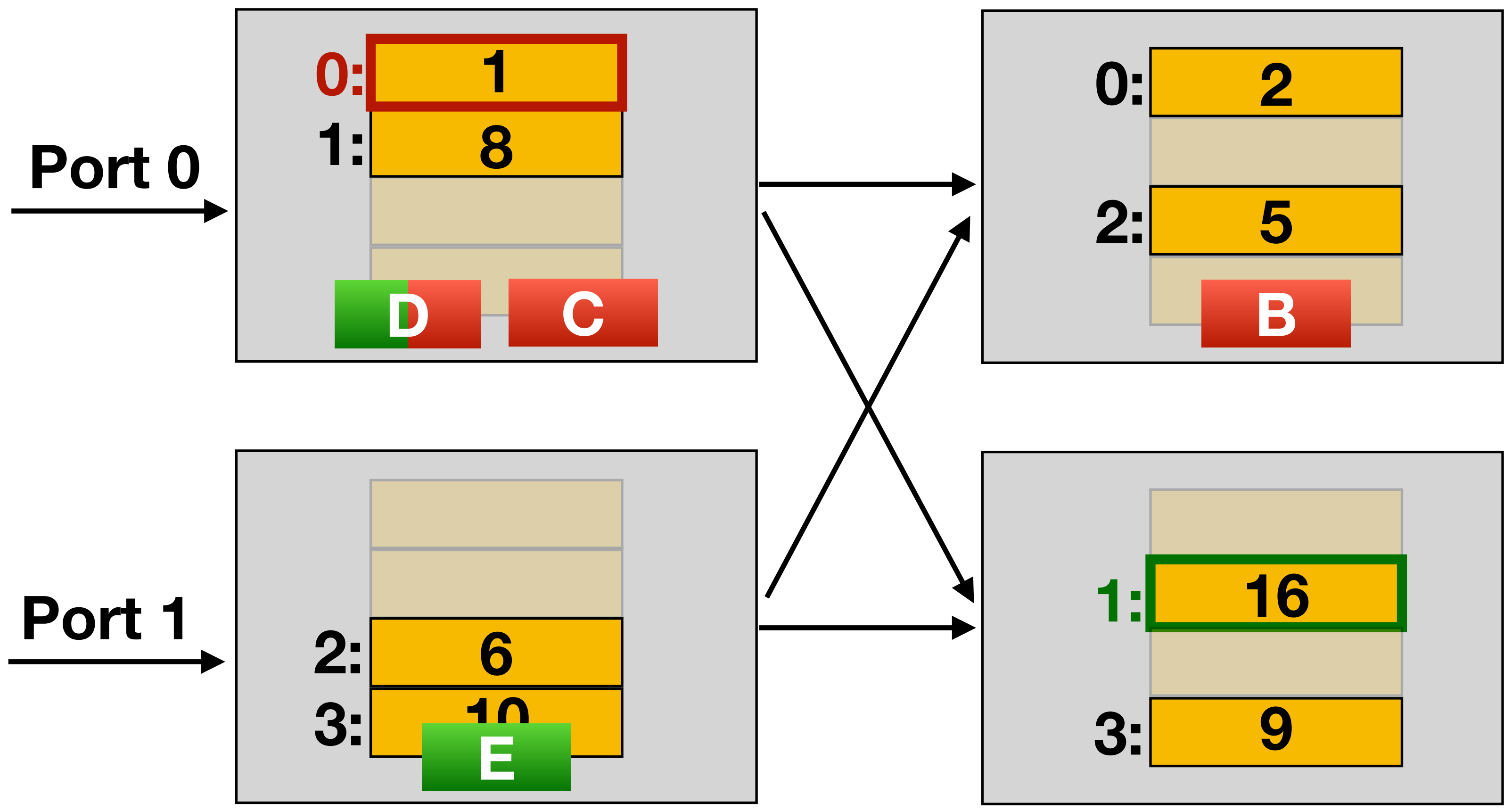

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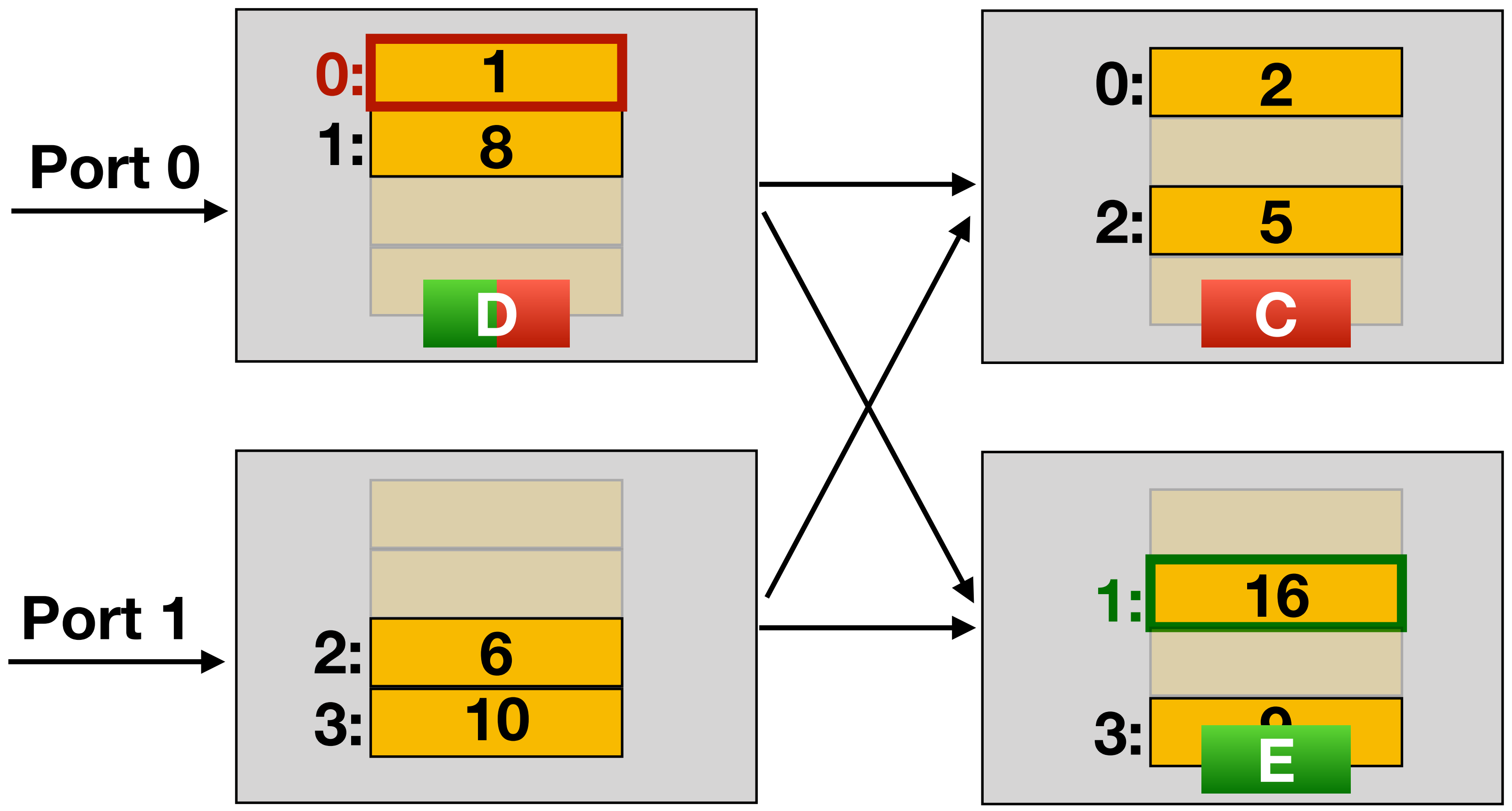

Each pipeline can process 1 packet per time unit

E will access index 1 in stage 2 before D!

(may violate functional equivalence)

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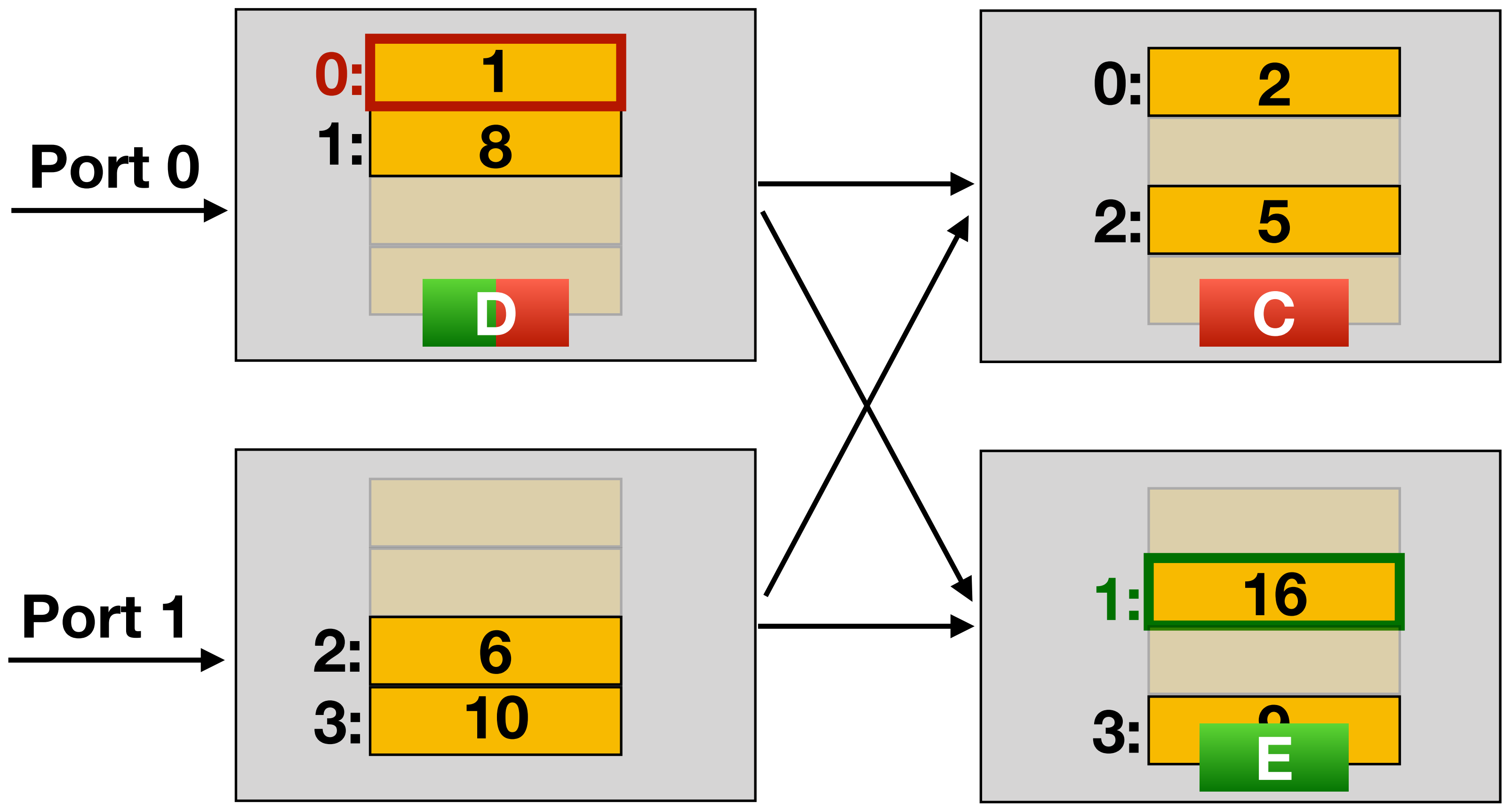

Each pipeline can process 1 packet per time unit

E will access index 1 in stage 2 before D!

(may violate functional equivalence)

Packet re-ordering can also impact application performance

e.g., if D and E belong to same TCP flow

Problem

How to avoid packet re-ordering and out-of-order state access?

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Too late if we try to enforce ordering *after* a packet visits a stateful stage
…due to non-deterministic waits at a stateful stage

Solution

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Too late if we try to enforce ordering *after* a packet visits a stateful stage
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Enforce ordering **preemptively** (i.e., *before* a packet reaches a stateful stage)

Solution

How to avoid packet re-ordering and out-of-order state access?

Step 1: Preemptively figure out all states a packet would access

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Hard in general (even impossible in some cases)

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Insight: Most packet processing programs access register index based on hash of a subset of packet header fields

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How to avoid packet re-ordering and out-of-order state access?

Step 1: Preemptively figure out all states a packet would access

Hard in general (even impossible in some cases)

Insight: Most packet processing programs access register index based on hash of a subset of packet header fields

…can be known as soon as a packet arrives at the switch

Solution

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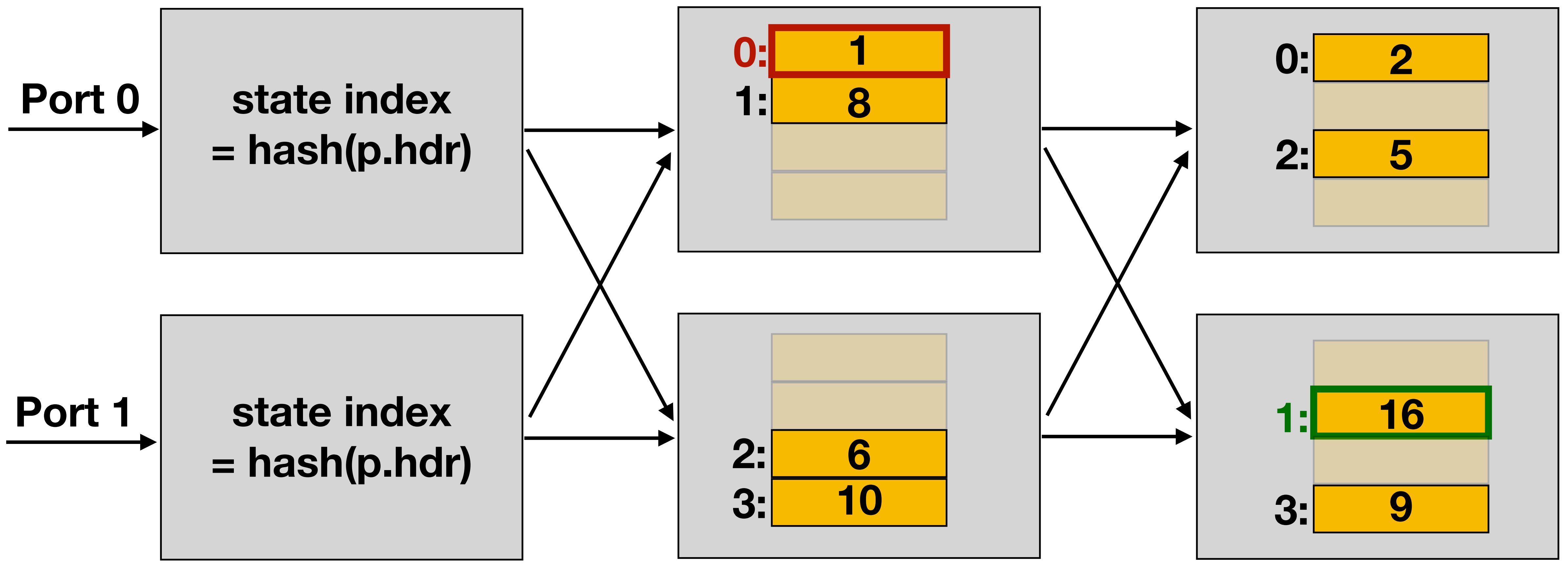
Compiler adds a new stage before any stateful stage



Solution

How to avoid packet re-ordering and out-of-order state access?

Step 2: Enforce ordering in the stateful stages

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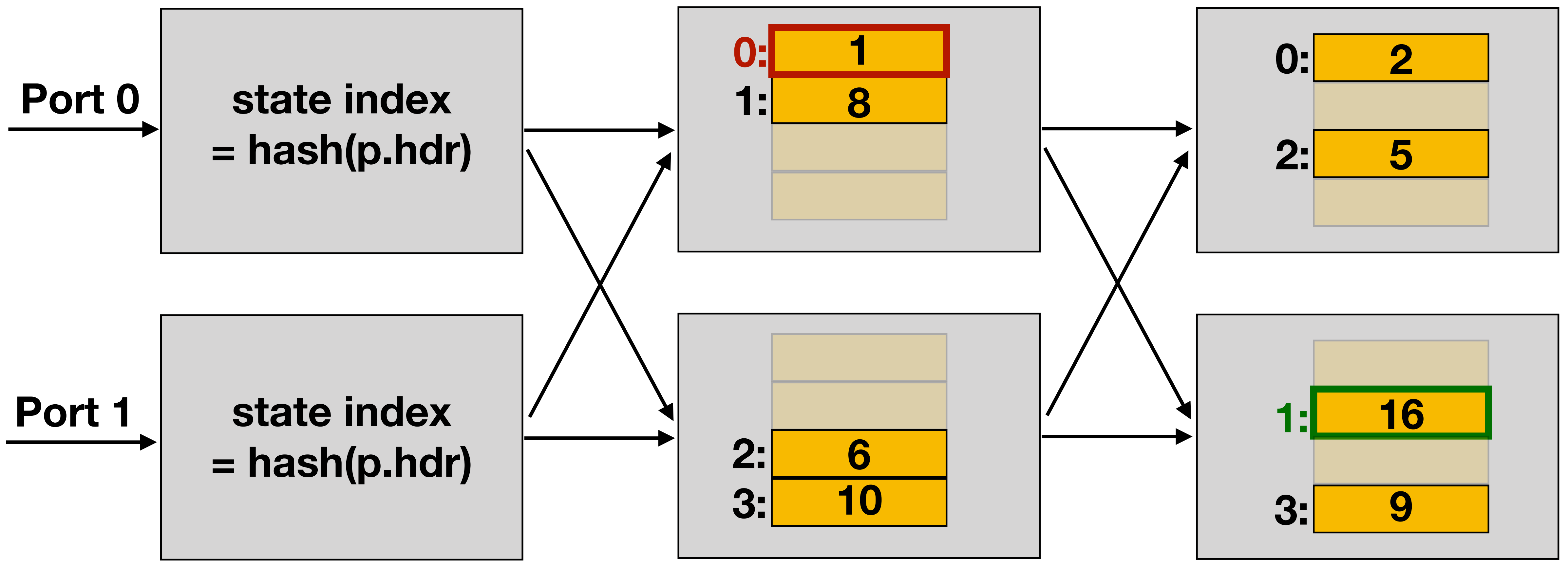

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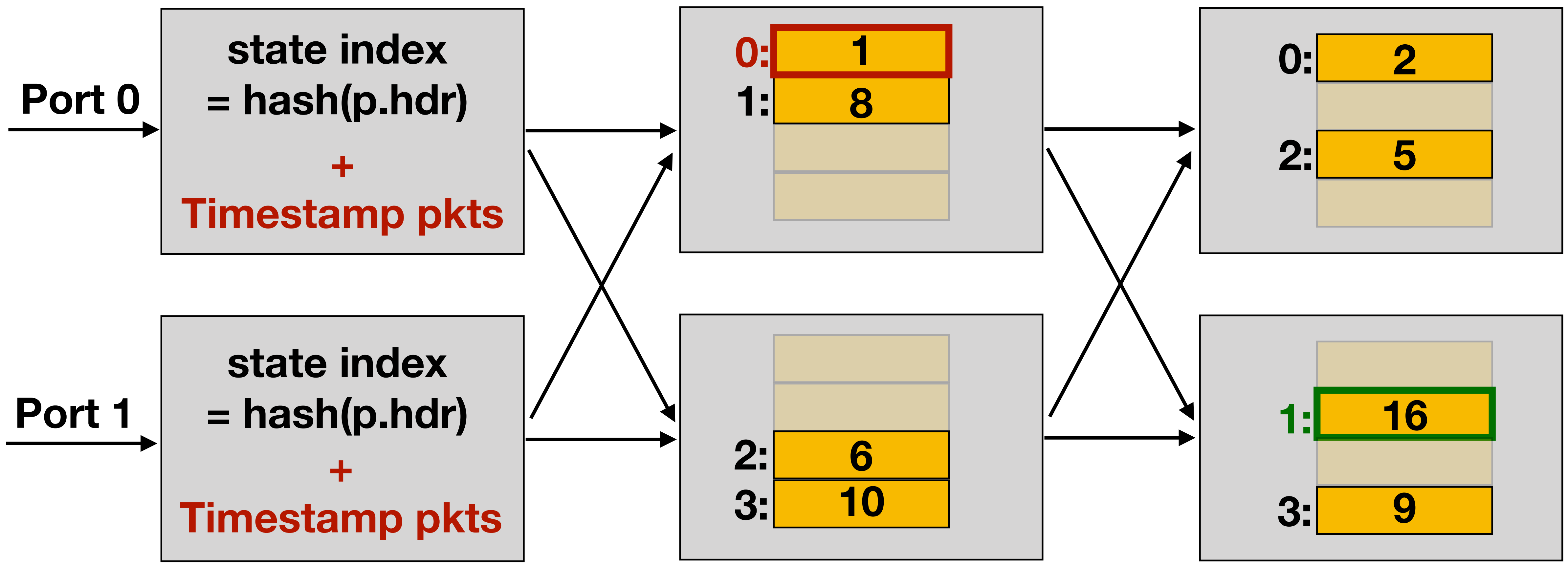
Timestamp Packets?



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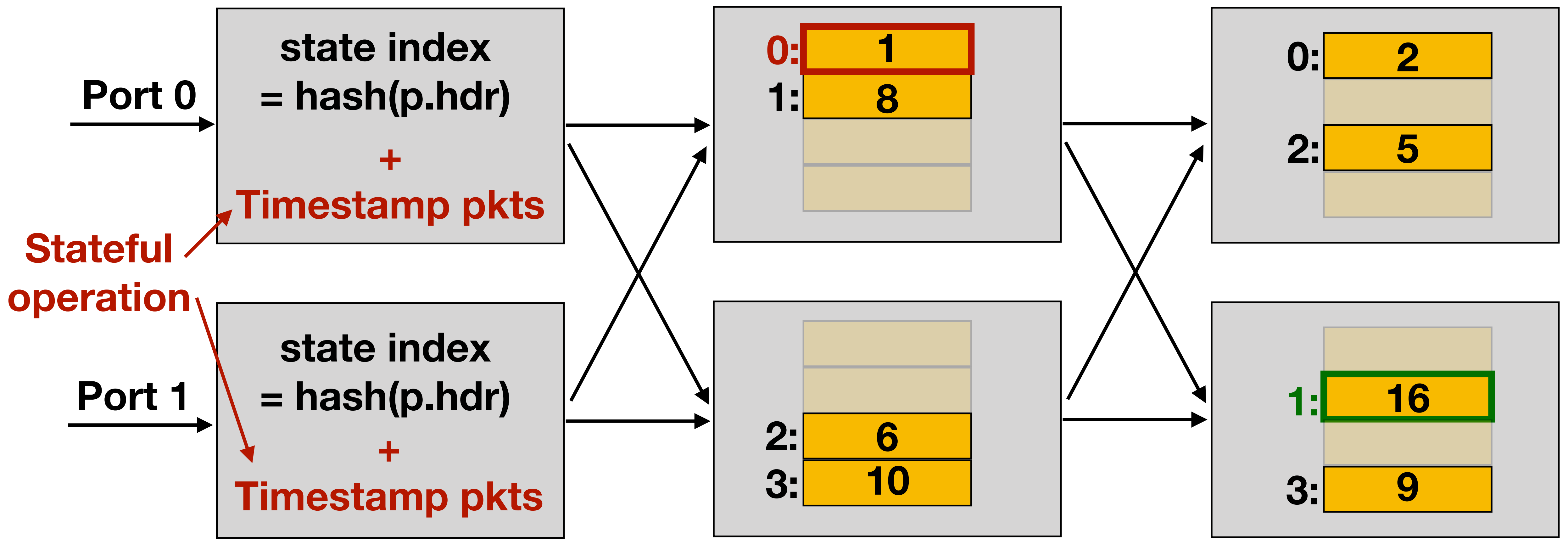
Timestamp Packets? - won't work!



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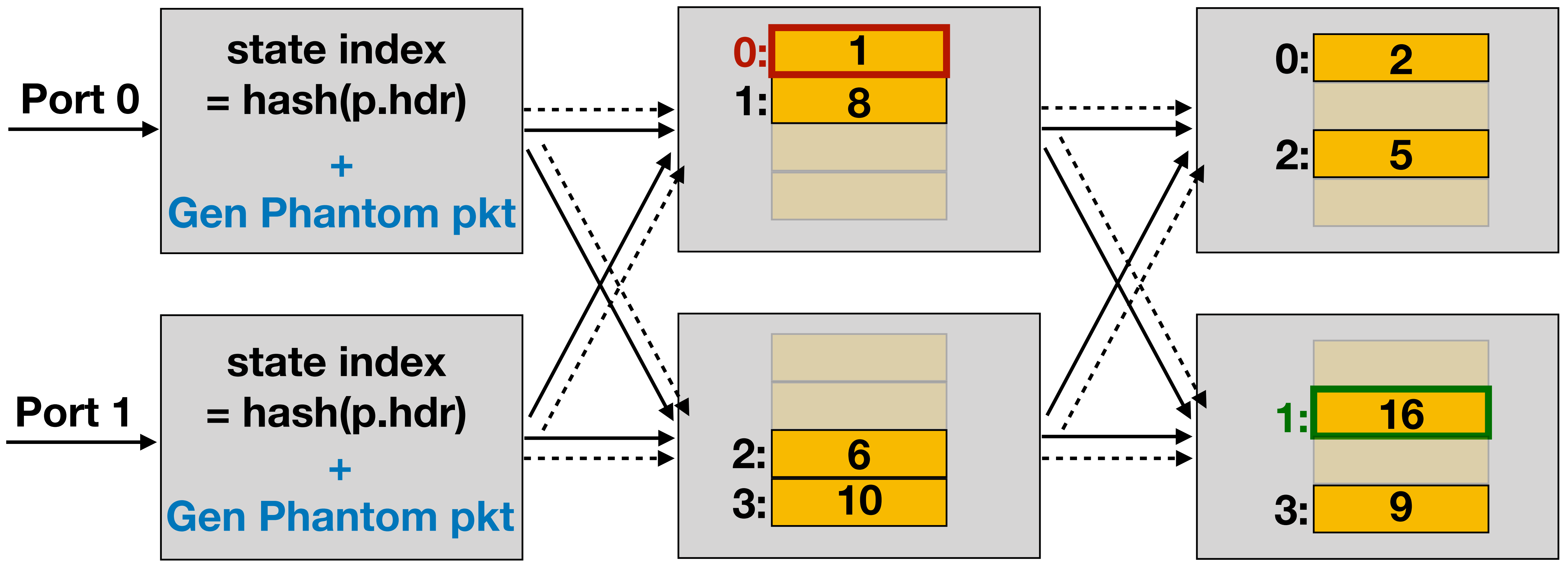
Generate "placeholders" for data packets



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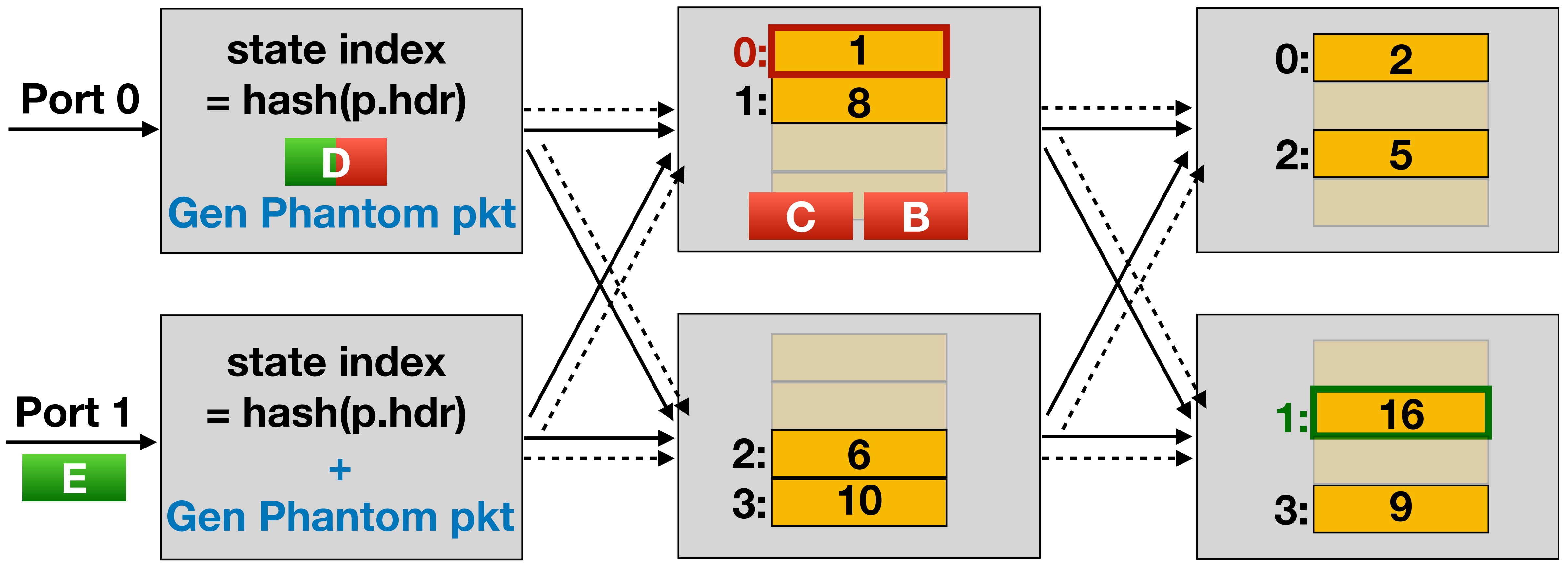

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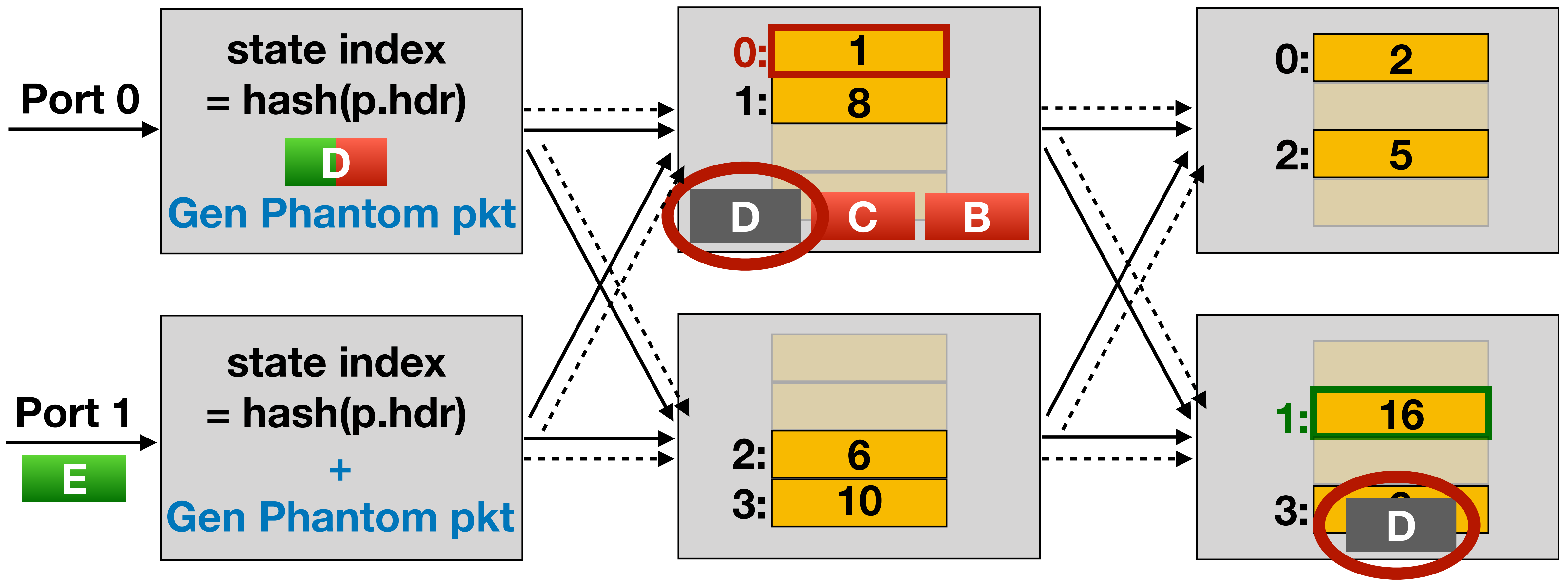

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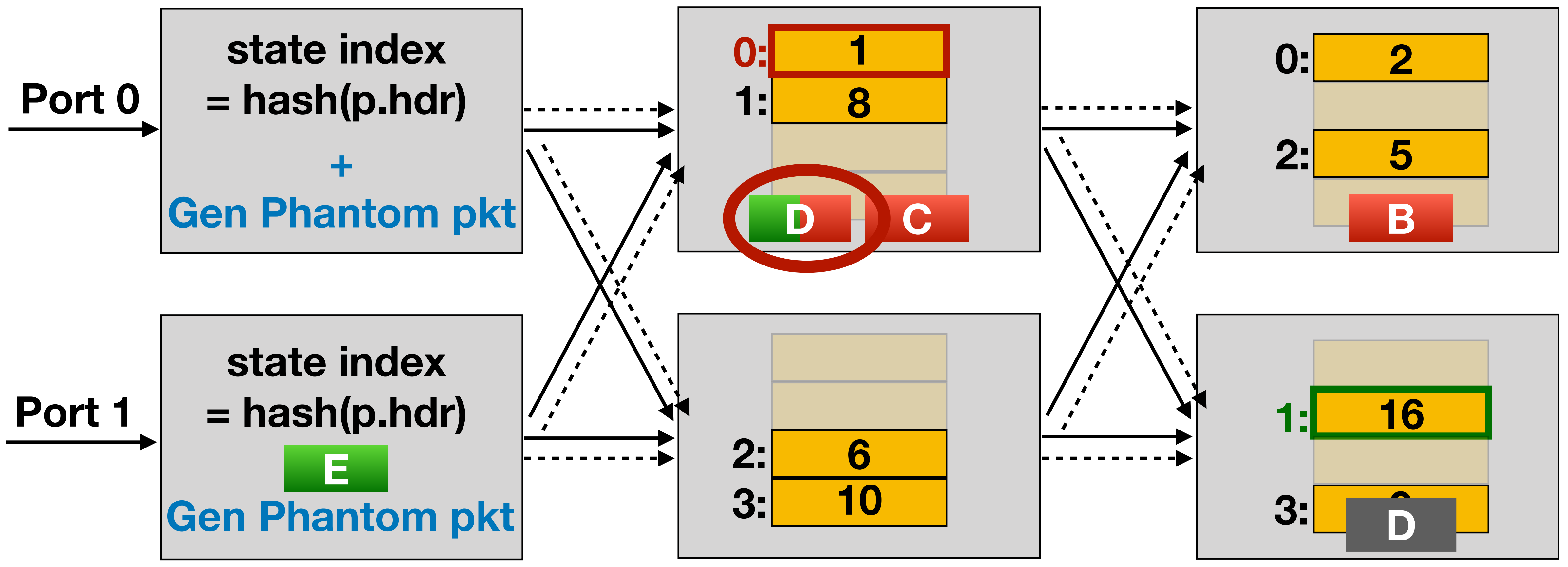

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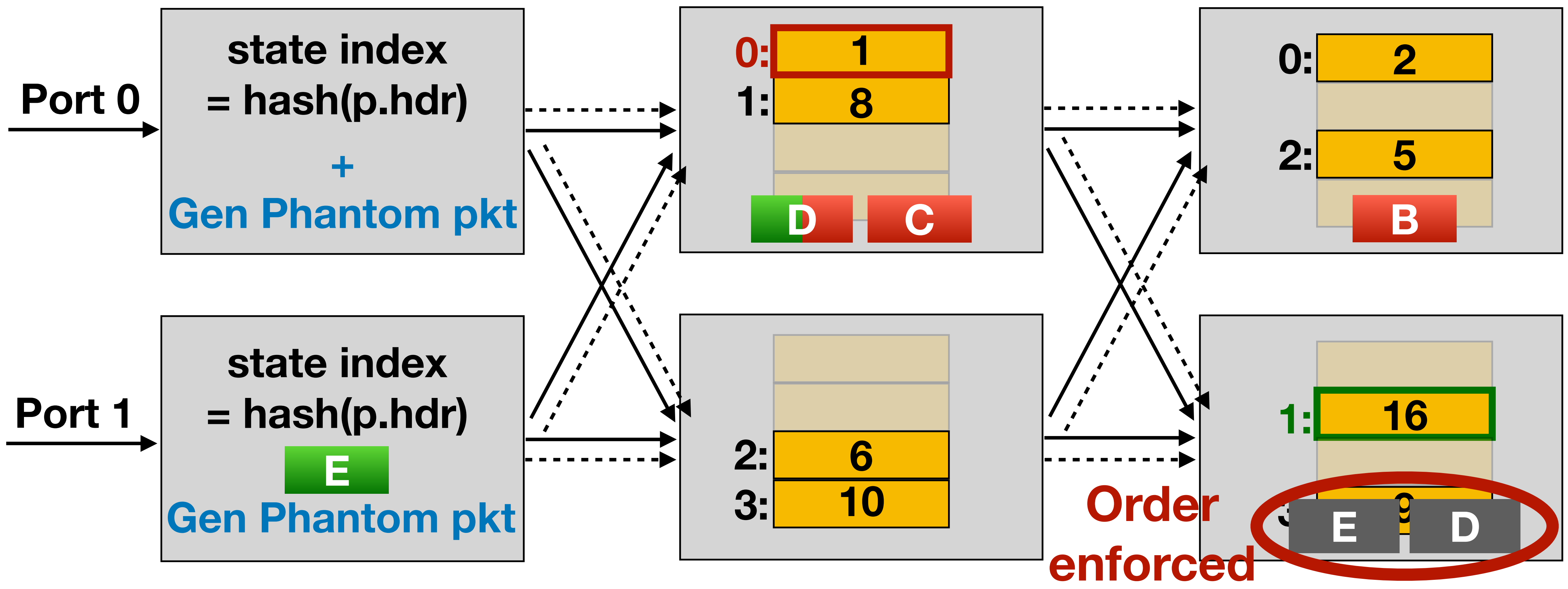
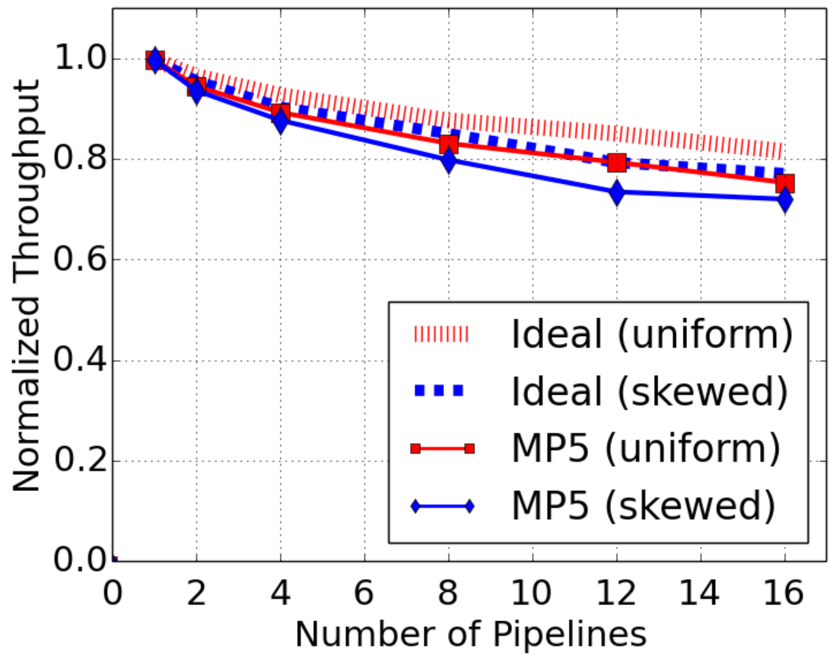


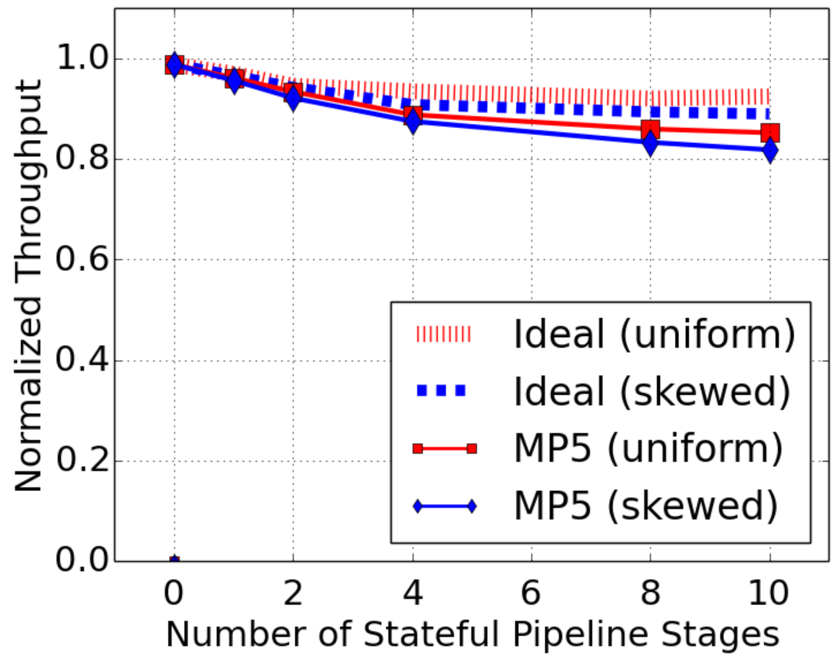
Goals and Techniques

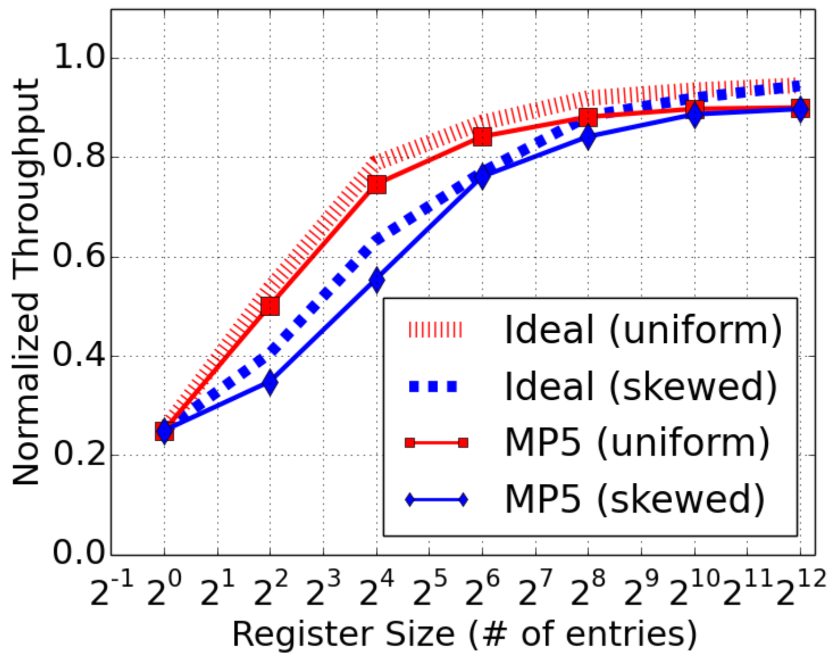
Techniques	Functional Equivalence		Performance	
	Stateless	Stateful	Stateless	Stateful
Replicate stateless processing	✓		✓	
+				
~~Limit stateful processing to single pipeline~~	~~✓~~	~~✓~~	~~✓~~	~~✗~~
+				
Dynamic state sharding & Feed-forward pkt steering	✓	✗	✓	✓
+				
Preemptive state access order enforcement	✓	✓	✓	✓

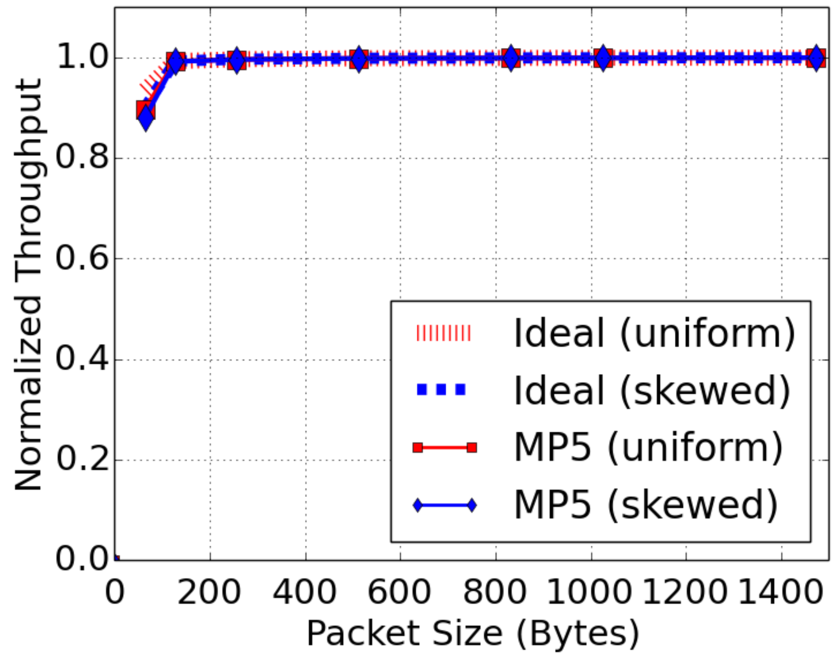
Performance Evaluation

Sensitivity Analysis

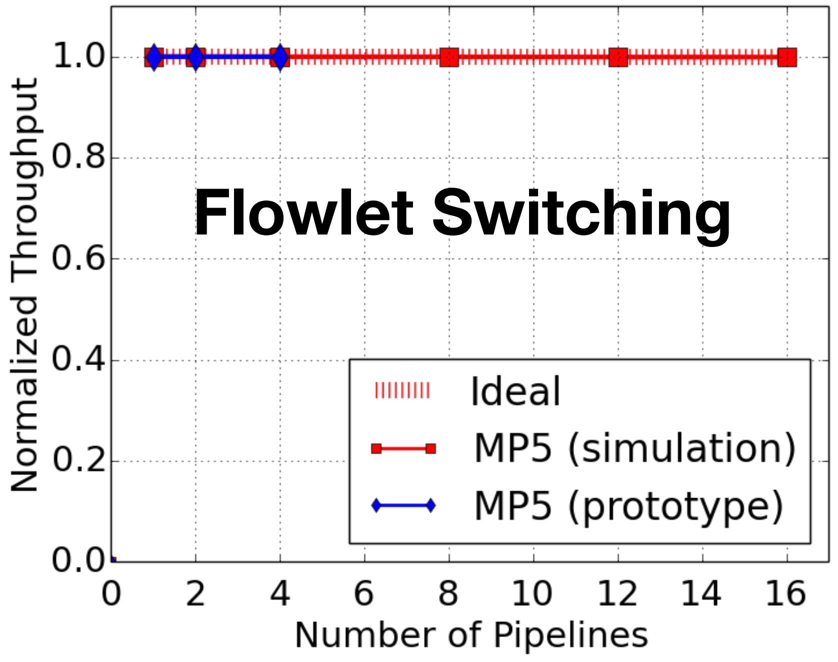


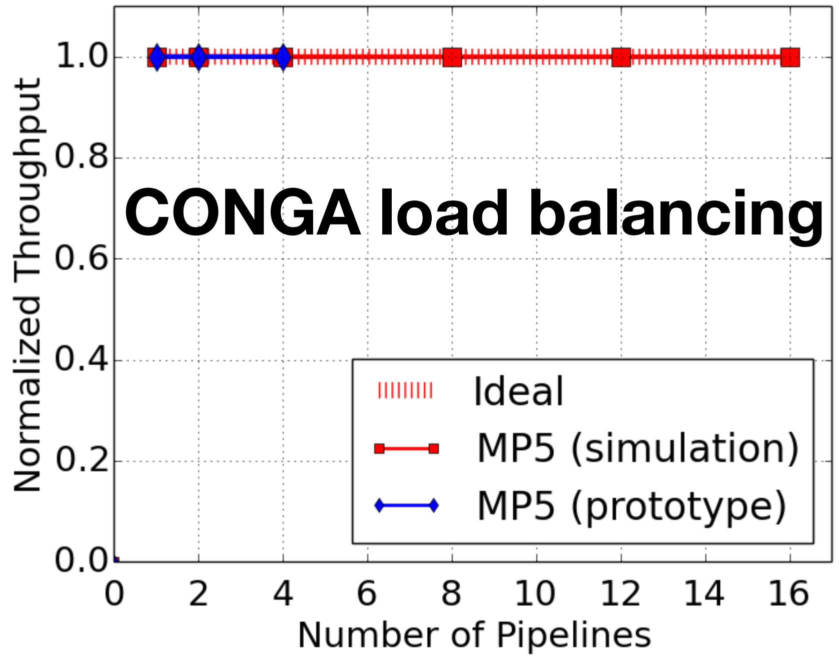


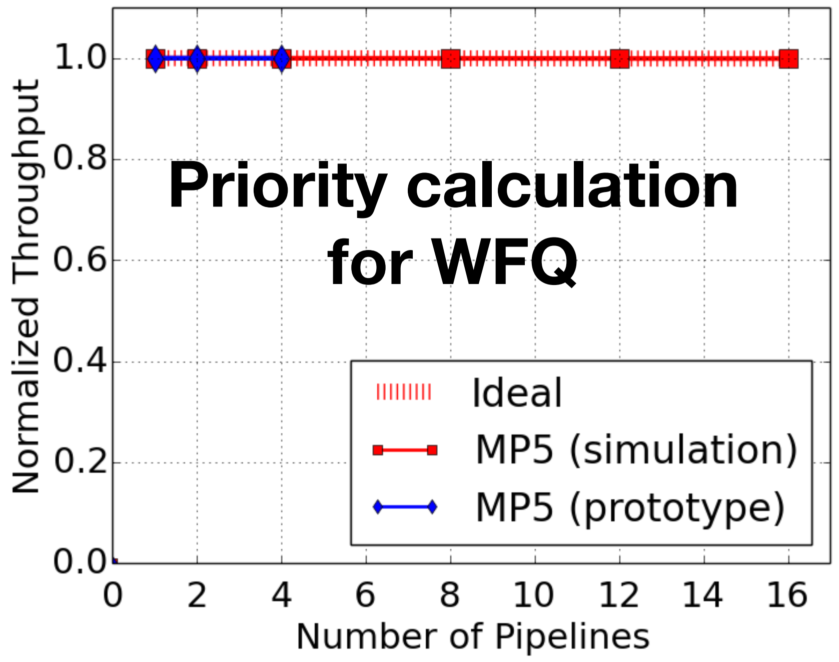


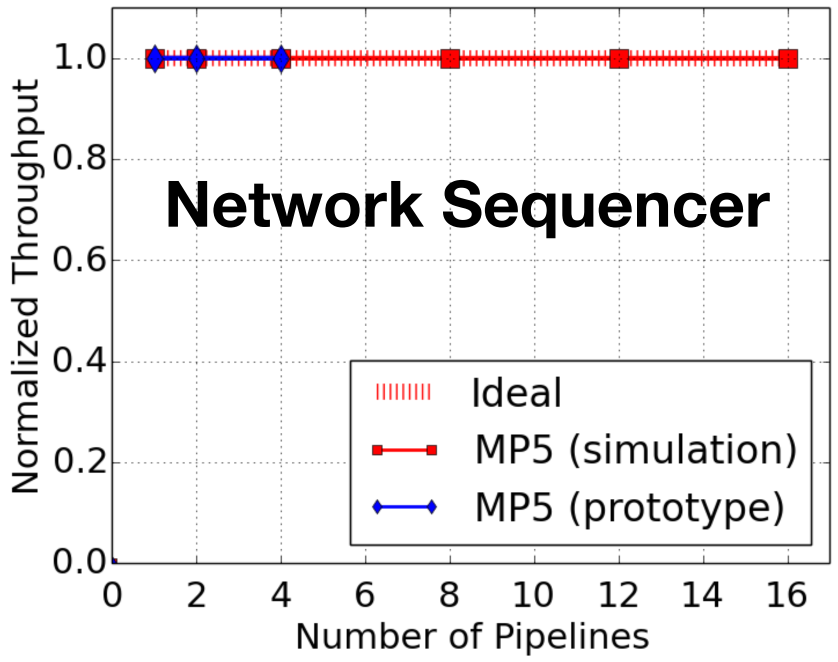


Realistic Workloads & Applications









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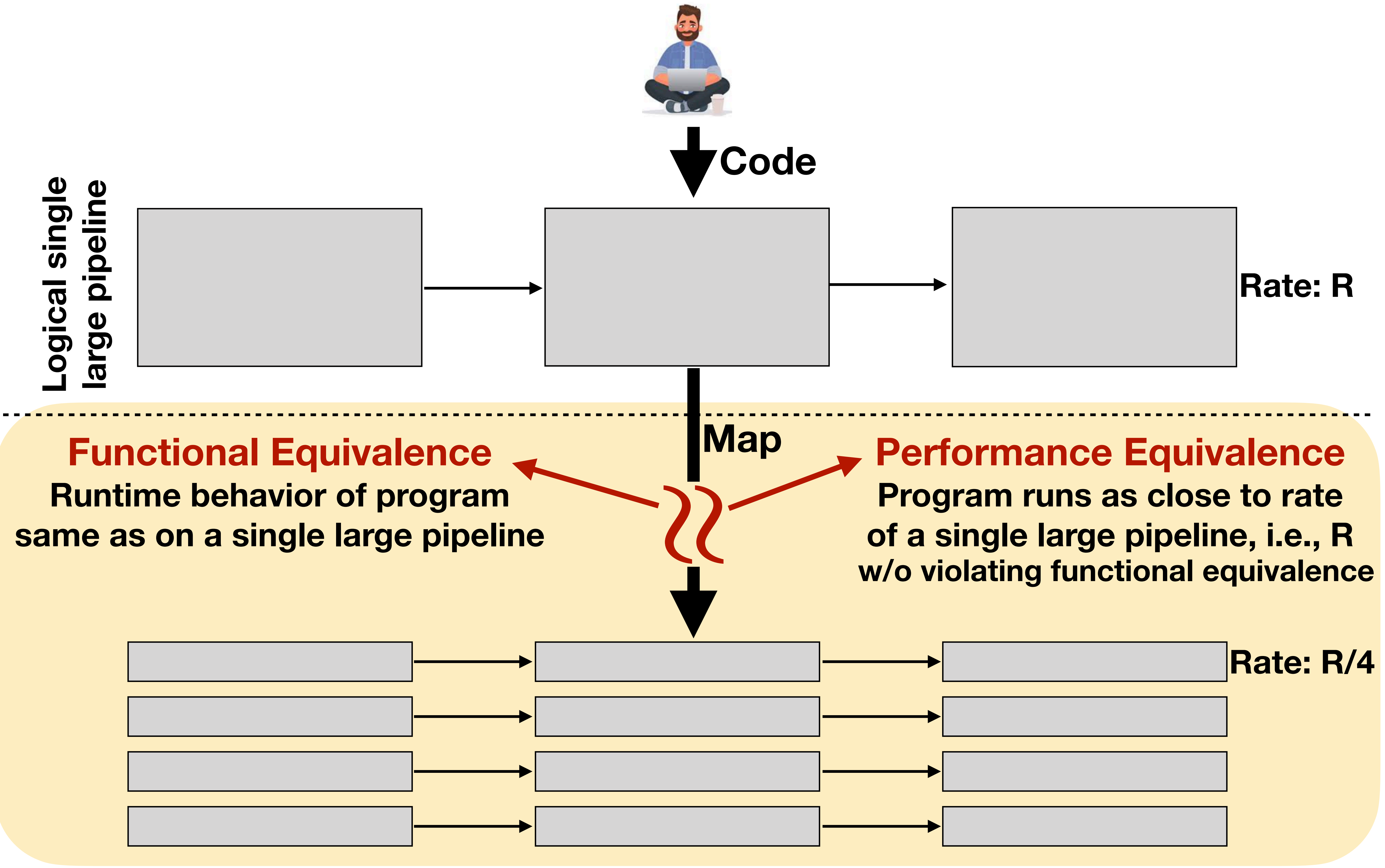

Code
Logical single large pipeline
Rate: R
Map
Functional Equivalence
Runtime behavior of program same as on a single large pipeline
Performance Equivalence
Program runs as close to rate of a single large pipeline, i.e., R w/o violating functional equivalence
Rate: R/4

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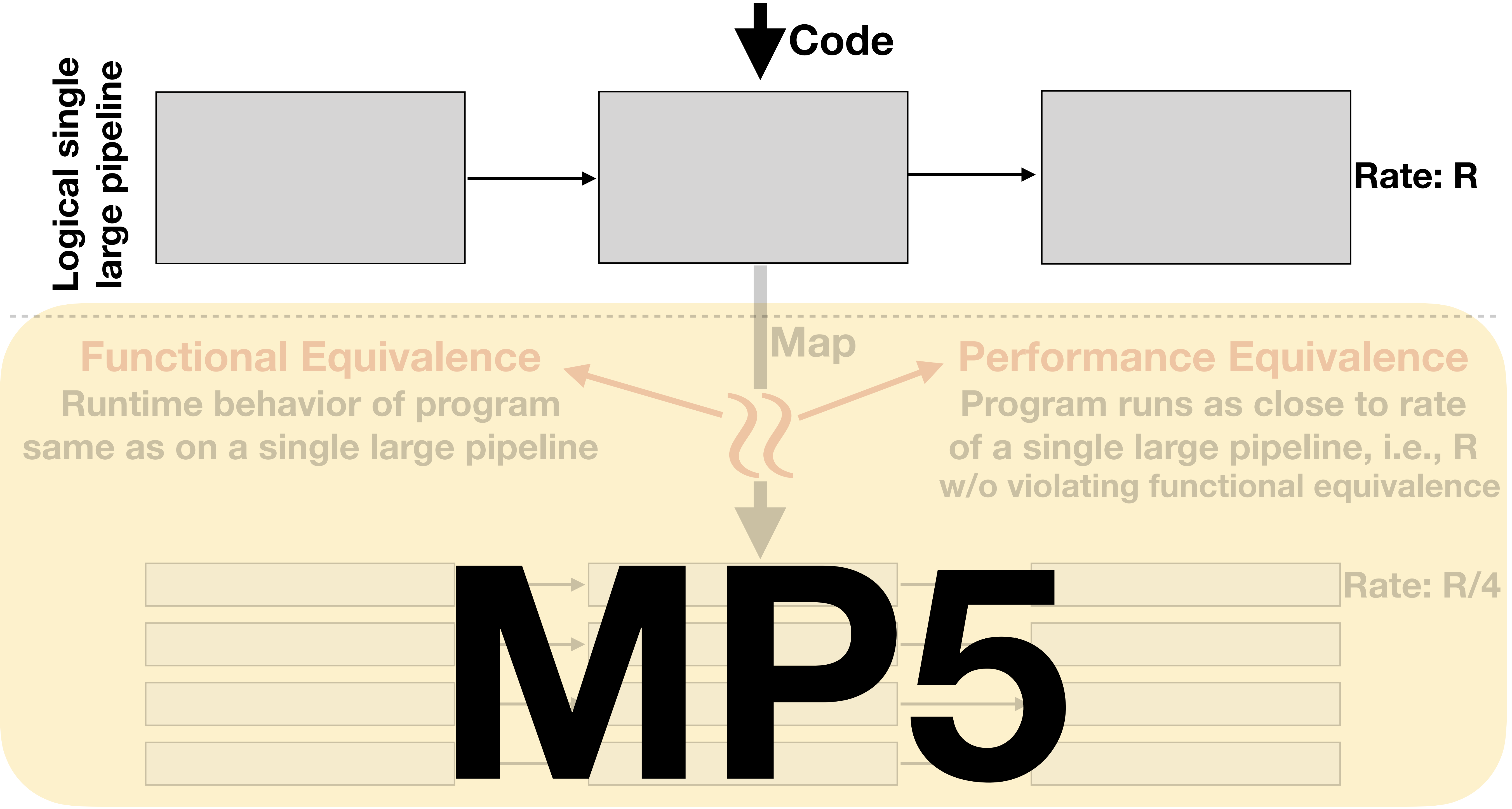

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MP5

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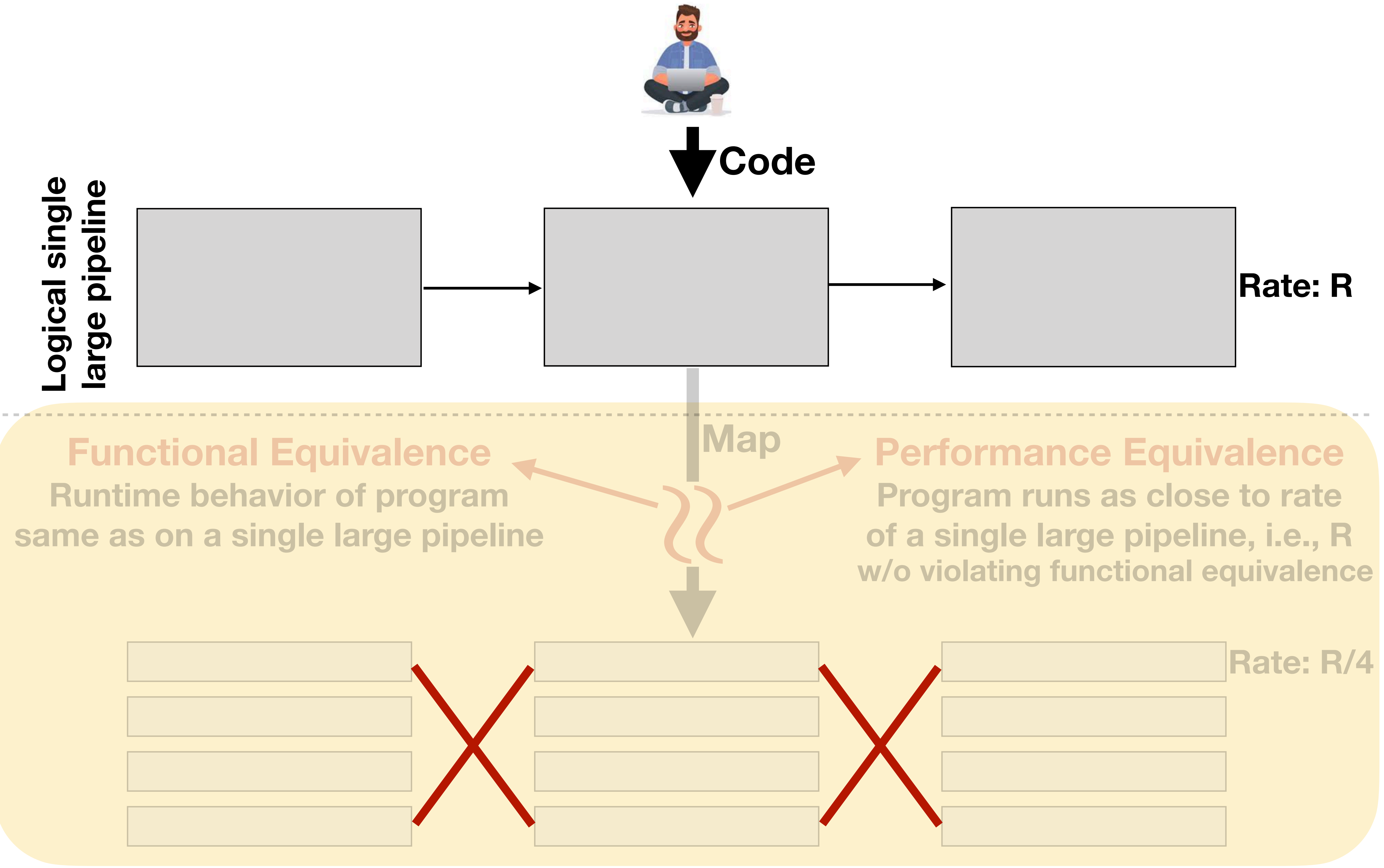
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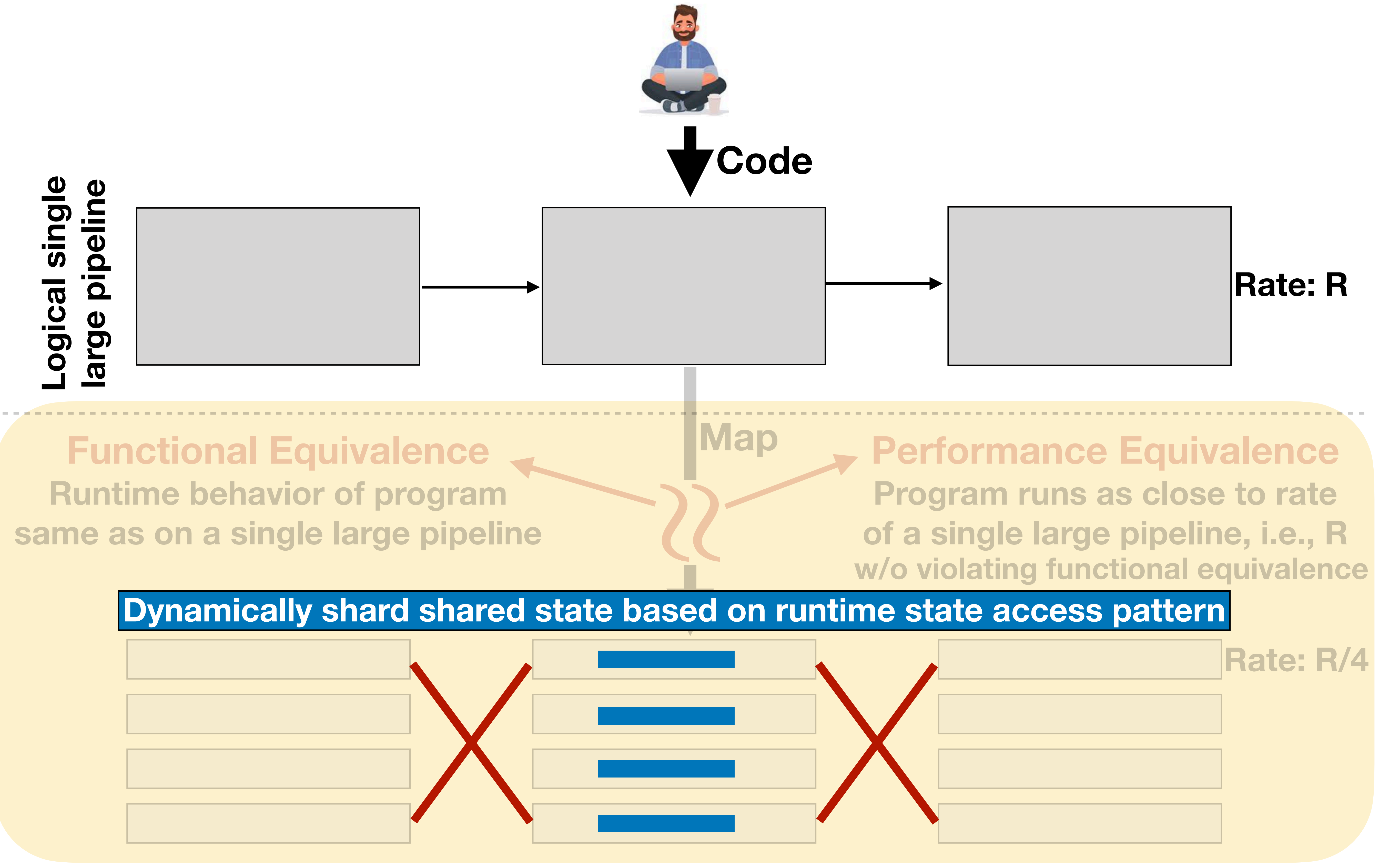
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Dynamically shard shared state based on runtime state access pattern
Rate: R/4

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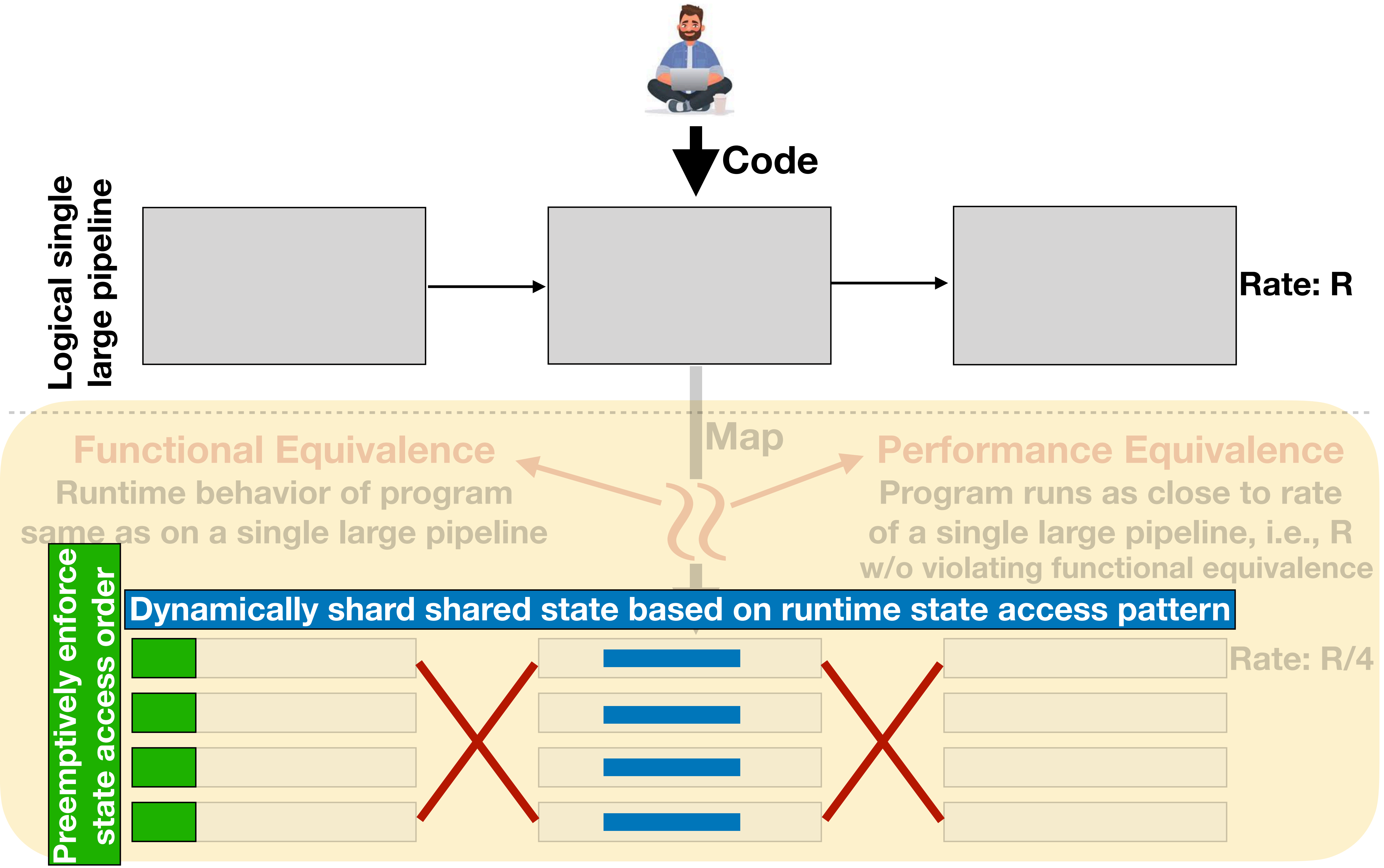
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Preemptively enforce state access order
Rate: R/4

Thank you!