Low Power Static RAM Architectures

- Basic Storage Elements of Semiconductor Memory

```
         ┌───────┐
         │ RAM   │
         └───┬───┘
       ┌─────┴─────┐
   ┌───┴───┐   ┌───┴───┐
   │ SRAM  │   │ DRAM  │
   └───────┘   └───────┘
```
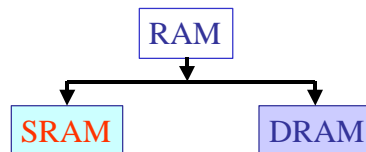
Organization of Static RAM

Memory Core:

The actual storage of information is done here in a two dimensional array. A row is activated by a global line called word line and each column can be accessed individually through bit lines.

Word Decoders:

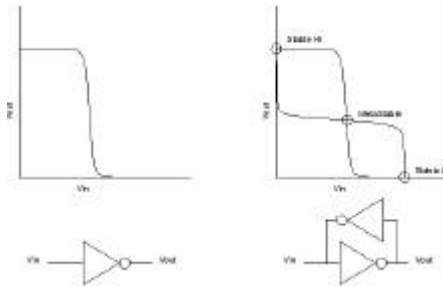Generate word line signals address lines.

Column Decoders:

Select particular bit lines to be connected to sense amplifiers.
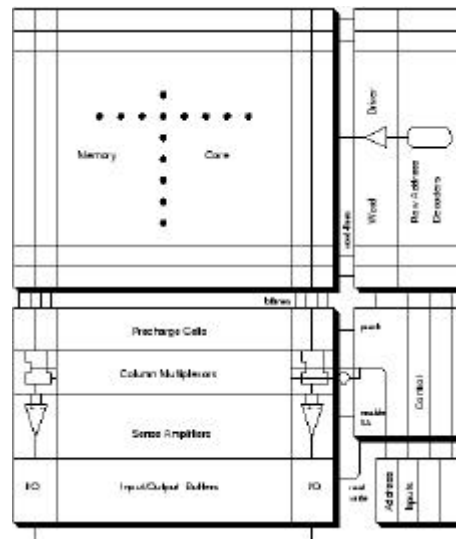
MOS Static RAM Memory Cell

A memory cell is formed
by a pair of inverters in a
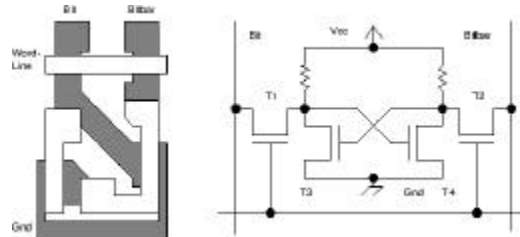closed loop

- 4T SRAM Cell
- 6T SRAM Cell

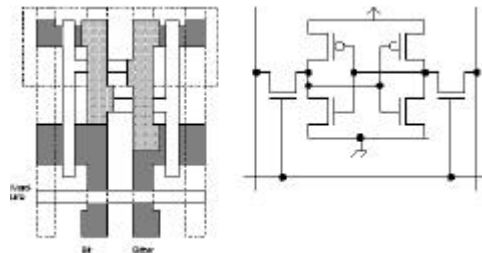Transfer characteristics of an inverter loop

MOS Static RAM Memory Cell

4T SRAM Cell
High degree of compactness
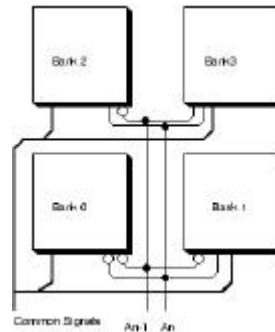High power consumption

6T SRAM Cell
Supply current is limited
to the leakage current of
transistors in the stable
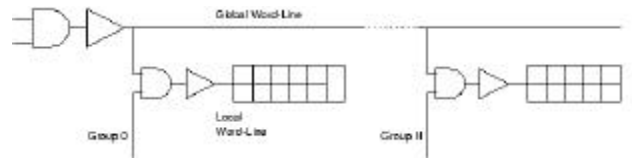state

Banked Organization of SRAM

Targets total switching capacitance to
achieve reduced power and improved speed
   - Additional set of decoders is needed
   - Optimum number of banks can be used
     for best performance.

Divided word line architecture:
   -Word lines are separated in global
   and local word lines.

Reduced Voltage Swings on BIT Lines

A set of sense amplifiers is used to detect
differential voltages developed across bit
lines.
   - Limits voltage swing on bit lines
     and saves power
   - Increases noise sensitivity and
   circuit complexity.
Pulsed Word Lines:
   - Limit bit line voltage
     discharge
   - Does not track the actual
     operation of sense amp.
     Designer needs to estimate
     the actual access time of
     RAM and insert a sufficient
     margin to determine the
     worst case pulse width.
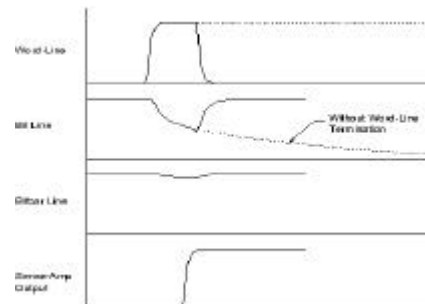
Self-Timing RAM Core

Speed of access to various rows and columns is not identical. Dummy column is used to time the flow of signals through the core. It is an additional column of bit cells, sense amp., and support circuit placed at the side farthest from the word drivers.
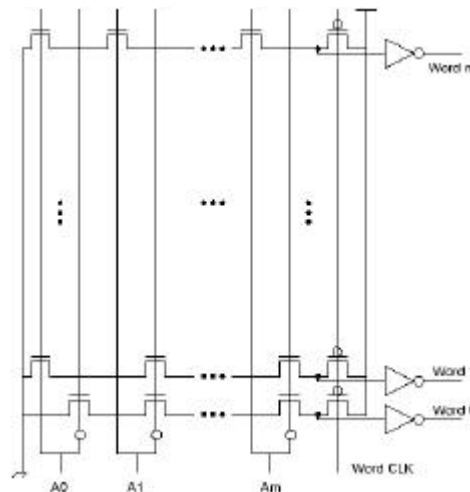
- Adds insignificant overhead to the entire RAM
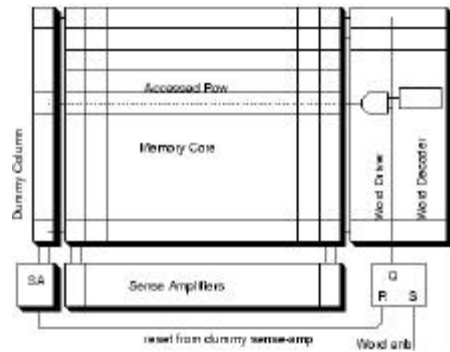
Reducing Power in Write Driver Circuits
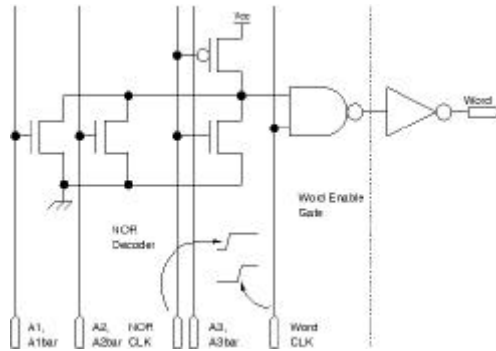
Domino NAND decoder:
- Changes the output of the decoder along one row.
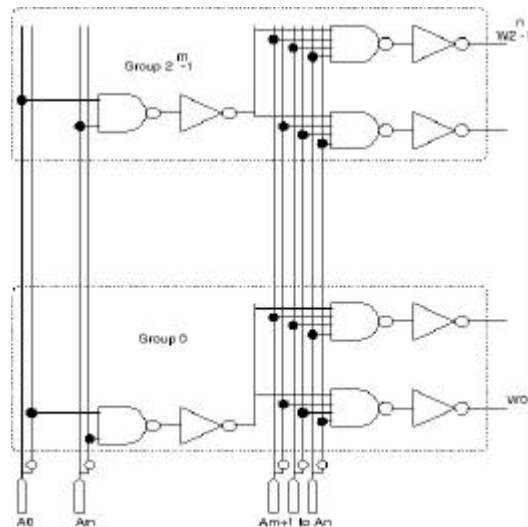- Low power consumption.
- May be slower

Reducing Power in Write Driver Circuits

NOR Decoder:
- Activates the outputs of all but one row.
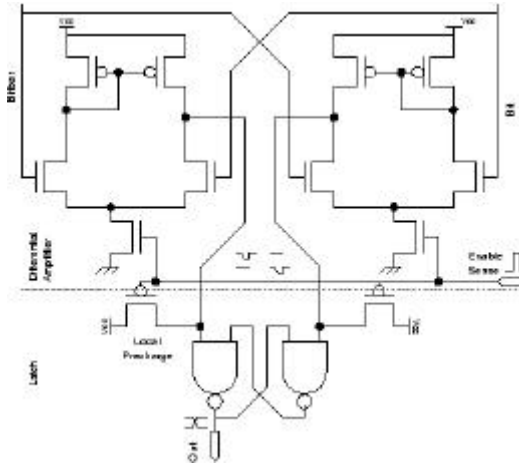- Faster decoding
- High power consumption

Multistage Decoder
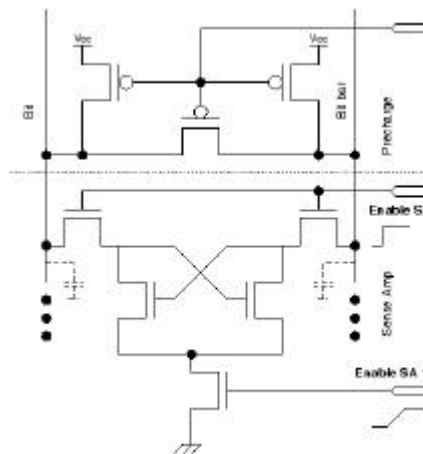
Reducing Power in Sense Amp. Circuits

Differential Sense Amplifier:
- Amplifies small differential bit line voltages into logic levels.
- Limits sense amp currents by precisely timing the activation of the sense amplifier.
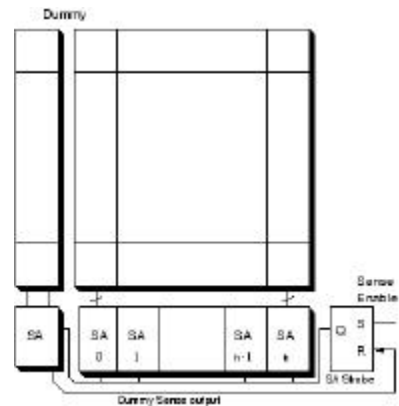

Differential Charge Amplifier

Employs sense amplifiers that automatically cut off after the sense operation.

Self-Timing the Enable for Sense Amp.

The enable sense amplifier signal is used to set up an SR flip-flop in the set state. Once the dummy sense amplifier has finished sensing, it resets the SR flip-flop, which in turn disables the enable for the sense amp.

Latched Sense Amplifier

Self latching sense amp accomplish an automatic limiting of currents after sense. It is a cross coupled amplifying inverter loop, with additional transistors to transfer bit line voltages to the inverter loop.