Deep Sub-micron Test: High Leakage Current and Its Impact on Test; Cross-talk Noise

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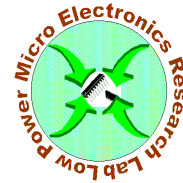


Impact of Leakage on IC Testing?

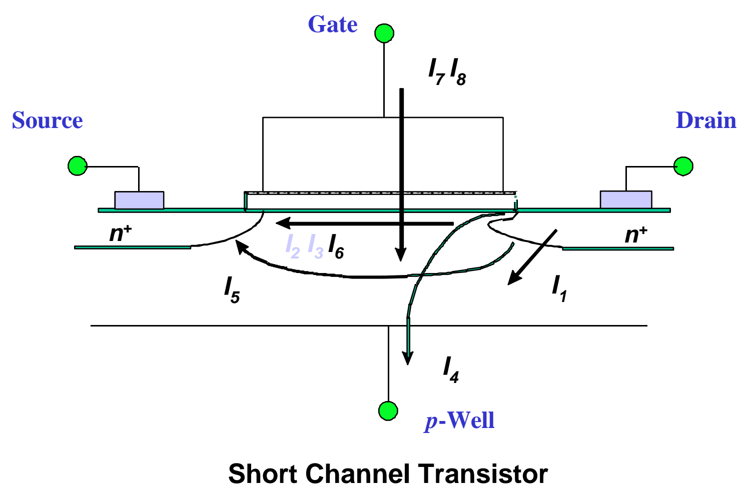
Our Focus

- Higher intrinsic leakage challenges current based test techniques
- I_{DDQ} test method well established and widely accepted for defects and is necessary
- I_{DDQ} testability issue - sensitivity?
- Novel testing solutions

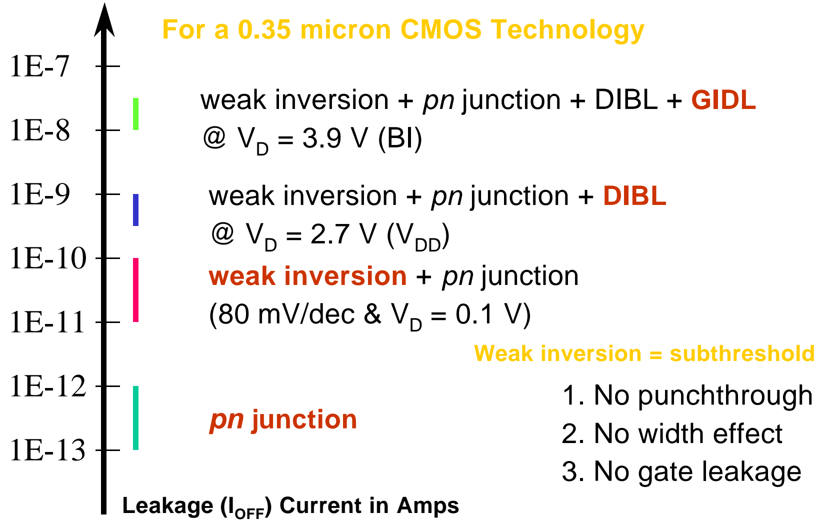
Problem Statement

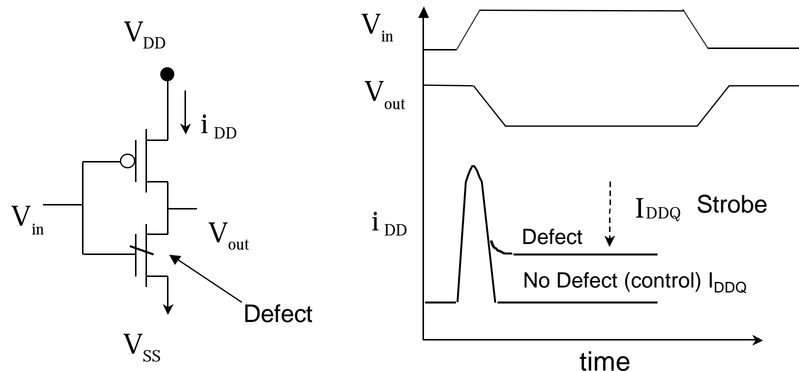
- Can I_{DDQ} and current based test methods be effective and survive the prohibitive increase in intrinsic leakage posed by technology scaling?
- How do we discriminate high speed leaky ICs from defective ones?

Transistor Leakage Mechanisms



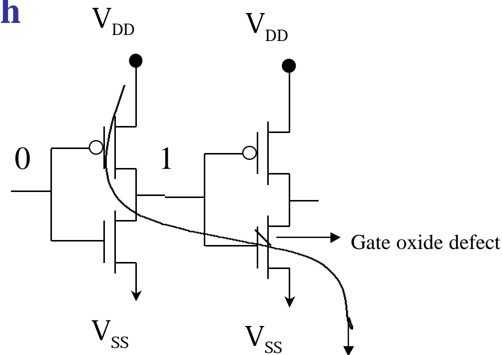
Short Channel Transistor


Components of I_{OFF}
For a 0.35 micron CMOS Technology
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
1E-13
weak inversion + pn junction + DIBL + GIDL
@ V_D = 3.9 V (BI)
weak inversion + pn junction + DIBL
@ V_D = 2.7 V (V_{DD})
weak inversion + pn junction
(80 mV/dec & V_D = 0.1 V)
Weak inversion = subthreshold
1. No punchthrough
2. No width effect
3. No gate leakage
pn junction
Leakage (I_{OFF}) Current in Amps
⇨ Subthreshold Leakage & SCE dominate


I_{DDQ} Testing
✓ Measures current in power supply (V_{DD}) during circuit quiescent state (when all logic states have settled)
V_{DD}
i_{DD}
V_{in}
V_{out}
Defect
V_{SS}
V_{in}
V_{out}
i_{DD}
I_{DDQ} Strobe
Defect
No Defect (control) I_{DDQ}
time
⇨ Choice of input vector matters in complex circuits

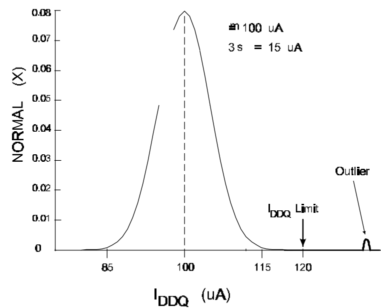
Gate Oxide Defect & I_{DDQ}

- ✓ I_{DDQ} most effective in detecting defects
- ✓ Example: NMOS gate oxide defect creating a V_{DD} to V_{SS} leakage path

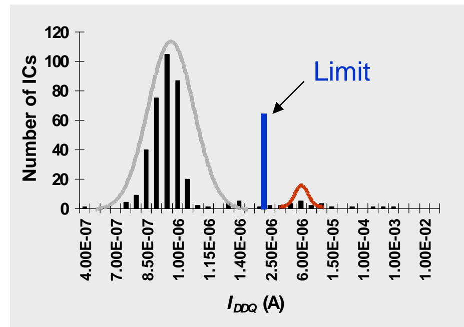


⇨ Circuits become more susceptible to defects with scaling

Single Threshold I_{DDQ} Test Limit



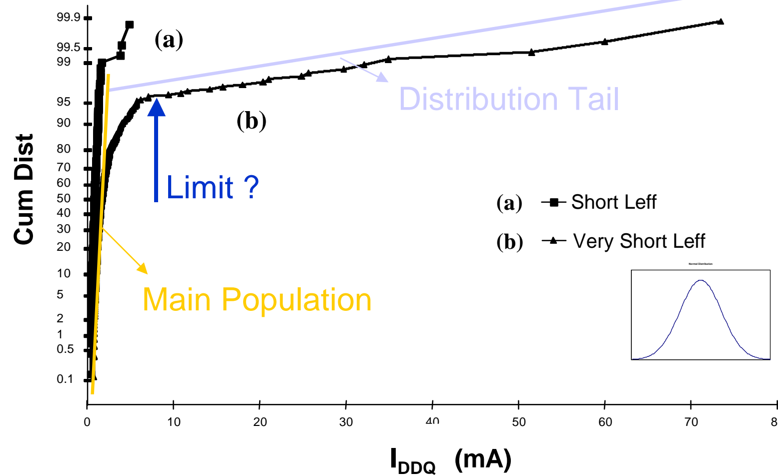
Limit Selection:
1. Quality and Reliability
2. Yield Loss and Cost



Failure Analysis to verify defects and study outliers

μP I_{DDQ} Distributions

Limit concept on cumulative probability plots



State-of-the-art in Current Testing

- Transient Current Testing [1,2]
- Current Signatures and Ratios [3,4]
- Delta I_{DDQ} [5]
- Divide and conquer techniques [6,7]
- Forcing stacked transistors by input vector selection [8]

- Not sufficient to address the problem
- Our solution not in conflict with above

References:

[1] M. Sachdev, et al., “Defect Detection with Transient Current Testing and its Potential for Deep Submicron ICs,” *Int. Test Conf.*, pp. 204-213, Oct. 1999.

[2] E.I. Cole Jr., et al., “Transient Power Supply Voltage (v_{DDt}) Analysis for Detecting IC Defects,” *Int. Test Conf.*, pp. 23-31, Nov. 1997.

[3] A. E. Gattiker et al., “Current Signatures,” VLSI Test Symposium, pp. 112-117, 1996.

[4] P. Maxwell, et al., “Current Ratios: A Self-Scaling Technique for Production IDDQ Testing,” *Proc. of International Test Conference*, pp. 738-746, Oct. 1999.

[5] C. Thibeault, et al., “Diagnosis Method Based on Delta IDDQ Probabilistic Signatures: Experimental Results,” *Int. Test Conf.*, pp. 1019-1026, 1998.

[6] K. Wallquist, “Achieving IDDQ/ISSQ Production Testing with Quic-Mon,” IEEE Design and Test of Computers, Fall 1995.

[7] W. Maly, et al., “Design of ICs Applying Built-in Current Testing,” J. of Electronic Testing: Theory and Applications, pp. 111-120, Dec. 1992.

[8] Y. Ye, et al., “A New Technique for Standby Leakage Reduction in High-Performance Circuits,” *Symp. on VLSI Ckts*, p. 40, June 1998.

Parameters Influencing I_{OFF}, I_{DDQ} & Standby Power

- **Substrate (Body) Bias**
- **Temperature**
- **Lowering Power Supply Voltage**
- **Combined Effects**

I_{OFF} / Leakage Reductions

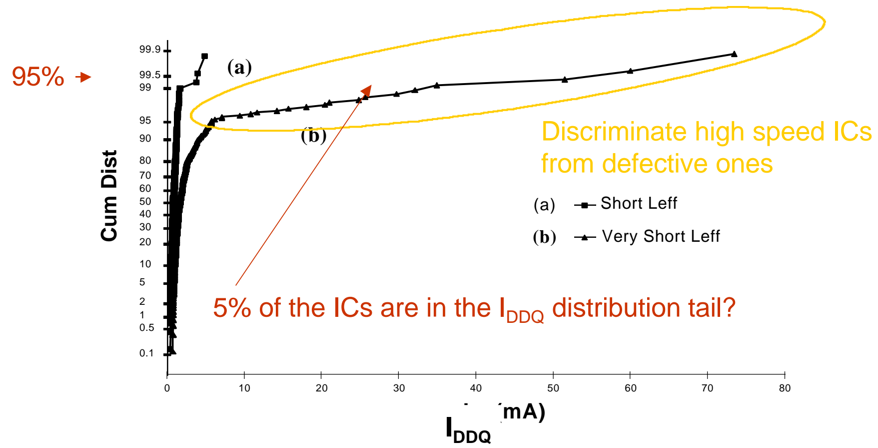
For a 0.35 micron CMOS Technology

- **Temperature**
  - **Factor of ~ 350 from room to -50°C**
- **Substrate backbiasing (RBB) - V_{BS}**
  - **Factor of ~ 3000 at ~ | 2 | V**
- **Lowered V_{DD}**
  - **Factor of ~ 10 from 2.7 V to 1.5 V**
- **Multiple V_T**

Two parameter Test Solution

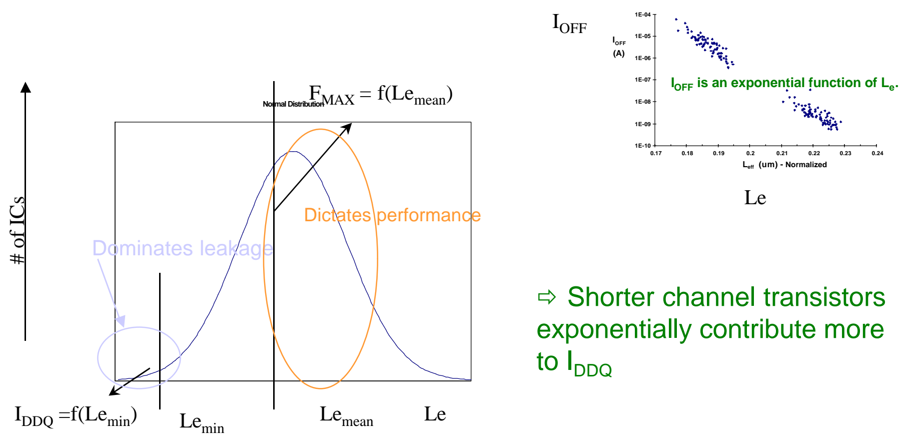
- Scaling
- Functional and Delay Fault Testing
- I_{DDQ}
- Components of transistor leakage
- Leakage reduction techniques
- ➡ Two-parameter test solution
- Sensitivity enhancement by RBB
- Sensitivity enhancement by Temperature

I_{DDQ} tail? Fast or Defective ICs?

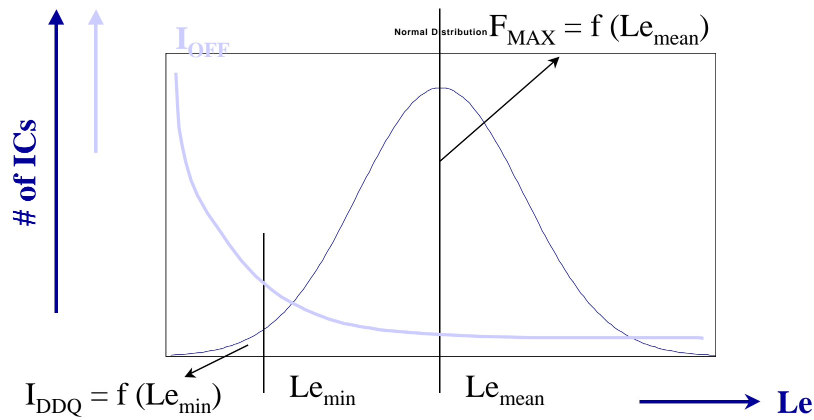


⇨ Intentionally skewed L_{eff} shorter for higher performance

I_{DDQ} and F_{MAX} as a function of L_e

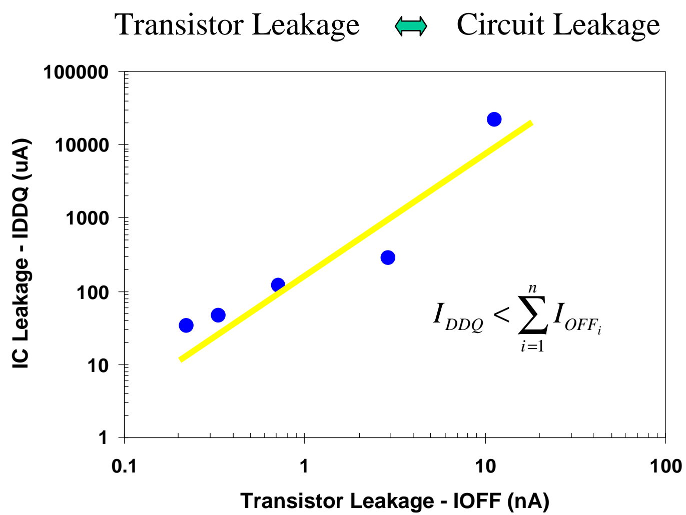


I_{OFF} Current and L_e Distribution

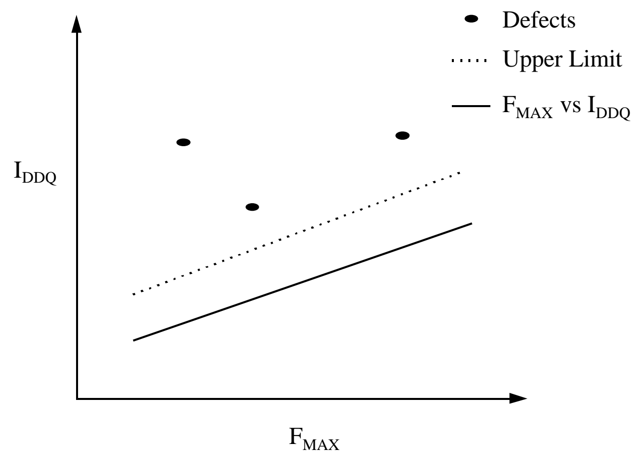


I_{OFF} vs I_{DDQ}

Transistor Leakage ⟺ Circuit Leakage



Two-Parameter Test Concept: Leakage vs Speed

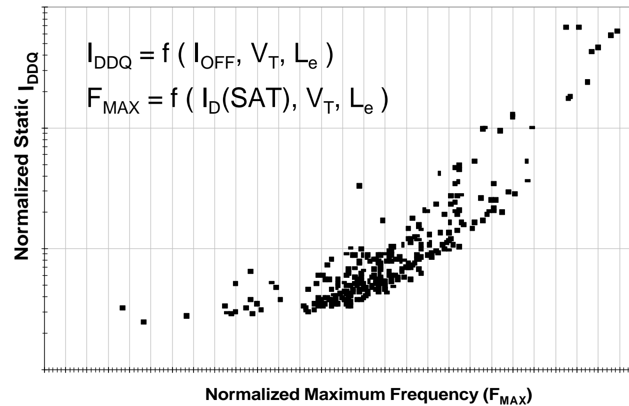


Two-Parameter Test: Decision Table & Adjustable Limit

Table 6.1. IC decision matrix for I_{DDQ} and F_{MAX} testing.

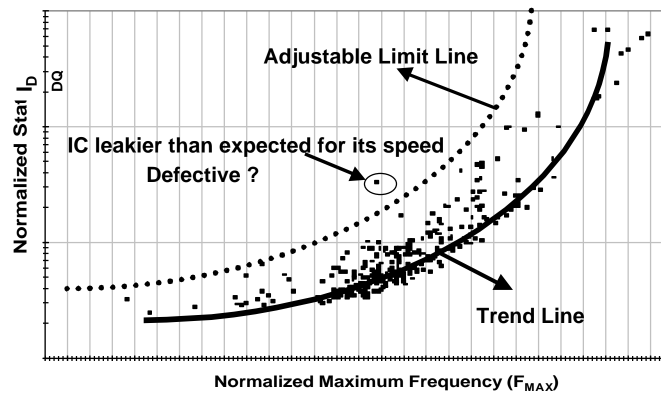
I_{DDQ}	F_{MAX}	**Decision on IC**
H	H	Good - Fast
H	L	Defect
L	H	Unlikely
L	L	Good - Slow

μP Circuit I_{DDQ} vs F_{MAX}



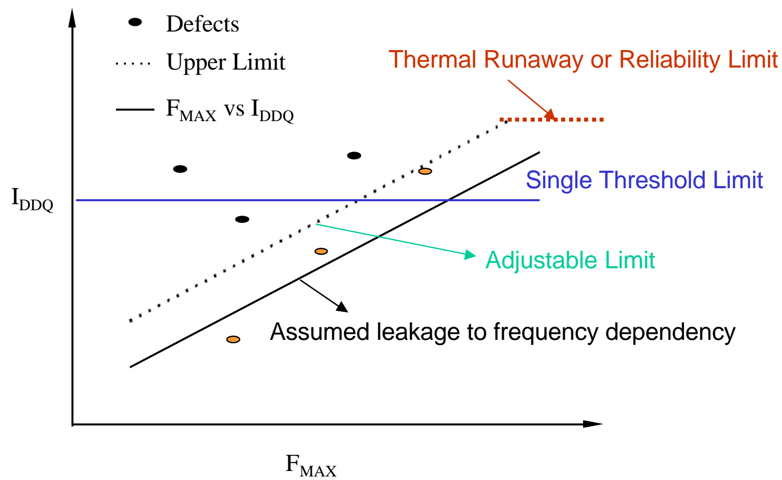
⇨ Empirical relationship derived from existing test methods
⇨ Data include die-to-die parameter variation

Adjustable Limit for I_{DDQ} vs F_{MAX}



⇨ Limit may be established by currently available statistical methods

Two-Parameter Test Practical Limitations



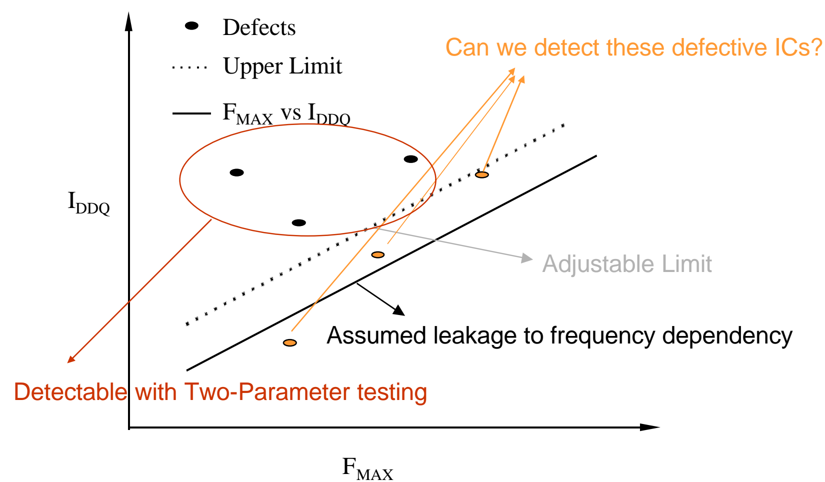
Addressing issues raised by the problem statement

- High intrinsic leakage
  - Our solution places I_{DDQ} in context of F_{MAX}
  - High I_{DDQ} leakage not an issue in itself
  - High leakage at high speed is OK
- I_{DDQ} effectiveness and sensitivity
  - Two-parameter test extends I_{DDQ} effectiveness
  - More on improving sensitivity by RBB
- Discriminates high speed leaky ICs from defective ones

How does our solution compare to state-of-the-art in I_{DDQ} testing?

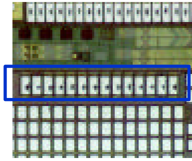
- No extra cost, no new hardware or instrumentation, uses established tests
- It complements the existing methods such as lowering V_{DD}, lowering temperature, and increasing V_T by RBB or multiple V_T

Two-Parameter Test
Leakage in context of Speed

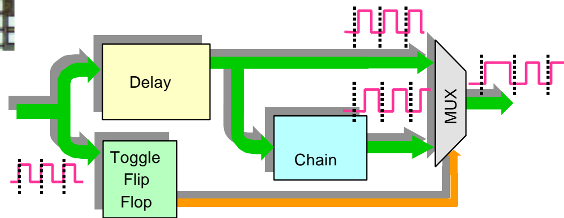


IC Chip Measurements

Delay Chain and RO Circuits

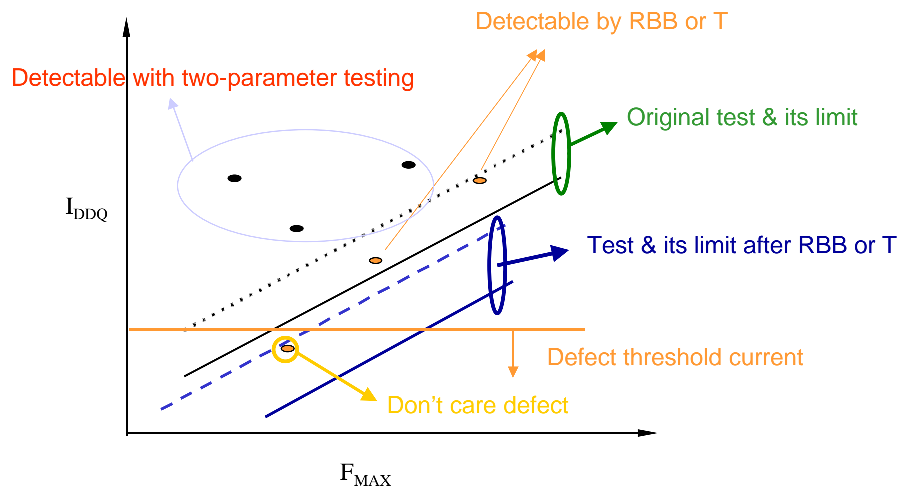


Leakage Current & Power Measurements on an IC with 20,000 transistors

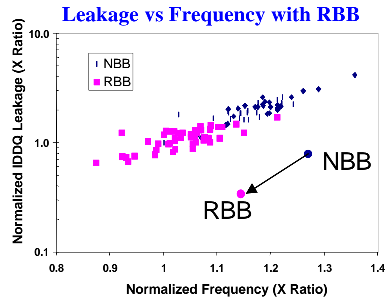


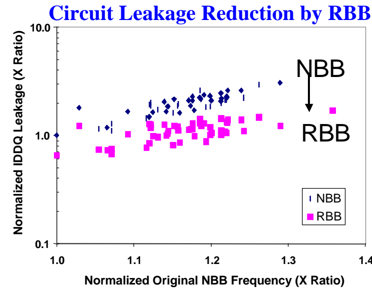
Direct measurement of circuit leakage & delay:
Delay tracks microprocessor clock frequency change in response to transistor performance change

Improving the Sensitivity Two-Parameter Test + RBB and/or T

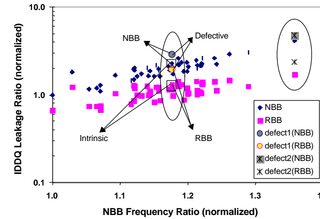


Leakage with RBB





0.5V RBB ⇨ on average leakage ↓ by 1.8X & frequency ↓ by 10%



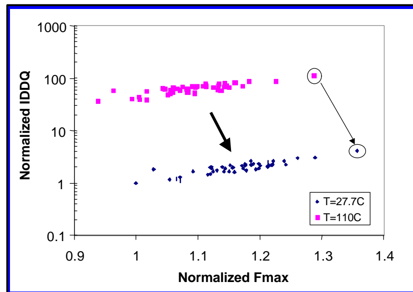
- ⇨ Leakage reduction : intrinsic=1.8X & defective=1.45X
- ⇨ Sensitivity enhanced by 1.8/1.45=1.25X or 25%
- ⇨ 25% improvement not very effective in scaled technologies

S/N Ratio of Two-Parameter Test

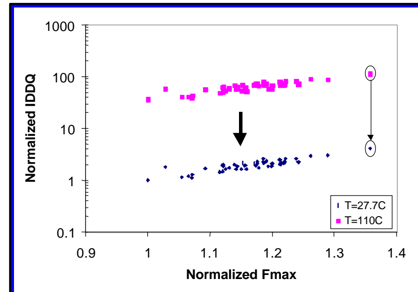
What do we mean by S/N ratio?

- ✓ Signal → defective IC leakage
- ✓ Noise → intrinsic IC leakage

- ⇨ Intrinsic leakage noise is predictable
- ⇨ RBB & T shifts the intrinsic leakage noise
- ⇨ Signal shifts less by RBB or T resulting in widening of spread between S & N



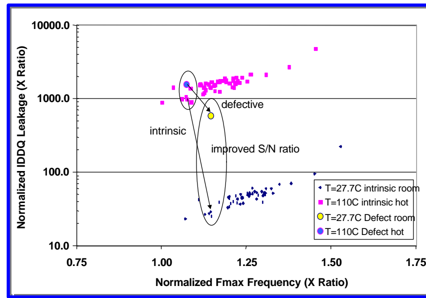
Leakage vs Frequency with T



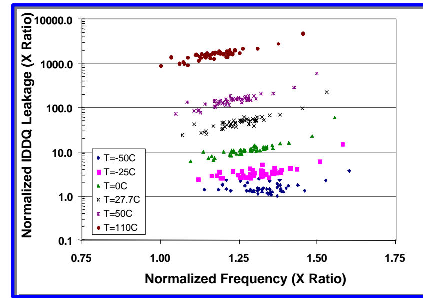
Circuit Leakage Reduction by T

Focus on leakage reduction only

Sensitivity Adjustment



Improving Sensitivity by T



Adjusting Sensitivity

Leakage reduction: intrinsic=36X & defective=2.6X
Sensitivity and S/N ratio enhanced by 36/2.6=13.8X

⇨ **More leakage reduction is possible at a higher cost (Tê)**

Issues in DSM Era

- Signal integrity
- DSM defects
  - capacitive and inductive coupling
  - voltage drop - charge share
  - power supply noise
  - functional/delay faults
- New DSM fault models should support
  - test generation
  - self-test capability
- IDDQ testabilty
- Diagnosis

High Speed Circuit Testing for Cross-Talk Defects

- Crosstalk -- One of the major noise injection mechanisms in DSM circuits
- Determine nodes that are susceptible to these faults in high-speed circuits.
  - Helps to generate the test pattern.
  - Provide guidelines to design noise tolerant circuits

Noise Sources in DSM Circuits

- Cross-talk coupling
- Power supply noise
- Charge redistribution

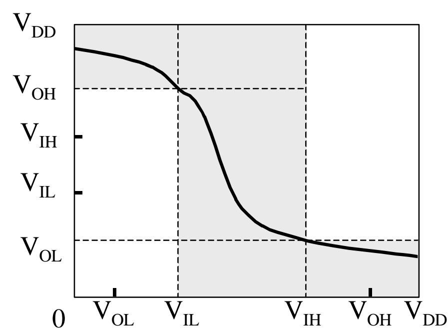
Why Noise Modeling?

- To determine the circuit immunity to noise.
  - Helps in designing noise tolerant circuit.
  - Reduces the number of nodes to be tested.

Static Noise Margin

$NM_L = |V_{IL} - V_{OL}|$

$NM_H = |V_{OH} - V_{IH}|$



Requirement of New Technique

New technique for testing of high-speed DSM monotonic logic circuits

- Dynamic Noise Modeling
  - Static NM - not sufficient
  - Dynamic NM - new metric to check functional violation
- Detection of functional/delay faults in a circuit
  - Estimate propagated noise at a victim node
  - Comparison with dynamic noise margin
- Analysis of noise immunities of high speed circuits

High Speed Circuit Testing for Cross-Talk Defects

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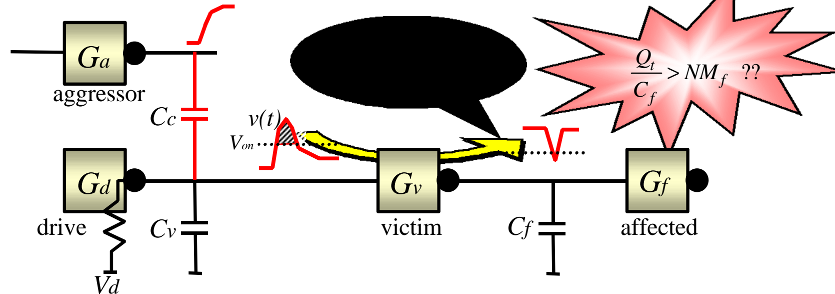
Dynamic Noise Model

$$i_o(v_i) = g_m \times (v_i - V_{on}) \quad : v_i \geq V_{on}$$

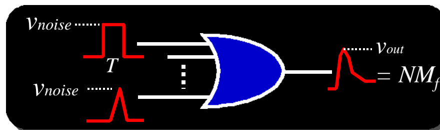
- Linear relation :



$$\frac{NM_f \cdot C_f}{g_m} \quad (volt \cdot sec)$$

- Dynamic noise margin :

Simulation Based Verification

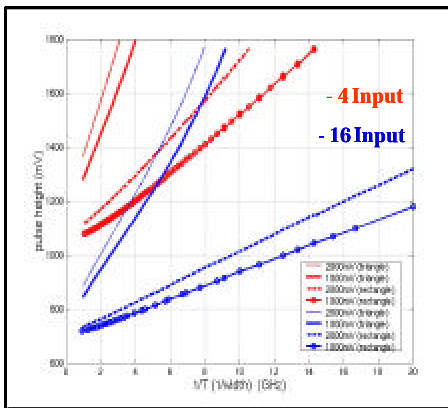


- Domino OR gate

$$\frac{g_m \int (v_{noise} - V_{on}) dt}{C_f} = NM_f$$

$$\Rightarrow (v_{noise} - V_{on}) \cdot T = \frac{NM_f \cdot C_f}{g_m}$$

$$\Rightarrow v_{noise} = \left(\frac{NM_f \cdot C_f}{g_m} \right) \cdot \frac{1}{T} + V_{on}$$



ISO-static NM contour plot

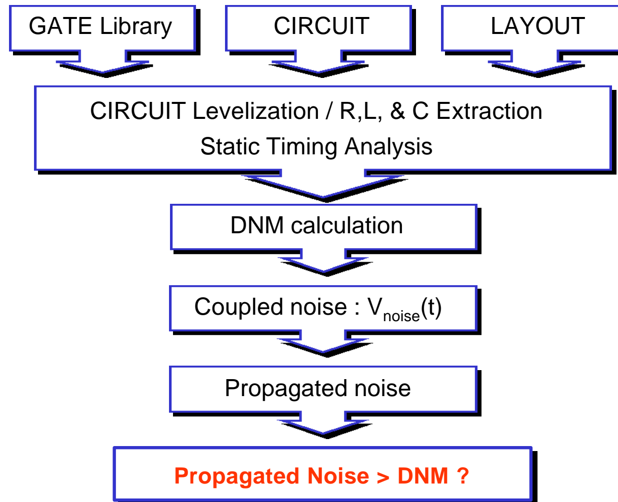
Linearity !

Different gates

with different noise inputs

Testing for Functional Faults

Algorithm:

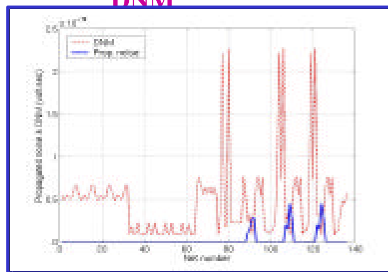


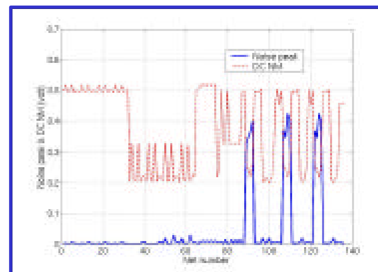
Testing for Functional Faults

A 4 bit full adder circuit is verified

- **Propagated Noise vs. DNM**

Noise Peak vs. DC NM
12 possible fault sites

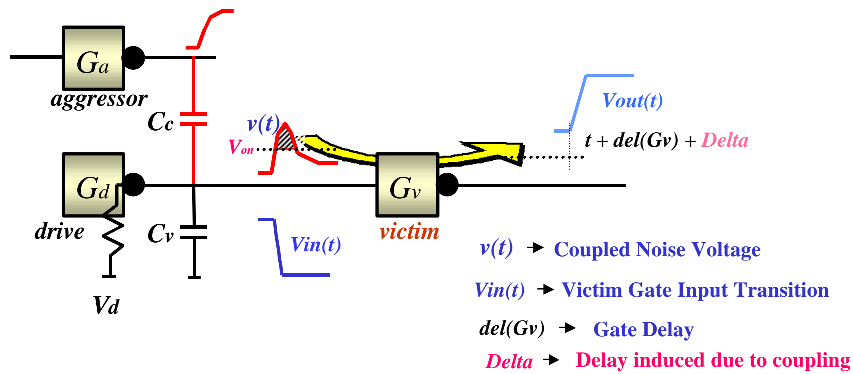




Results are also verified with HSPICE simulation

DNM Based Verification
Can help in reducing the cost for testing.

Delay Faults



C_c can be qualitative measure for delay fault

New layout architecture can help in reducing delay fault probability through C_c minimization

Conclusions

- Two-Parameter test with speed-adjusted leakage limit has a better S/N ratio
- It discriminates high speed leaky ICs from defective ones
- Reverse Body Bias (RBB) enhances the test sensitivity (S/N ratio) modestly
- Temperature improves the sensitivity by more than an order of magnitude (14X)

Conclusions

- Cross-talks faults are becoming increasing important for high-speed DSM circuits
- There is a need for good test and verification methodology for cross-talk defects