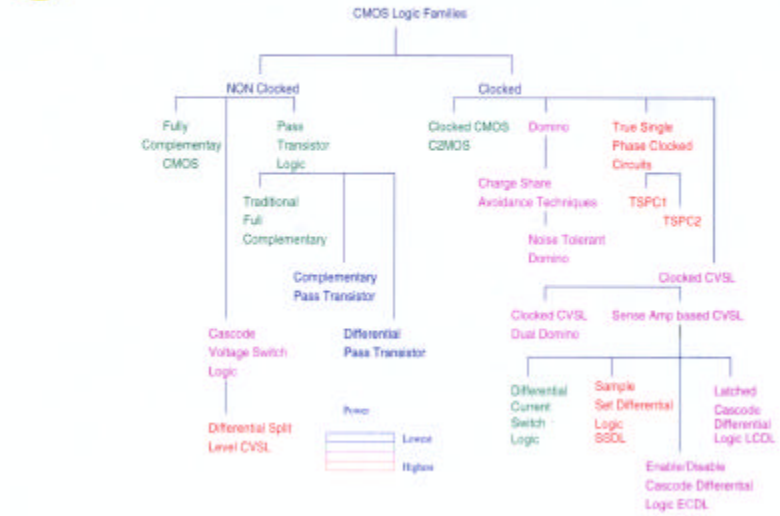
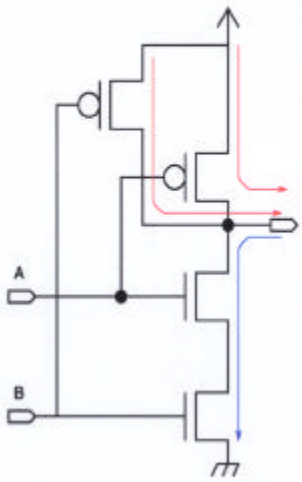
CMOS Logic Families



Fully Complementary CMOS

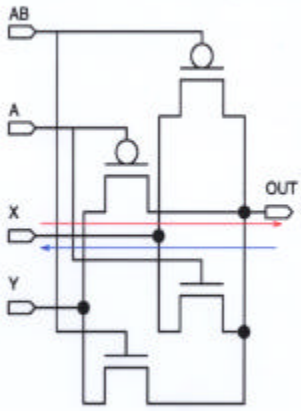


Characteristics

- High Noise Margin
- Low Power
  - Low Activity Factor
- Slower Speed than Domino, CPL type of gates.

Circuit shown implements a NAND Gate.

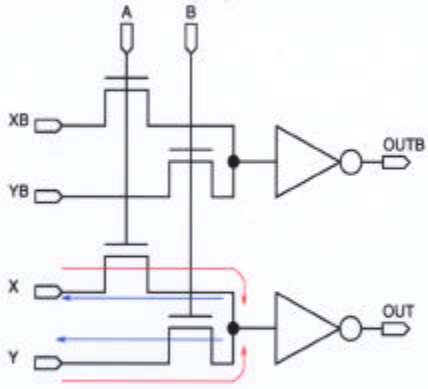
Transmission Gate Logic



Circuit implements a Multiplexor

- Circuit Speed rapidly degrades with increase in the number of levels of logic.
- Logic levels are not degraded, however buffering after a few levels may be required to achieve good speed.
- Input to Input paths may exist.
  - A and AB take on the same value

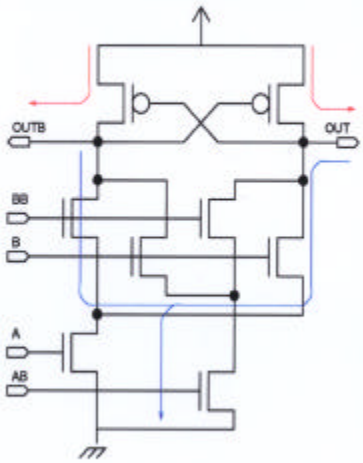
CPL



Complementary Pass Transistor Logic uses NMOS only pass gate structures.

- Always processes complementary inputs and generates complementary outputs
- Logic high levels are degraded at the inputs to the inverter
  - Avoided by using low Vt Pass transistors
  - Level restoration by inverters
- Low Vt Pass transistors degrade Noise margins
- Very Good speed with very low power

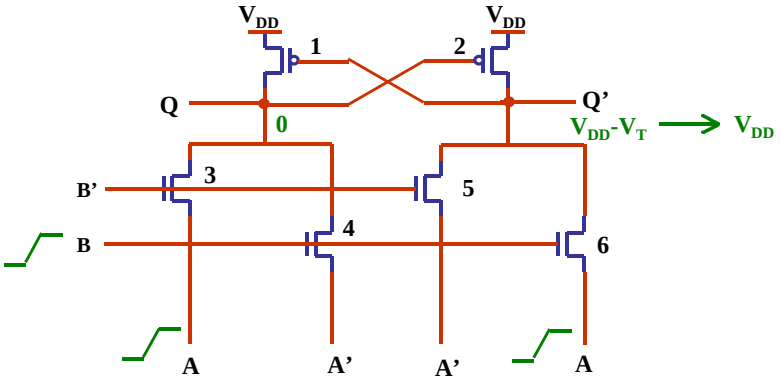
Cascode Voltage Switch Logic



CVSL circuit shown implements an XOR Gate

- NMOS heavy structure capable of implementing complex functionality gates.
- Is slower and consumes more power than other static logic families.
  - PMOS devices fight any change in output state
- Level translation is possible with CVSL. *Output voltage swing can be higher than input voltage swing.*
- Uses complementary inputs and outputs at all times

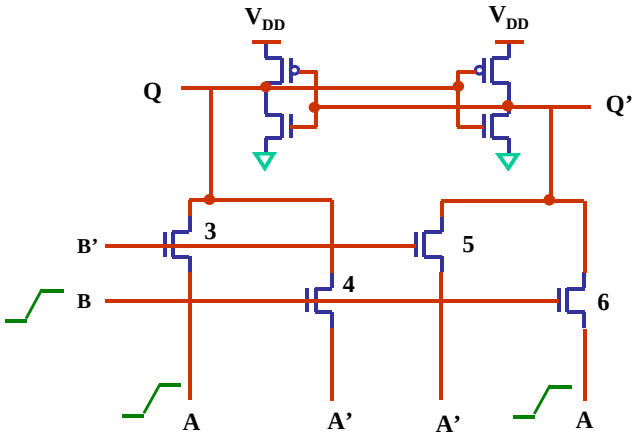
DCVS Logic With Pass Gate (DCVSPG)



- Full Swing
- Area, power reduction
- Differential noise immunity

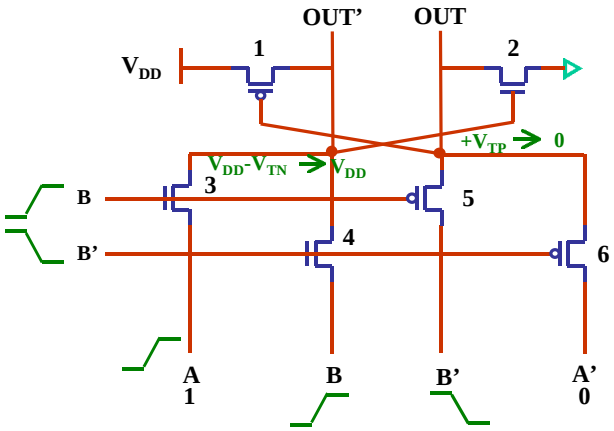
- Limited logical depth
- Body effect

Swing-Restored Pass Gate Logic (SRPL)



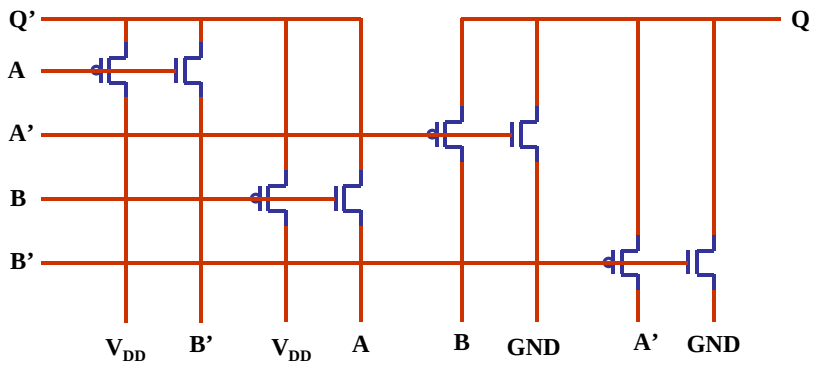
- Low stand-by power
- High design margin, process tolerance
- Less delay via sense-amp action

Push-Pull Pass Transistor Logic (PPL)



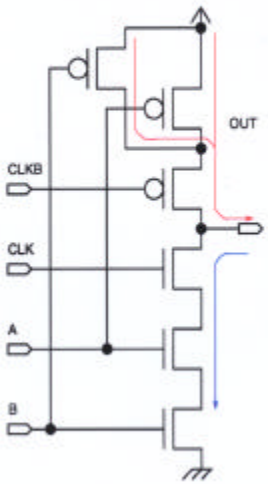
- Push-Pull action, no need for re-buffering
- Low power
- PFET drive dependence

Double Pass-Transistor Logic (DPL)



- High Speed
- Avoids buffer
- Avoids V_T drop
- Redundant device structure

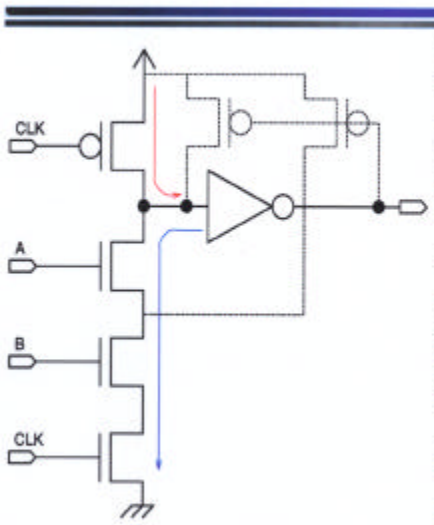
Clocked CMOS C^2MOS



C^2MOS NAND Gate is shown

- Uses complementary clock phases. More than two clock phases are required to effectively pipeline the circuit
- Building block is a tri-state gate. An output holding cell is required to avoid dynamic precharged nodes
- Has high input capacitance because of the presence of both PMOS and NMOS devices.
- Unlike most dynamic logic families it is possible to have low activity at output nodes

Domino Logic

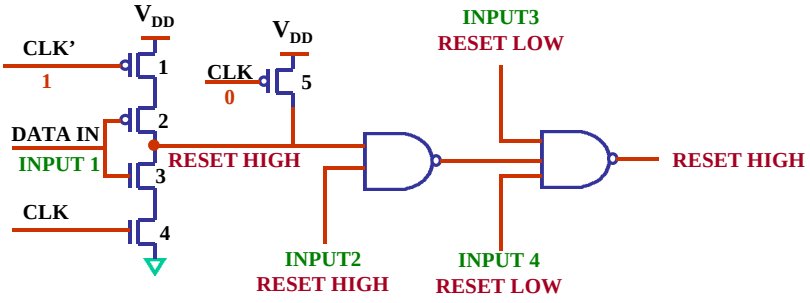


Circuit shown is a two input Domino NAND Gate

Transistors shown in dashed lines are required in practice to avoid charge share and dynamic precharged Nodes

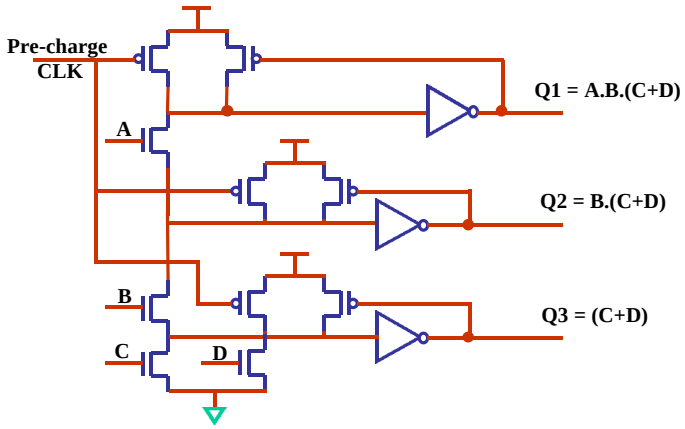
- Allows cascading of gates
- Very efficient pipeline structures can be implemented, by exploiting the fact that the gate senses the last arrival of date or clock
- Fast due to low input capacitance
- Poor noise margin as Vt drops

Pulsed Static Logic (PS-CMOS)

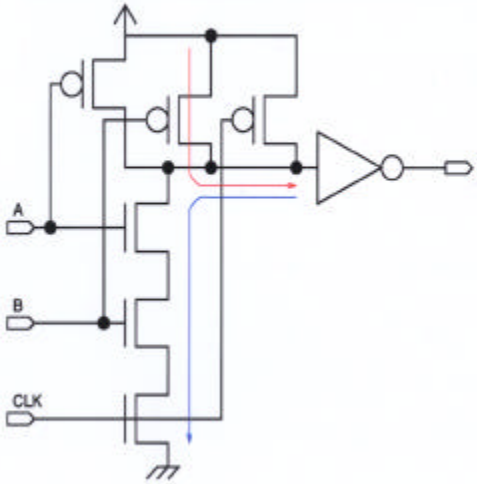


- High performance, skew transitions in a particular direction
- Good dynamic noise immunity
- Static circuit testability
- Cumbersome monotonic stage operation
- Complex clocking

Multiple Output Domino (MODL)



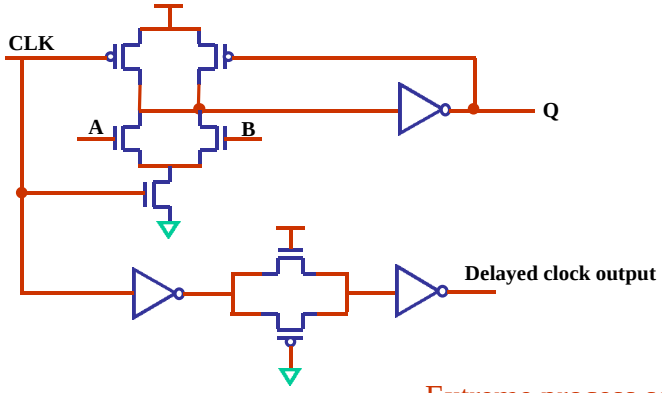
Noise tolerant logic, NTL Domino



Addresses noise issues of Domino

- Hybrid of static CMOS and Domino. PMOS/NMOS width ratio is small unlike FCMOS
- Suitable for low voltage low Vt processes

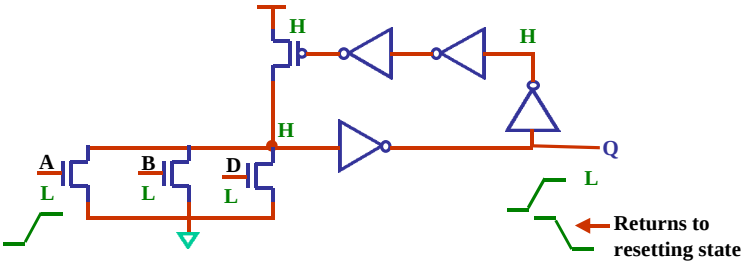
Clock Delayed Domino (CD Domino)



- Capability of inverting functions
- Reduced chip clock overhead

- Extreme process sensitivity
- Timing complexity
- Additional clk propagated with logic

Self Resetting Domino (SR CMOS)

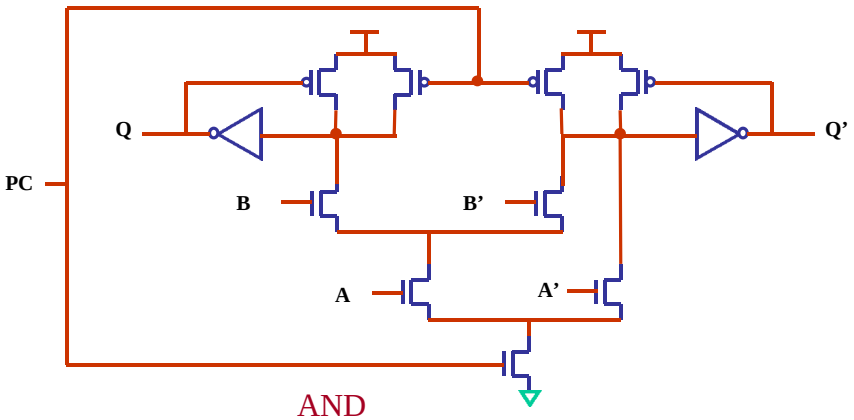


- Own appropriate clocking
- Very high speed
- Reduced clock over-head

- Low noise immunity
- High process sensitivity
- Additional device count
- Difficult to time

Dual Rail Domino

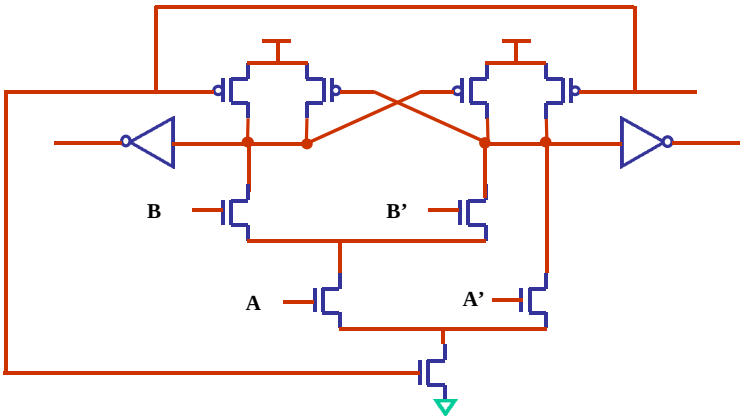
Differential



AND

- Complete logic family

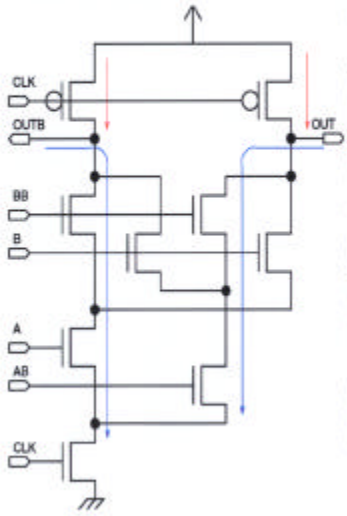
Cross-Coupled Domino



- Logically complete
- Enhanced noise immunity
- High performance

- Higher device count
- Higher clock load
- Higher power

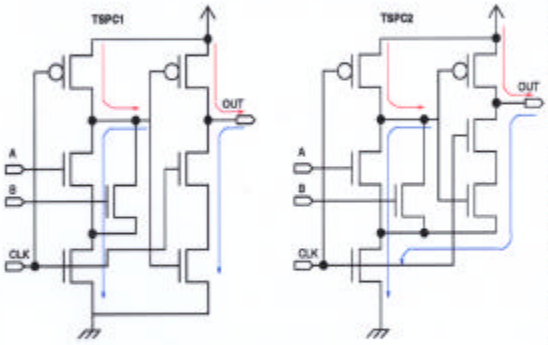
Clocked DCVSL



Clocked DCVS Gate.

- Modified form of the structure is often present as a dual domino gate, by adding inverters at the output.
- Rarely used in the form shown because of the need of multiple clock phases to achieve pipelining
- Useful in the domino form since both true and complementary outputs are generated. Increases complexity but avoids the problem of Domino having non-inverting outputs
- SSDL, ECDL, LCDL add sense amp between the output nodes to improve speed

True Single Phase Clock Logic



Addresses the issue of managing clock skews on multiple clock phases.

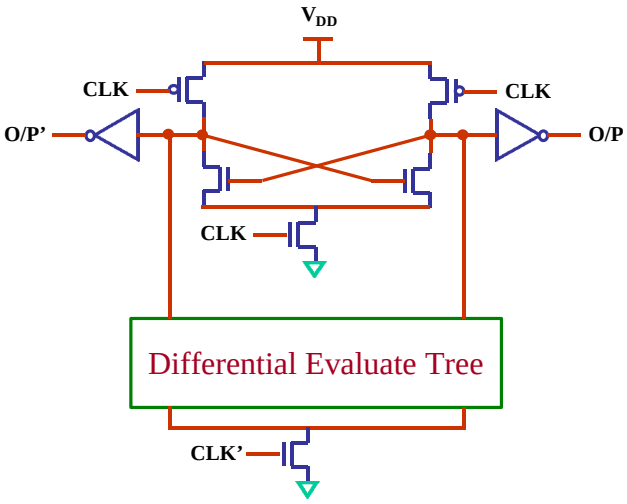
- Uses a single clock phase. Circuit shows integrated OR gate and latch N type TSPC circuit.
- Pipelines are realized by alternating N P TSPC stages
- TSPC2 avoids output glitch of TSPC1
- Dynamic circuit which is very fast. However large clock load causes the circuit to be power hungry

Latched Domino Structure

- Merging of a latch with the load devices of a dynamic logic element

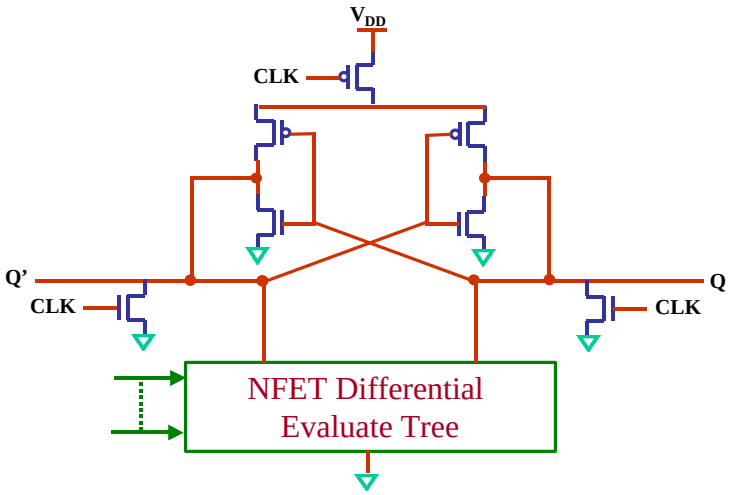
  - Result is fully latched
  - Need for O/P buffer eliminated
  - Tree does not need to complete its transition
  - Sense amplification and additional noise immunity adds design reliability

Sample-Set Differential Logic (SSDL)



CLK = 0 : Sample
CLK = 1 : Differential discharge arrested

Enable/Disable CMOS Differential Logic (ECDL)



CKT disabled until clk transitions low

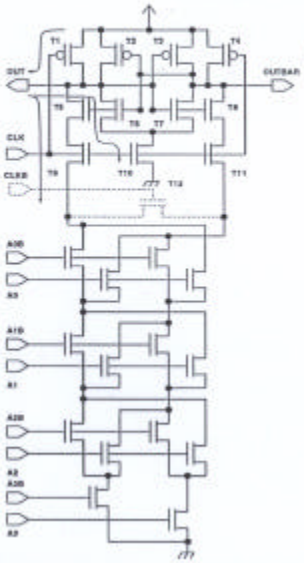
DCSL Features

- Clocked Differential Cascode Voltage Switch Logic style
  - Differential NMOS tree gives gate functionality.
- Capable of implementing High fan-in gates with low delay
  - Gates having fanin between 6 to 18 perform better than comparable domino gates.
- High Complexity gates
  - Allows a reduction in logic depth and number of output nodes (not possible in every case)

DCSL Features (contd.)

- Efficient implementation of XOR based circuits.
  - Arithmetic circuits with lots of XORs benefit the most.
- Achieves low power without sacrificing speed by *restricting the voltage swing of internal nodes*
  - Internal voltage swings are of the order of 0.4volts in a 5volt CMOS process.
- Automatic lock out of inputs once gate evaluation is complete
  - Functionally identical to a latch followed by a combinatorial gate

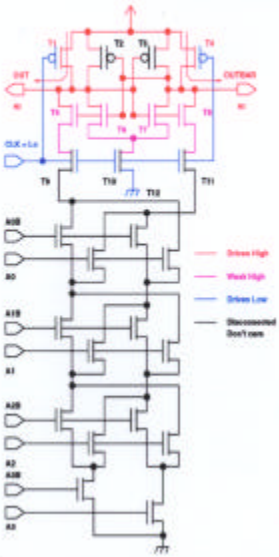
DCSL Circuit Topology



DCSL features are:

- A Clocked Differential Cascode Logic Family
- High Fan-in Gates (Large tree heights)
- High Gate Speed which is substantially independent of gate complexity
- Low Power because of restricted internal node voltage swings
- Automatic lock out of inputs once gate evaluation completes

DCSL Precharged High

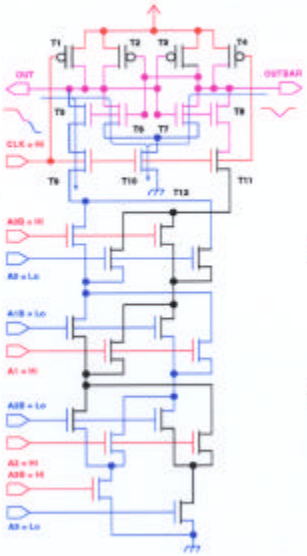


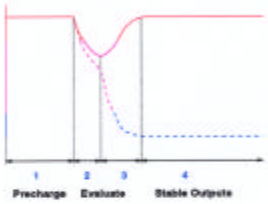
Gate shown is a four input XOR.

Stage 1

- CLK is low.
- Gate outputs are precharged high, through $T1$ and $T4$.

DCSL Evaluate Phase





Stage 2

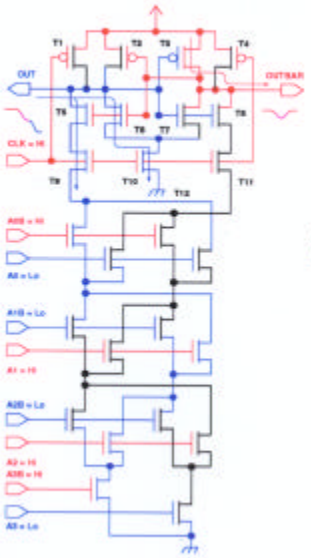
- CLK goes high. $T9$, $T10$, $T11$ turn on.
- Outputs discharge through $T6$/$T7$ and $T10$. With inputs shown an additional path through the NMOS tree exists for OUT. OUT decays faster.

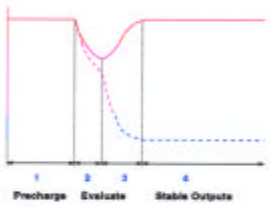
Stage 3

- On crossing the inverter threshold, $T2$, $T3$, $T6$ and $T7$ drive the outputs to the rails due to the strong positive feedback.
- $T8$ turns off since OUT is low and the NMOS tree is disconnected from the rising output.

5

DCSL With Outputs Stable



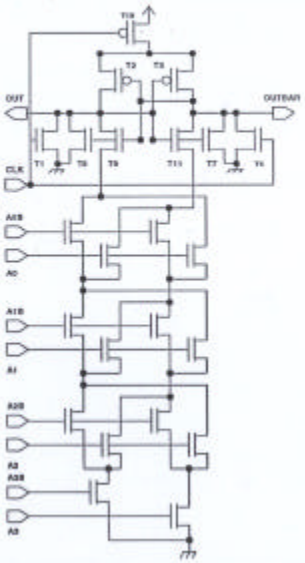


Stage 4

- *CLK* is high, and outputs are stable.
- Outputs are driven strongly. *OUT* is low and *OUTBAR* is high.
- Changes in input do not create any changes in the output.

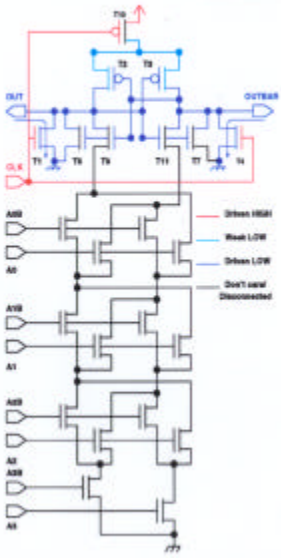
6

Precharged Low DCSL



- This is an alternative form of DCSL
- Circuit works with outputs precharged low
- It is better from the power standpoint as compared to the previous circuit.

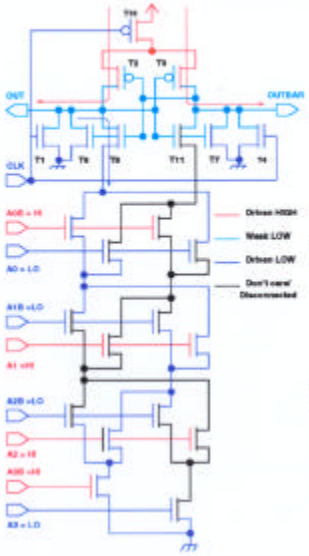
DCSL Precharged Low

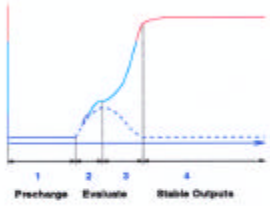


Stage 1

- CLK is high.
- Gate outputs are precharged low, through $T1$ and $T4$.

DCSL Evaluate Phase





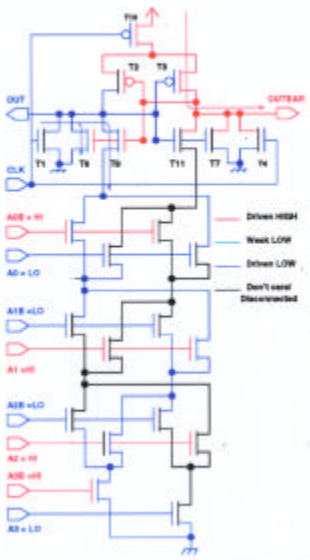
Stage 2

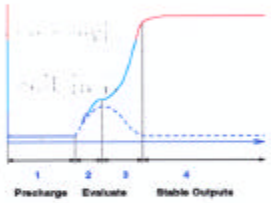
- CLK goes low. $T10$ goes on. $T1$ and $T4$ go off.
- Outputs charge towards $V_C C$ through $T2/T3$ and $T10$. OUT is held low by the NMOS tree while $OUTBAR$ charges.

Stage 3

- On crossing the inverter threshold, $T2$, $T3$, $T6$ and $T7$ drive the outputs to the rails due to the strong positive feedback.
- $T11$ turns off since OUT is low and the NMOS tree is disconnected from the rising output.

DCSL With Outputs Stable





Stage 4

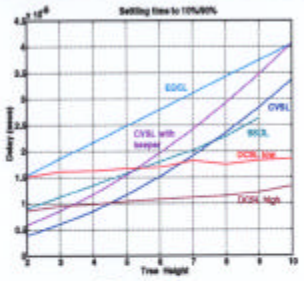
- *CLK* is low, and outputs are stable.
- Outputs are driven strongly. *OUT* is low and *OUTBAR* is high.

Results

A comparison of DCSL with similar logic families has been carried out.

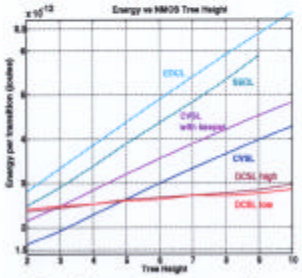
- An XOR tree similar to that shown previously is used.
- Comparison is with respect to circuit in the absence of $T9$ and $T11$. Circuits compared are
  - DCSL precharged high is similar to "Sample Set Differential Logic" SSDL.
  - DCSL precharged low is similar to "Enable Disable Cascode Logic" EDCL.
  - Clocked DCVS with and without a "keeper" P transistor.

Results



Gate Delay

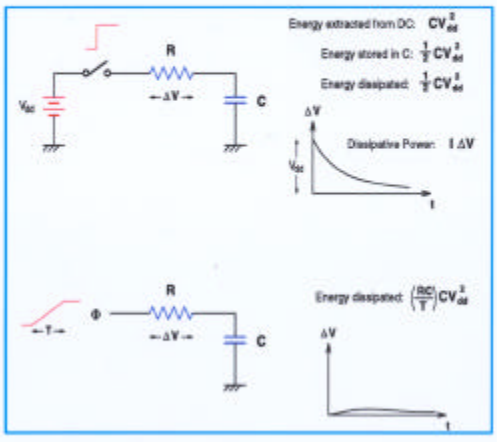
- Gate performance is better than most DCVS logic families and Domino at higher tree heights.
- Gate power consumption is also lower.



Gate Energy Consumption

- Newer version of the gate is robust. When used in the critical path of a domino adder it improves the delay by 20% at the same power consumption.

Adiabatic Switching Concept



3c)

$$RC\left(\frac{dV_c}{dt}\right) + V_c = \Phi$$

$$\Phi = \begin{cases} 0 & t < 0 \\ \left(\frac{V_{dd}}{T}\right)t & 0 \le t < T \\ V_{dd} & t \ge T \end{cases}$$

The solution of the above equation is given by

$$V_c = \begin{cases} 0 & t < 0 \\ \Phi - \left(\frac{RC}{T}\right)V_{dd}(1 - e^{-t/RC}), & 0 \le t < T \\ \Phi - \left(\frac{RC}{T}\right)V_{dd}(1 - e^{-T/RC})e^{-(t-T)/RC} & t \ge T \end{cases} \tag{7.2}$$

The energy dissipation in the above charging process can be calculated as follows:

$$E_{source} = \int_0^\infty iV_R\,dt = \int_0^T iV_R\,dt + \int_T^\infty iV_R\,dt \tag{7.3}$$

The first term of Eq. (7.4) can be written as

$$\begin{aligned} \int_0^T iV_R\,dt &= \int_0^T \frac{(\Phi - V_c)^2}{R}\,dt \\ &= \int_0^T \frac{\left[(V_{dd}/T)RC(1 - e^{-t/RC})\right]^2}{R}\,dt \\ &= \frac{R^2C^2}{T^2}CV_{dd}^2\int_0^{T/RC}(1 - e^{-t/RC})^2\,d\left(\frac{t}{RC}\right) \\ &= \left(\frac{RC}{T}\right)CV_{dd}^2\left[1 - \frac{3}{2}\left(\frac{RC}{T}\right) + 2\left(\frac{RC}{T}\right)e^{-T/RC} - \frac{1}{2}\left(\frac{RC}{T}\right)e^{-2T/RC}\right] \end{aligned}$$

And the second term can be written as

$$\begin{aligned} \int_T^\infty iV_R\,dt &= \int_T^\infty \frac{(\Phi - V_c)^2}{R}\,dt \\ &= \frac{RC}{T^2}CV_{dd}^2(1 - e^{-T/RC})^2\int_T^\infty e^{-2(t-T)/RC}\,dt \\ &= \left(\frac{RC}{T}\right)^2 CV_{dd}^2\left[\frac{1}{2}(1 - e^{-T/RC})^2\right] \end{aligned}$$

Finally we have

$$E_{source} = \left(\frac{RC}{T}\right)CV_{dd}^2\left(1 - \frac{RC}{T} + \frac{RC}{T}e^{-T/RC}\right) \tag{7.4}$$

Let us consider the two extreme cases. When $T \gg RC$,

$$E_{source} = \left(\frac{RC}{T}\right)CV_{dd}^2 \tag{7.5}$$

and when $T \ll RC$

$$\begin{aligned} E_{source} &= \left(\frac{RC}{T}\right)CV_{dd}^2\left\{1 - \frac{RC}{T} + \frac{RC}{T}\left[1 - \frac{T}{RC} + \frac{1}{2}\left(\frac{T}{RC}\right)^2\right]\right\} \\ &= \frac{1}{2}CV_{dd}^2 \end{aligned} \tag{7.6}$$