Advanced VLSI Design (EE 695K)

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Course Outline

- Scaling
- Process variation
- High Performance Design
  - High performance logic families, clocking strategies, interconnects
- Low-Power Design
  - Power estimation, low voltage designs, leakage estimation and leakage control techniques, circuit/device/technology issues, high level design
- Algorithm and architecture level optimization
- VLSI signal processing
  - Multipliers and adders, scheduling and binding of datapaths, low power designs, re-configurable DSP
- Logic synthesis

Exam and Project

- One mid-term exam (30% of overall grade)
- Project – due at the last day of class (70%)
  - Innovative design (publishable quality)
  - Circuit design, algorithms, architecture, interconnects – power, performance, noise
  - Project presentation
- CAD tools – Cadence and Synopsys

Text

Low Power CMOS VLSI Circuit Design, K. Roy & S. Prasad, John Wiley.

Design of High-Performance Microprocessor Circuits, A. Chandrakasan, Bowhill, & Fox, IEEE Press

Class notes

Technology Scaling

Technology scaling improves:

Transistor performance
Transistor density
Energy consumed per switching transition

0.7X scaling factor (30% scaling) results in:

30% gate delay reduction (43% freq.)
2X transistor density increase (49% area)
Energy per transition reduction

Technology Scaling

- Speed & Performance
  - High drive current and low parasitics
  - Low gate delay and high frequency
- Density & Area
  - Small feature size
- Power & Reliability
  - Low power supply voltage
  - Low off-state leakage

Technology Generation Scaling

$$Dimensions \xrightarrow{scale} 0.7,\ V_{dd} \xrightarrow{scales} \beta,\ V_t \xrightarrow{scales} \beta$$

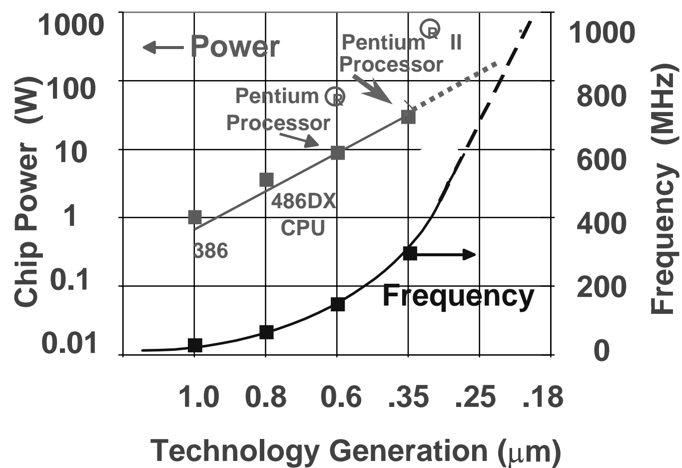
$$I = \frac{kW}{T_{ox}}(V_{dd} - V_t) \xrightarrow{scales} \frac{0.7}{0.7} \times \beta = \beta$$

$$D = \frac{CV_{dd}}{I} \xrightarrow{scales} \frac{0.7 \times \beta}{\beta} = 0.7 \quad \text{(30\% delay reduction)}$$

$$E = CV_{dd}^{\ 2} \xrightarrow{scales} 0.7\beta^{\ 2}$$

IC Frequency & Power Trends

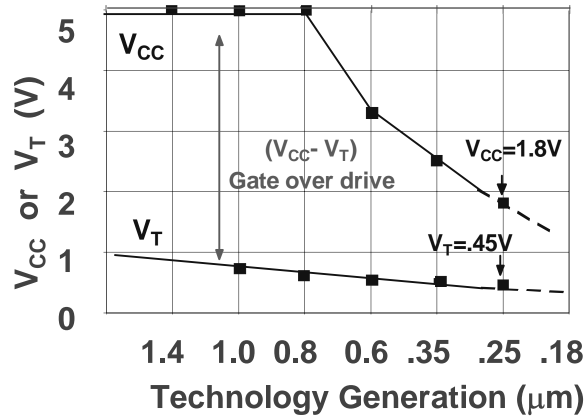
- Clock frequency improves 50%
- Gate delay improves ~30%
- Power increases 50%
- Power = $C_L V^2 f$



Active switched capacitance "C_L" is increasing.

Constant Voltage vs Field Scaling

- Recently: constant e-field scaling, aka voltage scaling
- V_{CC} 1V
- V_{CC} & modest V_T scaling
- Loss in gate overdrive (V_{CC}-V_T)



Voltage scaling is good for controlling IC's active power, but it requires aggressive V_T scaling for high performance

Barriers to Voltage Scaling

Voltage Scaling = Constant Electric Field Scaling
Voltage scaling is good for IC's active power, but degrades gate over drive. Requires V_T scaling.

Leakage power

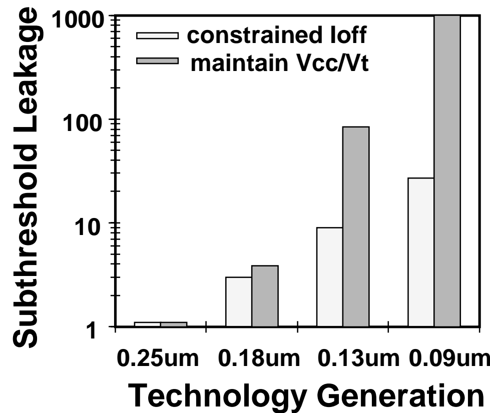
Short-channel effects

Special circuit functionality, noise

Soft error

Parameter variation

Barriers to Voltage Scaling



- Leakage power
- Short-channel effects
- Soft error
- Special circuit functionality

Delay

$$\tau_d = \frac{C_L V_{DD}}{I_D}$$

$$\tau_d = \frac{C_L}{(\frac{W}{2L})\mu C_{ox} V_{DD} (1 - \frac{V_T}{V_{DD}})^2}$$ Long Channel MOSFET

$$\tau_d = \frac{C_L}{W C_{ox} \upsilon_{SAT} (1 - \frac{V_T}{V_{DD}})}$$ Short Channel MOSFET

$$\tau = \frac{C L^{0.5} T_{ox}^{0.5}}{V_{DD}^{0.3} (0.9 - V_T / V_{DD})^{1.3}} \left(\frac{1}{W_n} + \frac{2.2}{W_p}\right)$$ [1]

[1] C. Hu, "Low Power Design Methodologies," Kluwer Academic Publishers, p. 25.

Performance significantly degrades when V_{DD} approaches $3V_T$.

V_T Scaling: V_T and I_{OFF} Trade-off

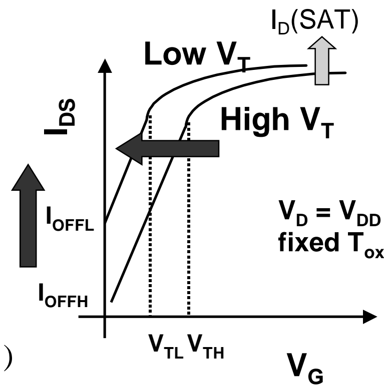
Performance vs Leakage:

V_T I_{OFF} $I_D(SAT)$

$$I_{OFF} \propto I_{subth} \propto \frac{W_{eff}}{L_{eff}} K_1 e^{(V_{GS}-V_T)}$$

$$I_D(SAT) \propto \frac{W_{eff}}{L_{eff}} K_2 (V_{GS}-V_T)^2$$

$$I_D(SAT) \propto K_3 W_{eff} C_{ox} \upsilon_{SAT} (V_{GS}-V_T)$$

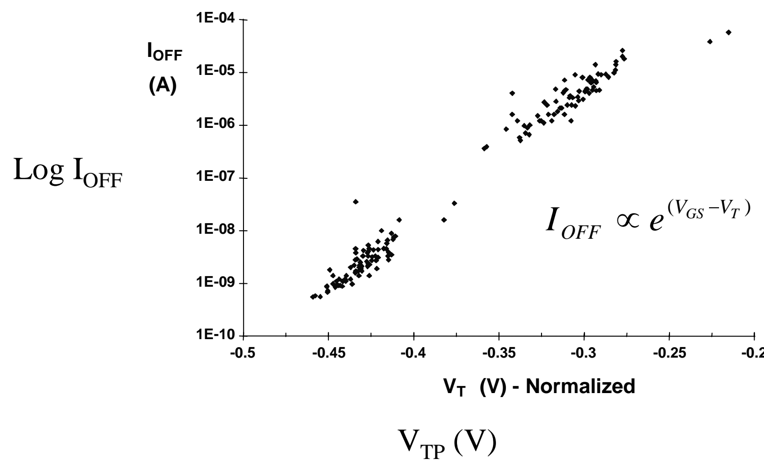


As V_T decreases, sub-threshold leakage increases

Leakage is a barrier to voltage scaling

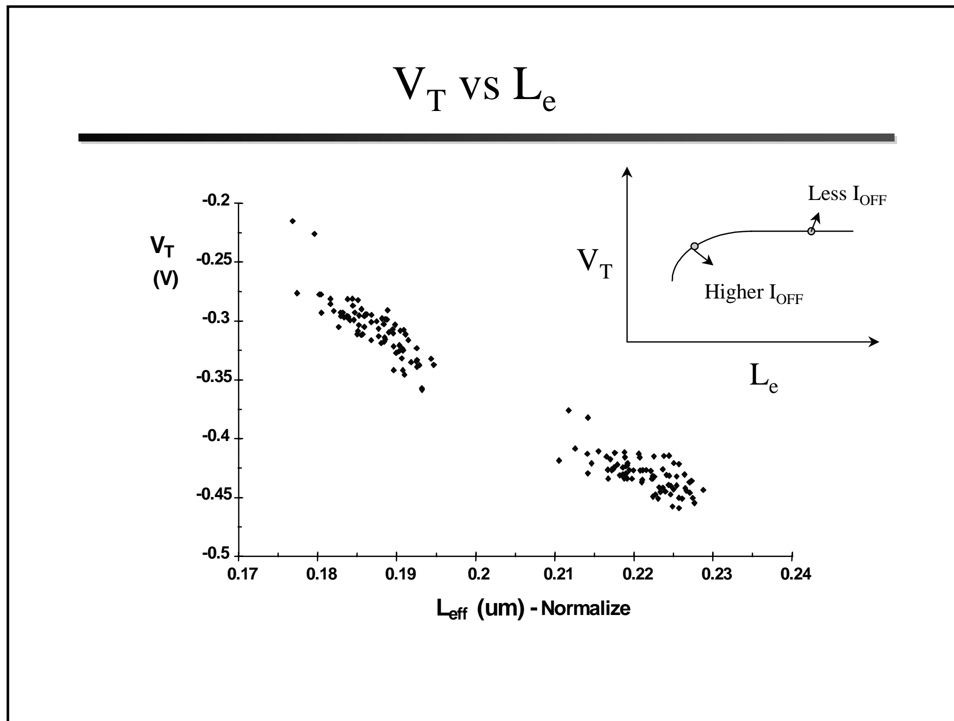
I_{OFF} vs V_T

Log I_{OFF}

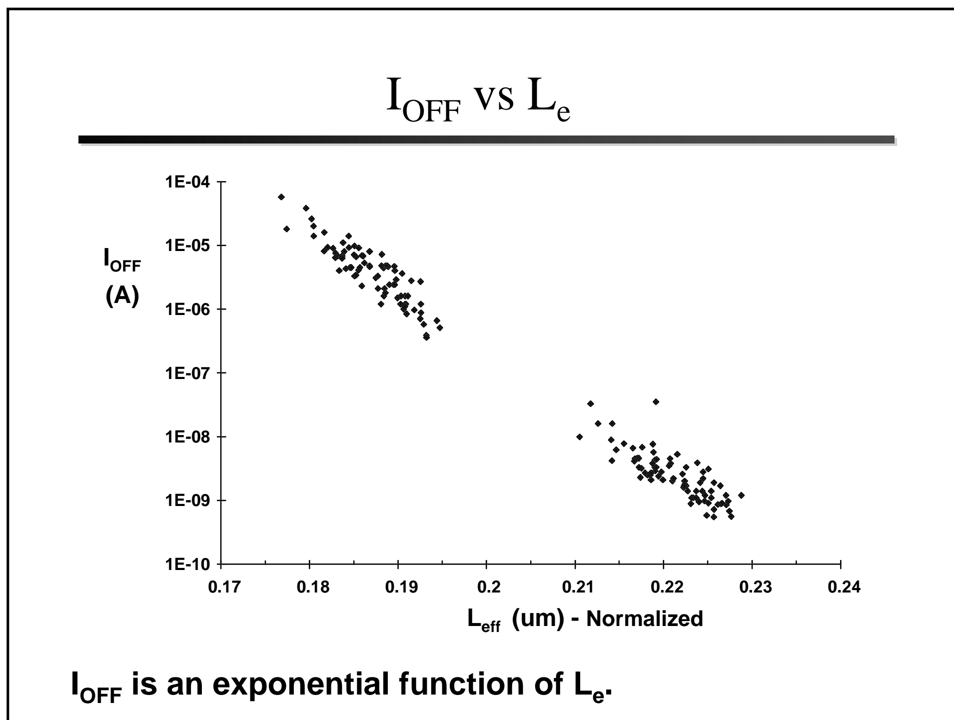


V_{TP} (V)

I_{OFF} is an exponential function of V_T.



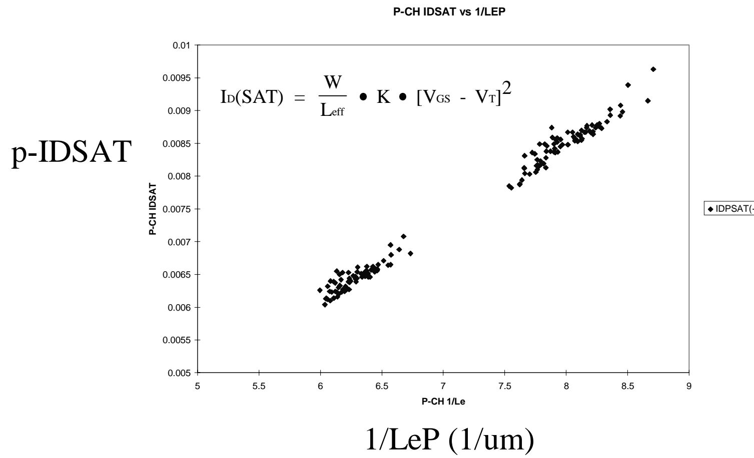
V_T vs L_e
V_T (V)
-0.2
-0.25
-0.3
-0.35
-0.4
-0.45
-0.5
0.17
0.18
0.19
0.2
0.21
0.22
0.23
0.24
L_{eff} (um) - Normalize
Less I_{OFF}
Higher I_{OFF}
V_T
L_e



I_{OFF} vs L_e
I_{OFF} (A)
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
0.17
0.18
0.19
0.2
0.21
0.22
0.23
0.24
L_{eff} (um) - Normalized
I_{OFF} is an exponential function of L_e.

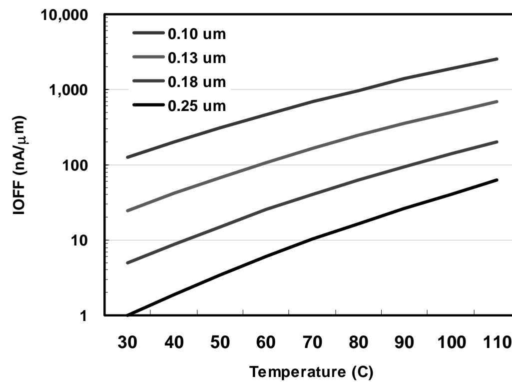
IDSAT (Drive) vs 1/Le

p-IDSAT



1/LeP (1/um)

Future: Projected Leakage Trends



I_{OFF} (0.25um) = 1 nA/um (scales 5X)
V_T (0.25um) = 450 mV (scales by 15%)

S_t (30C) = 80 mV/dec
S_t (100C) = 100
d V_T/dT = 0.7 mV/C

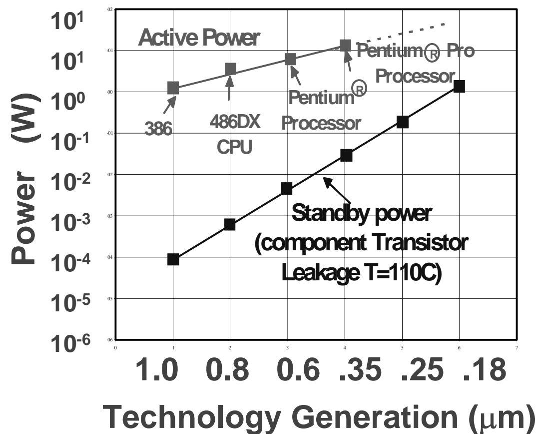
A Technology Scaling Barrier

- Constant electric field scaling (V_{CC} scaling) to control IC's active power
- Loss in gate overdrive $(V_G\text{-}V_T)^n$
- Subthreshold leakage increases with V_T scaling

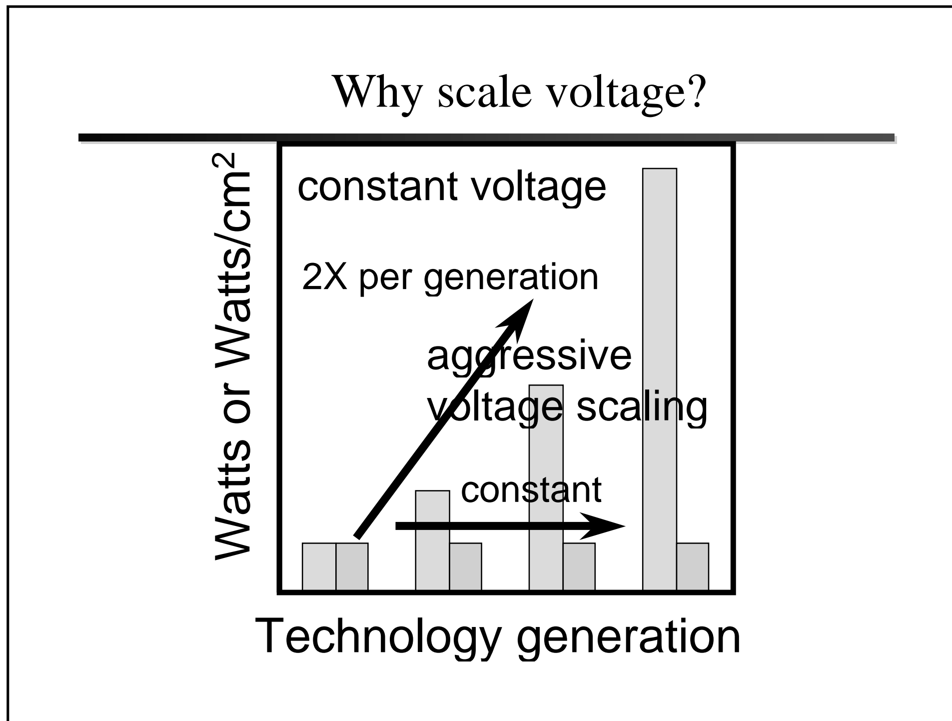
V. De et al., 1999.
A. Keshavarzi et al., 1997.
S. Thompson et al., 1997.
B. Davari, 1996.
Y. Taur et al., 1995.
T.C. Holloway et al., 1997.
R.A. Chapman et al., 1997.
M. Rodder et al., 1996.
D. Liu et al., 1993.

Why Excessive leakage an Issue?

- Leakage component to active power becomes significant % of total power
- Approaching ~10% in 0.18 μm technology
- Acceptable limit less than ~10%, implies serious challenge in V_T scaling!



Barrier high static leakage (standby) power



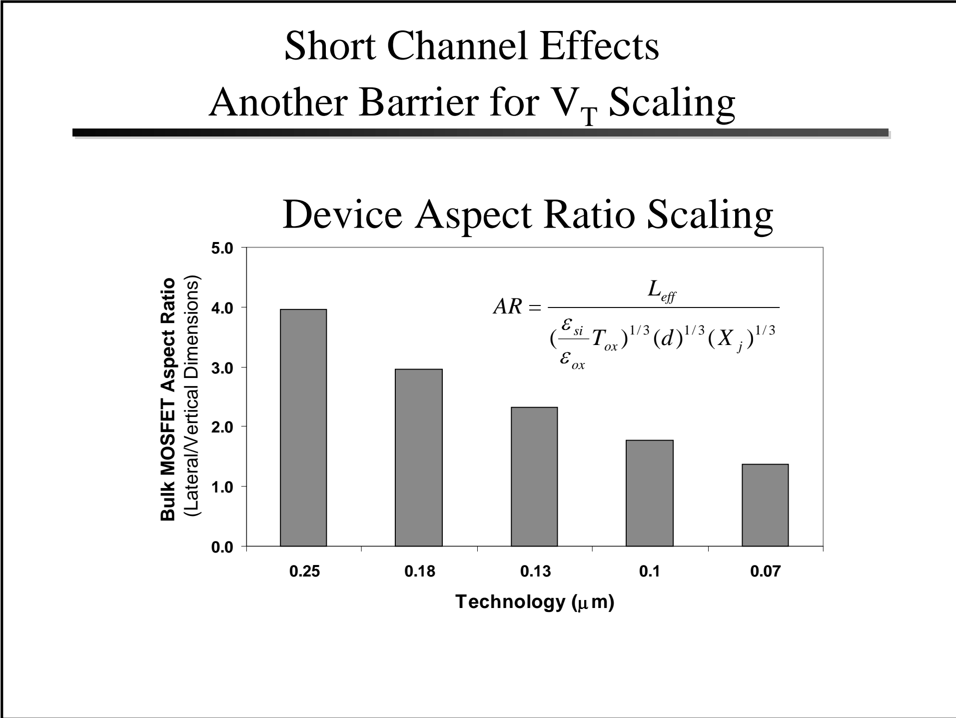
Impact of Leakage on IC Testing?

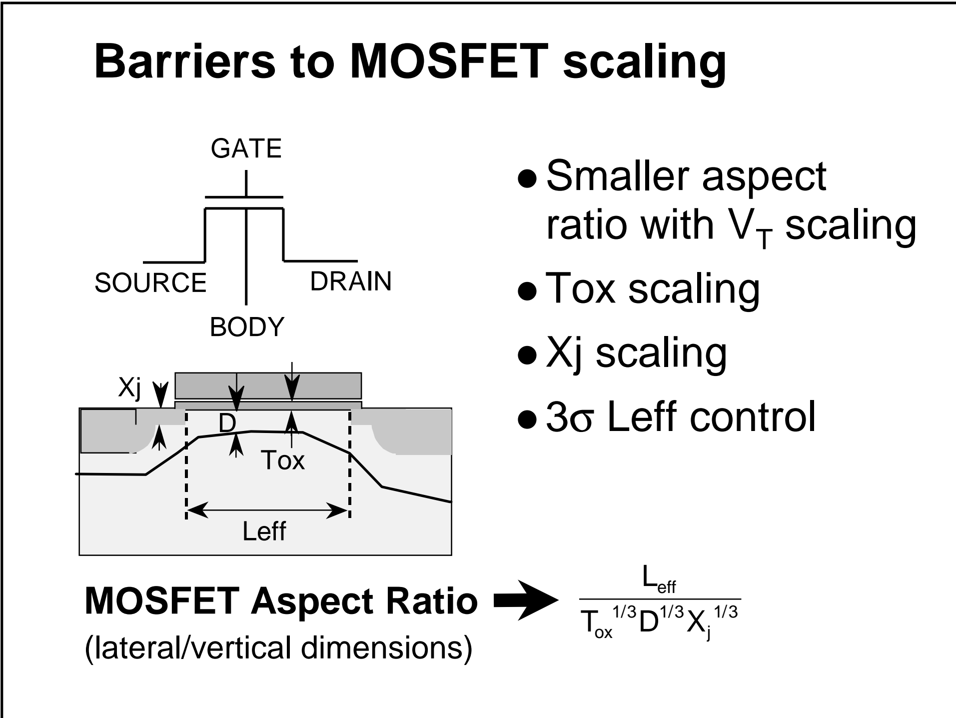
Higher intrinsic leakage challenges current based test techniques

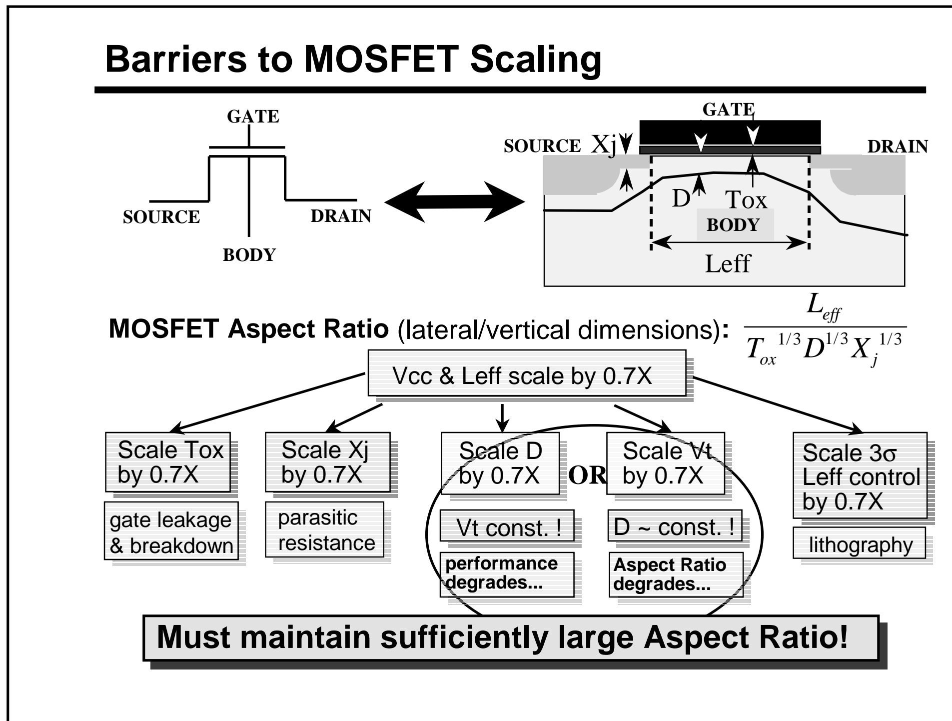
I_{DDQ} test method well established and widely accepted for defects and is necessary

I_{DDQ} testability issue - sensitivity?

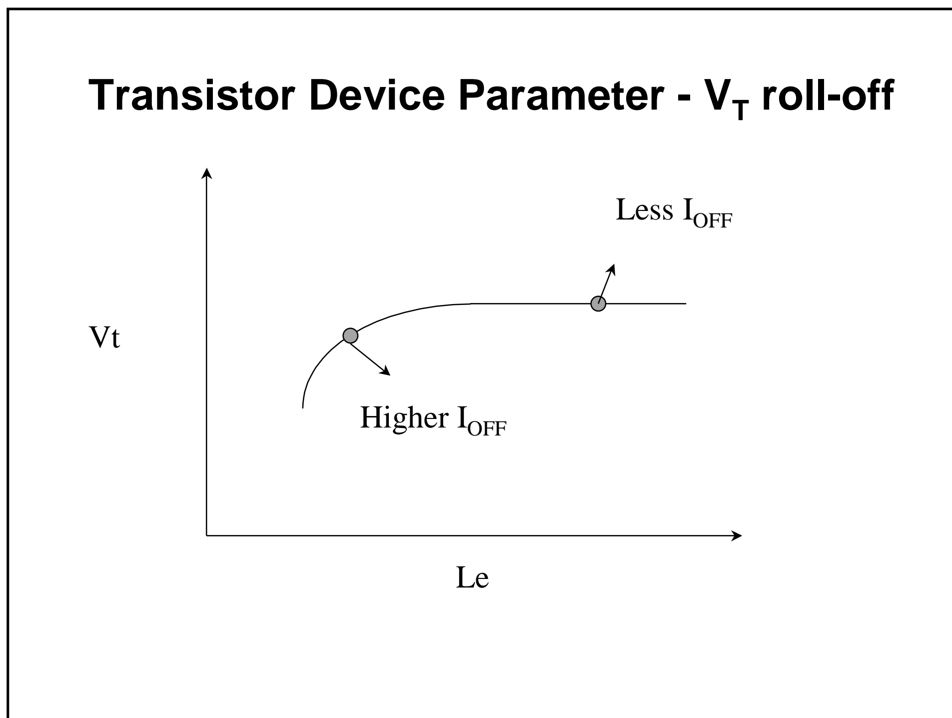
Novel testing solutions

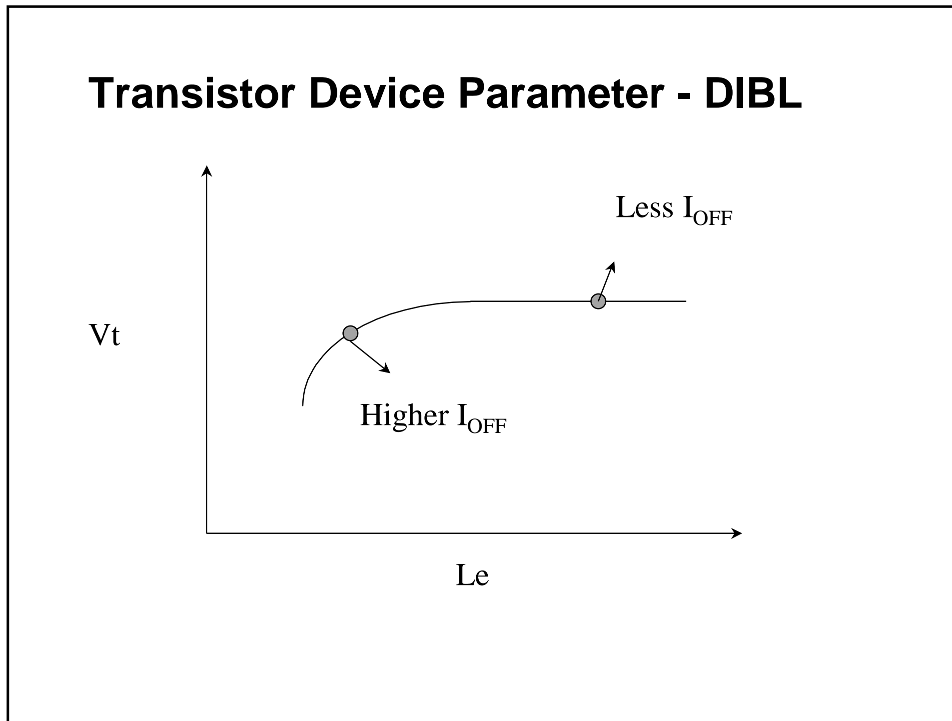

Short Channel Effects
Another Barrier for V_T Scaling
Device Aspect Ratio Scaling
Bulk MOSFET Aspect Ratio
(Lateral/Vertical Dimensions)
5.0
4.0
3.0
2.0
1.0
0.0
$AR = \frac{L_{eff}}{(\frac{\varepsilon_{si}}{\varepsilon_{ox}} T_{ox})^{1/3} (d)^{1/3} (X_j)^{1/3}}$
0.25
0.18
0.13
0.1
0.07
Technology (μm)


Barriers to MOSFET scaling
GATE
SOURCE
DRAIN
BODY
Xj
D
Tox
Leff
● Smaller aspect ratio with V_T scaling
● Tox scaling
● Xj scaling
● 3σ Leff control
MOSFET Aspect Ratio
(lateral/vertical dimensions)
$\frac{L_{eff}}{T_{ox}^{1/3} D^{1/3} X_j^{1/3}}$



$$\frac{L_{eff}}{T_{ox}^{1/3} D^{1/3} X_j^{1/3}}$$





Static logic-- pros and cons

"Complementary" logic

Inversion — Q

"True" logic

- High noise margin--robust design
- Static, lower power
- Flexibility in trip points
- Scalable across technologies
- Moderate performance
- P transistors too big--$\mu_n/\mu_p = 3$
- P stack limits fan-in
- Short-circuit current reduces speed
- Larger in size

Vout — Short Circuit Current — Vin

Domino logic--pros and cons

CLK
CLK
A
B
C
Q1
Static Gate
CLK
D1 Domino Gate
B
C
Q2
D2 Domino Gate

- High performance ~30% over static
- High NOR fan-in, less logic gates
- High fan-in complex gates possible
- Smaller area

- Lower AC noise margin ~ Vt
- Ioff could limit NOR fan-in
- High activity, higher power, ~2X
- Irreversible logic evaluation
- Scalability is not good

Effect on Soft Error Rate

- Soft errors are caused by
  - Alpha particles in materials
  - Cosmic rays from space
    - Susceptibility increases with altitude
- Soft error rate will increase
  - C, V, and T reduce
  - Smaller Q can flip bits in memory
- Parity, ECC cover memory
- Logic latches may be affected
  - Increasing node capacitance to improve soft error immunity impacts performance

Logic 1
Logic 0
$V_{induced}$

10
Soft error susceptibility
1
0.25μ 0.18μ 0.13μ 0.1μ 0.07μ

$$V_{induced} = \frac{Q_{collected}}{C_{node}} = \frac{A_{node}}{C_{node}} = \frac{0.7^2}{0.7} = 0.7$$

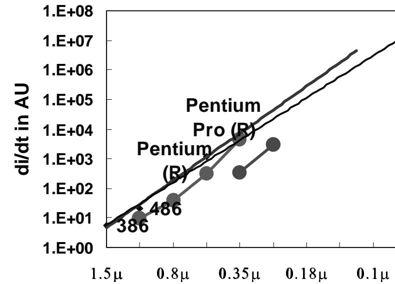
$$\frac{Susceptibility}{Bit} \propto \left(\frac{V_{induced}}{V_{dd}}\right) \times \left(\frac{1}{T}\right) = \frac{0.7}{0.7 \times 0.7} = 1.43$$

$$Soft\ error\ \overline{susceptibility}\ increases \approx 43\%$$

June 25th, 1999

Power delivery and distribution

- Supply currents reduce only linearly with voltage
- Expect parasitics to increase
  - Capacitance will increase
  - R may reduce, but not much
  - L's will not reduce
- Noise will increase
  - RI drops in power distribution
  - L(dI/dt) noise will increase
  - Supply voltage will reduce
  - Signal to noise ratio will reduce
- Solutions
  - Breakthrough in decoupling
  - Robust circuits



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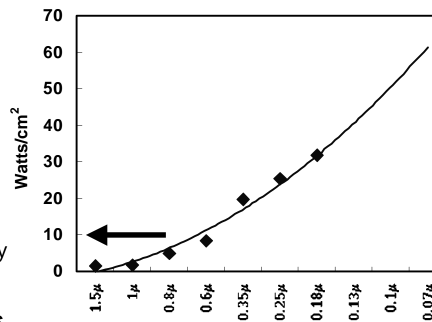
Power density

Power density will increase

Surpassed hot-plate power density in 0.6μ

Junction Temp <= 100 C is necessary
- Performance (higher freq)
- Exponential growth in leakage
- Exponential impact on reliability

Low cost and more efficient heat spreading techniques are needed



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Process technology goals

- 1. Reduce gate delay by 30% ➡ 50% freq gain
- 2. Increase density by 2x
  - 0.7 shrink on a side, 50% area reduction on compaction
  - Transistor W and L shrink by 30%
  - Interconnect pitches shrink by ~30%
  - Add metal layers to make-up for (1) pitches < 30%, and (2) RC
- 3. Scale Vdd by ~30% per generation
  - ~70% reduction in energy per transition per generation

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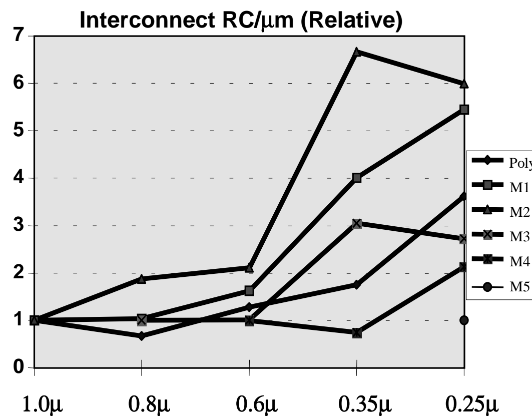
What's the net RC impact?



% increase each tech generation	R	C	RC
Poly	45%	-2%	42%
M1	53%	5%	61%
M2	46%	12%	62%
M3	39%	8%	51%
M4	18%	24%	46%

S. Borkar et. al. [1]

- **RC/μm increases ~40-60% per generation!**

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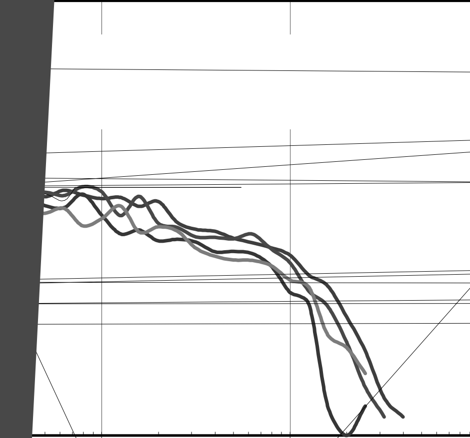
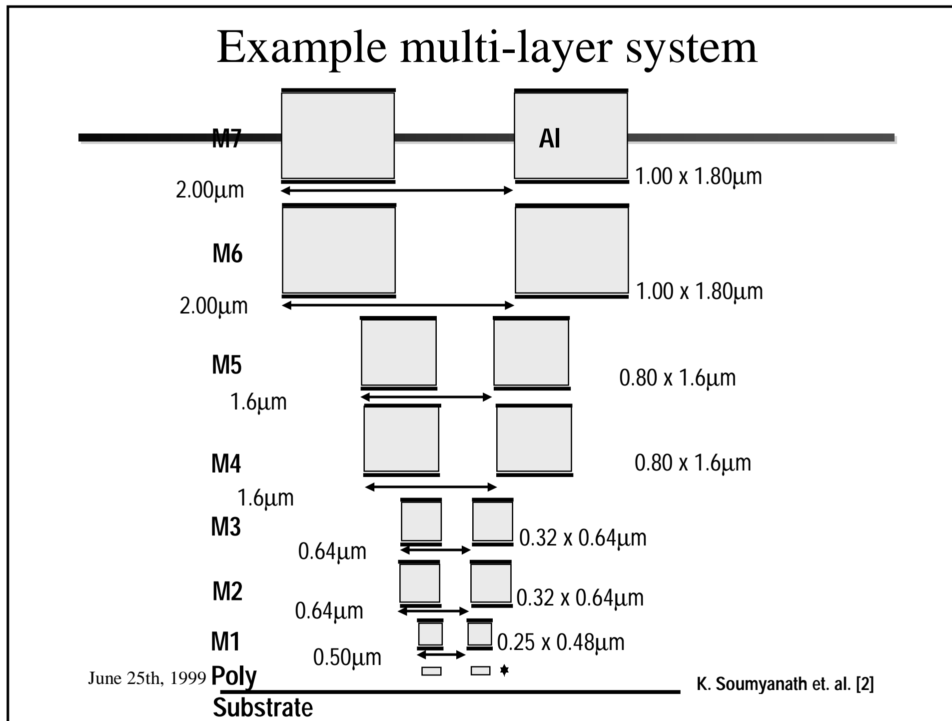
bution scaling trends

side of the story...




Example multi-layer system
M7
Al
2.00µm
1.00 x 1.80µm
M6
2.00µm
1.00 x 1.80µm
M5
1.6µm
0.80 x 1.6µm
M4
1.6µm
0.80 x 1.6µm
M3
0.64µm
0.32 x 0.64µm
M2
0.64µm
0.32 x 0.64µm
M1
0.50µm
0.25 x 0.48µm
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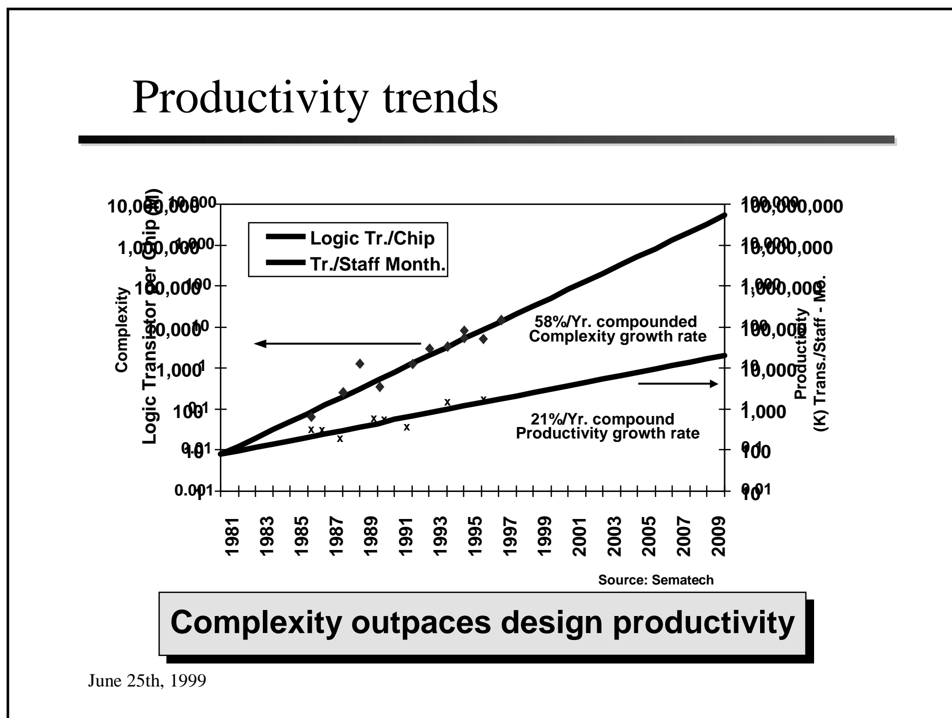
Poly
Substrate
K. Soumyanath et. al. [2]


Productivity trends
Logic Tr./Chip
Tr./Staff Month.
58%/Yr. compounded Complexity growth rate
21%/Yr. compound Productivity growth rate
Complexity
Logic Transistor per Chip (M)
Productivity
(K) Trans./Staff - Mo.
Source: Sematech
Complexity outpaces design productivity
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Summary

- Performance demand continues, barrier: Power
- Vt has to be scaled to improve performance
- Barrier: Leakage currents and leakage energy
- Make special circuits leakage tolerant
- Active leakage power will limit V_{dd} scaling
- Need active and standby leakage control techniques
- Larger divergence between cache & logic performance
- Power delivery and distribution could be the limiter
- Interconnects will get worse, not better
- Transistor scaling will be limited by Tox, Xj & SCE

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Process Variability

- *A robust design not only matches circuit design style to architecture and function but also to the CMOS technology in which the design is manufactured.*
  - *Portable among fabricators with differing process details (important for fab-less design shops)*
- *Categories of process variation*
  - *Fabricator-to-Fabricator (Inter-Fab Variation)*
  - *Inter-die variation*
  - *Intra-die variation*

Inter-Die Variations

- Functionality to be assured at process extremes
  - *A standard practice is to ensure functionality for +/- 3 sigma timing delay variation found by allowing all significant electrical parameters to vary randomly across their own 3-sigma window over many random statistical simulations of a given circuit model.*
- Response variation caused by path composition differences
  - *The ratio of intrinsic delay to RC delay of global critical paths can vary widely on larger die (On a large microprocessor, the composition delay can range from 95% intrinsic delay and 5% RC delay to 40% intrinsic delay and 60% RC delay).*